Absolute Maximum Ratings

(All voltages relative to ground.)
Voltage Range on V_{CC} or V_{BAT} ..... -0.3V to +6.0V
Voltage on Any Non-Power Pin ..... -0.3V to (V_{CC} + 0.3V)
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Maximum ..... +150°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

µSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 206.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 42°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	DS1308-18	1.71	1.8	5.5	V
		DS1308-3	2.7	3.0	5.5	
		DS1308-33	3.0	3.3	5.5	
Battery Voltage	V_{BAT}		1.3		5.5	V
Logic 1 Input	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0 Input	V_{IL}		-0.3		0.3 x V_{CC}	V

DC Electrical Characteristics

(**V_{CC} = V_{CCMIN} to V_{CCMAX}**, V_{BAT} = V_{BATMIN} to V_{BATMAX}, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Active Current (Note 3)	I_{CCA}	f_{SCL} = 400kHz			325	µA
Power-Supply Standby Current (Note 4)	I_{CCS}	-33: V_{CC} = 3.63V			125	µA
		-3: V_{CC} = 3.3V			125	
		-18: V_{CC} = 1.89V			100	
		V_{CC} = V_{CCMAX}			200	
Battery Leakage Current	I_{BATLKG}	$V_{CC} \geq V_{PF}$	-100	25	+100	nA
Input Leakage (SCL)	I_I	V_{IN} = 0V to V_{CC}	-0.1		+0.1	µA
I/O Leakage (SDA, SQW/CLKIN)	I_{IO}	I²C bus inactive, ECLK = 1	-0.1		+0.1	µA
Output Logic 0 (SDA, SQW/CLKIN), V_{OL} = 0.4V	I_{OL}	$V_{CC} \geq V_{CCMIN}$	3.0			mA
		$V_{BAT} \geq 1.3V \geq V_{CC} + 0.2V$	250			µA
Power-Fail Trip Point	V_{PF}	-33	2.70	2.82	3.00	V
		-3	2.45	2.55	2.70	
		-18	1.45	1.62	1.70	

DC Electrical Characteristics

(**V_{CC} = 0V**, V_{BAT} = V_{BATMIN} to V_{BATMAX}, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switchover Voltage	V_{SW}	V_{BAT} > V_{PF}		V_{PF}		V
		V_{BAT} < V_{PF}		V_{BAT} > V_{CC}		
Battery Current, SQW Off (Note 5)	I_{BAT1}	V_{BAT} = 3V		250		nA
		V_{BAT} = V_{BATMAX}			600	
Battery Current, SQW On (Note 6)	I_{BAT2}	V_{BAT} = 3V		550		nA
		V_{BAT} = V_{BATMAX}			1100	
Data-Retention Current (Note 7)	I_{BATDAT}	V_{BAT} = 3V		25	100	nA

AC Electrical Characteristics

(V_{CC} = V_{CCMIN} to V_{CCMAX}, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 8)	0.03		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 9)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 10, 11)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 12)	100			ns
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Rise Time of Both SDA and SCL Signals	t_R	(Note 13)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 13)	20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for each Bus Line	C_B	(Note 13)			400	pF
SCL Spike Suppression	t_{SP}			60		ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 14)		100		ms
Timeout Interval	$t_{TIMEOUT}$	(Note 15)	25		35	ms

Power-Up/Down Characteristics

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 16)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}		1	2	ms
V_{CC} Slew Rate (V_{PF} to 0V)	t_{VCCF}			1/50	V/µs
V_{CC} Slew Rate (0V to V_{PF})	t_{VCCR}			1/1	V/µs

Capacitance

(T_A = +25°C, unless otherwise noted.) (Note 16)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Capacitance	C_I		10		pF
I/O Capacitance	C_O		10		pF

Warning: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 2: Limits are 100% production tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are not guaranteed.
Note 3: SCL clocking at max frequency. V_{SCL} = 0V to V_{CC}.
Note 4: Specified with I2C bus inactive. Timekeeping and square-wave functions operational.
Note 5: CH = ECLK = SQWE = 0.
Note 6: CH = ECLK = 0, SQWE = RS1 = RS0 = 1, I_{OUT} = 0mA.
Note 7: CH = 1. ECLK = SQWE = 0.
Note 8: The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if SCL is held low for $t_{TIMEOUT}$.
Note 9: After this period, the first clock pulse is generated.
Note 10: A device must internally provide a hold time of at least 300ns for the SDA signal (referenced to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 11: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 12: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
Note 13: C_B is the total capacitance of one bus line, including all connected devices, in pF.
Note 14: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $2.4V \leq V_{CC} \leq V_{CCMAX}$.
Note 15: The DS1308 can detect any single SCL clock held low longer than $t_{TIMEOUTMIN}$. The device's I2C interface is in reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. Once the part detects this condition the SDA output is released. The oscillator must be running for this function to work.
Note 16: Guaranteed by design and not 100% production tested.

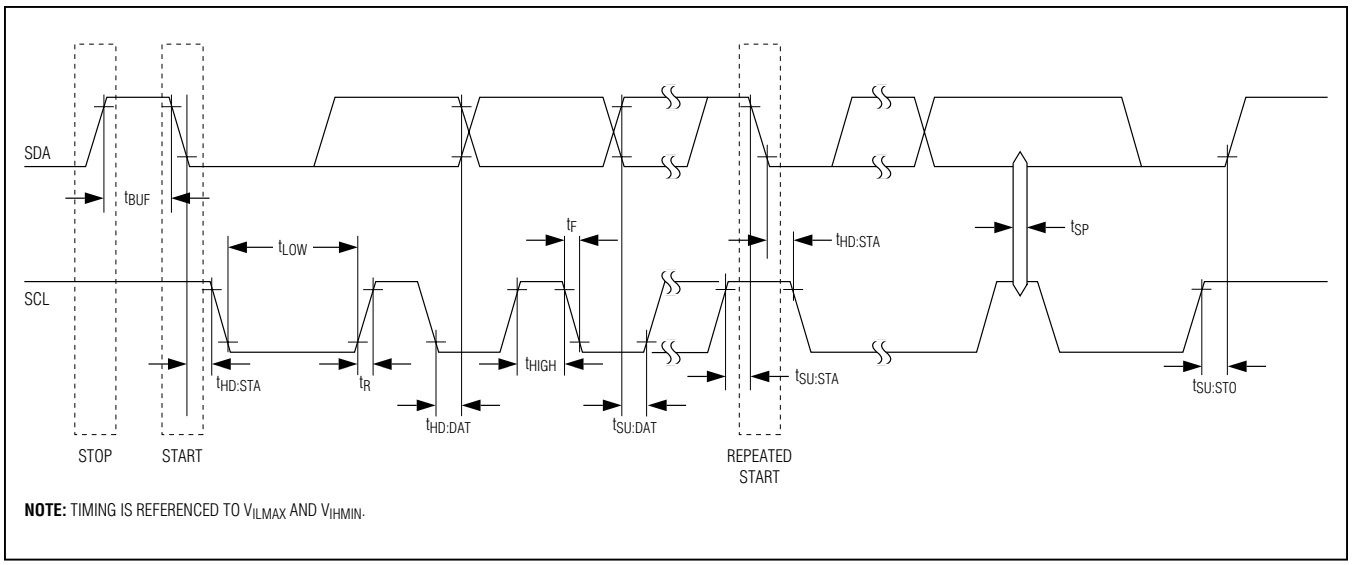


Figure 1. Data Transfer on I2C Serial Bus

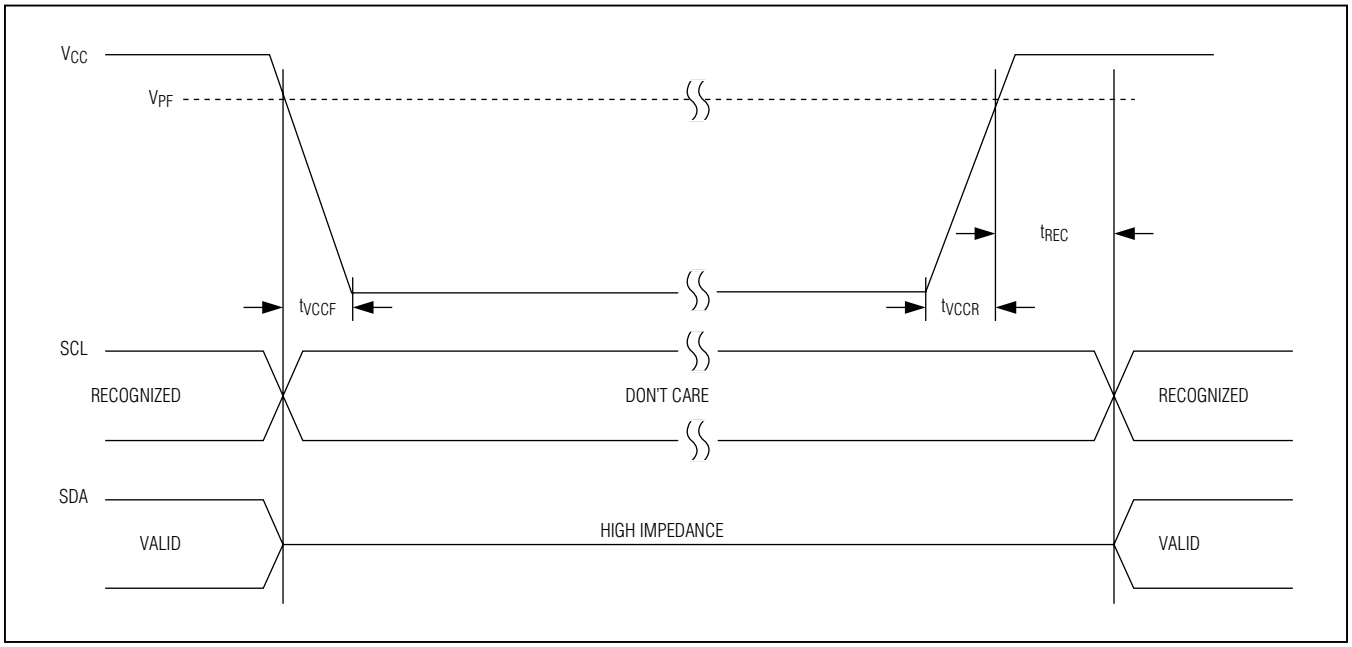
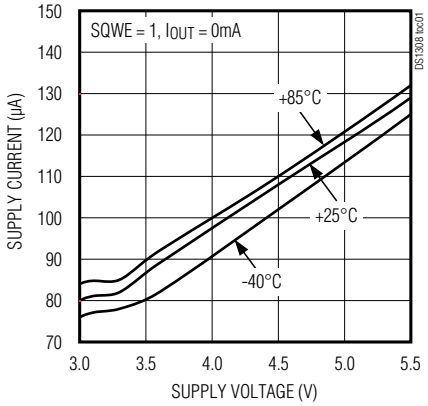


Figure 2. Power-Up/Power-Down Timing

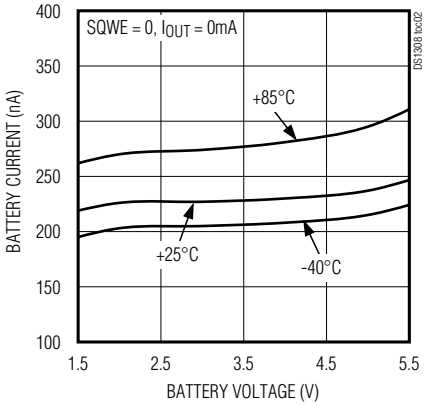
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.)

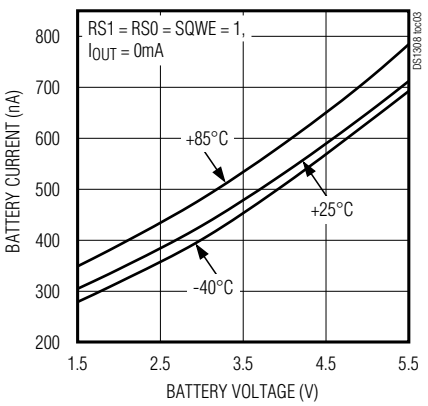
SUPPLY CURRENT vs. SUPPLY VOLTAGE



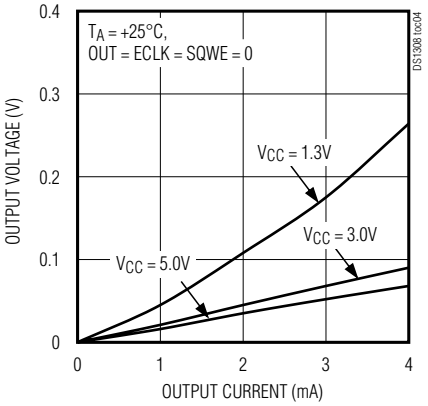
BATTERY CURRENT (SQW OFF) vs. BATTERY VOLTAGE



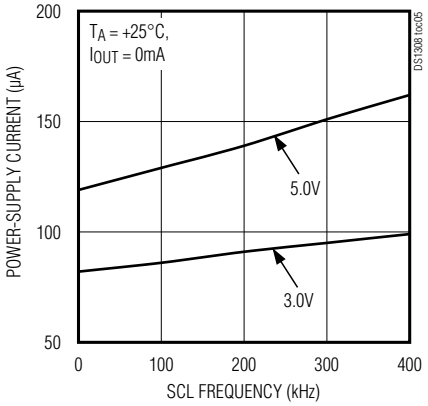
BATTERY CURRENT (SQW ON) vs. BATTERY VOLTAGE



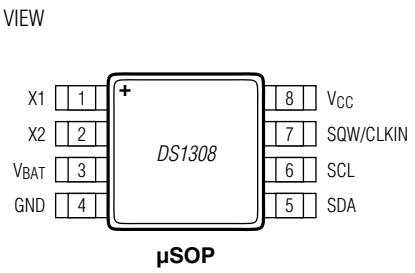
SQW/CLKIN OUTPUT-VOLTAGE LOW vs. OUTPUT CURRENT



POWER-SUPPLY CURRENT vs. SCL FREQUENCY



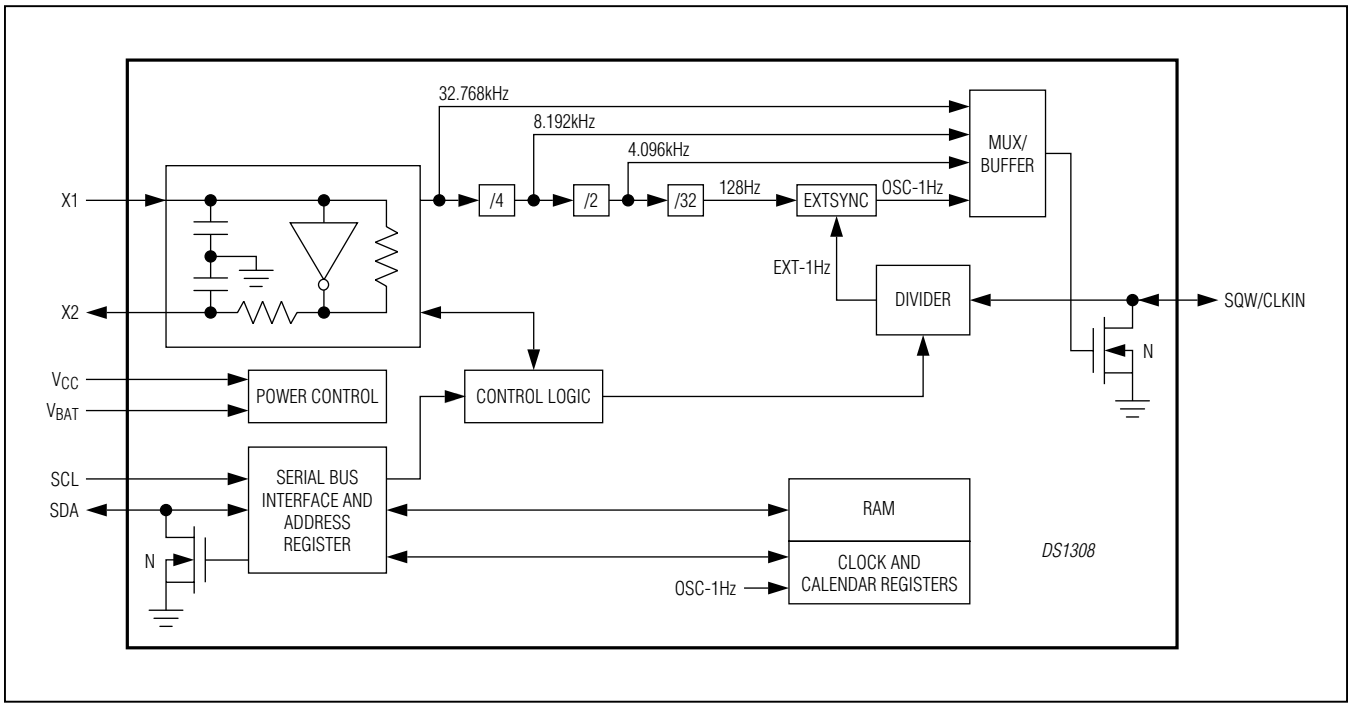
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	X1	32.768kHz Crystal Connections. The internal oscillator circuitry is designed for use with a crystal having a specified load capacitance (C_L) of 6pF. **Note:** For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Maxim Real-Time Clocks (RTCs).*
2	X2	
3	V_{BAT}	Battery Supply Input for Lithium Cell or Other Energy Source. Battery voltage must be held between the minimum and maximum limits for proper operation. Diodes placed in series between the backup source and the V_{BAT} pin can prevent proper operation. If a backup supply is not required, V_{BAT} must be grounded. UL recognized to ensure against reverse charging when used with a lithium cell.
4	GND	Ground
5	SDA	Serial Data Input/Output for the I²C serial interface. It is an open-drain output and requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.
6	SCL	Serial Clock Input for the I²C serial interface. Used to synchronize data movement on the serial interface. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.
7	SQW/CLKIN	Square-Wave Output/Clock Input. This I/O pin is used to output one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz) or accept an external clock input to drive the RTC counter. In the output mode (ECLK = 0), it is open drain and requires an external pullup resistor. The square-wave operates on V_{CC}, or on V_{BAT} with BBCLK = 1. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin may be left unconnected.
8	V_{CC}	Primary Power Supply. Decouple the power supply with a 0.1µF capacitor to ground.

Functional Diagram



Detailed Description

The DS1308 serial RTC is a low-power, full BCD clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I²C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The DS1308 has a built-in power-sense circuit that detects power failures and automatically switches to the V_{BAT} supply.

Operation

The DS1308 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{BAT} is greater than V_{CC}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PF}. If V_{BAT} is less than V_{PF}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT}. The oscillator and timekeeping functions are maintained from the V_{BAT} source until V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC}. The *Functional Diagram* shows the main elements of the DS1308.

An enable bit in the seconds register (CH) controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PCB leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within 1 second.

On the first application of power to the device, the time and date registers are reset to 01/01/00 01 00:00:00 (DD/MM/YY DOW HH:MM:SS), and CH bit in the seconds register is set to 0.

Freshness Seal Mode

When a battery is first attached to the device, the device does not immediately provide battery-backup power to the RTC or internal circuitry. After V_{CC} exceeds V_{PF}, the devices leave the freshness seal mode and provide battery-backup power whenever V_{CC} subsequently falls below V_{BAT}. This mode allows attachment of the battery during product manufacturing, but no battery capacity is consumed until after the system has been activated for the first time. As a result, minimum battery energy is used during storage and shipping.

Oscillator Circuit

The DS1308 uses an external 6pF 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. See Table 2 for the external crystal parameters. The *Functional Diagram* shows a simplified schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Whenever $V_{CC} > V_{PF}$, a 5µs glitch filter at the output of the crystal oscillator is enabled.

Table 1. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	No	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	Yes	V_{CC}

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 3 shows a typical PCB layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Maxim Real-Time Clocks (RTCs)* for detailed information.

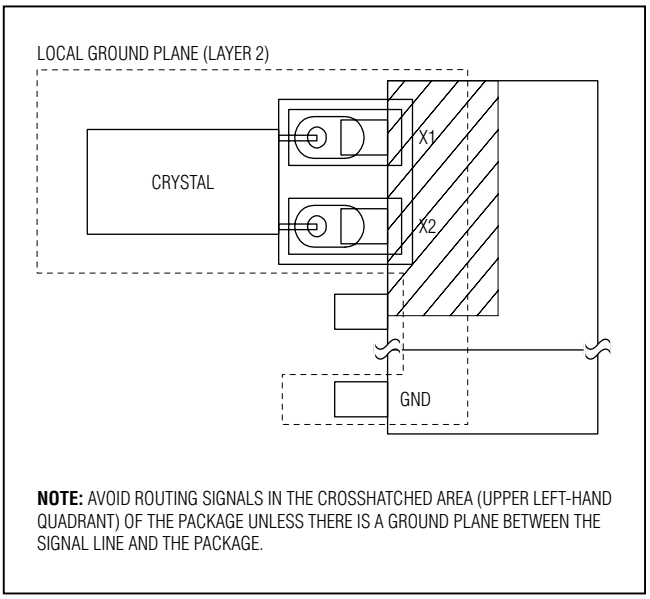


Figure 3. Typical PCB Layout for Crystal

Table 2. Crystal Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			100	kΩ
Load Capacitance	C_L		6		pF

Note: *The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Maxim Real-Time Clocks (RTCs) for additional specifications.*

RTC and RAM Address Map

Table 3 shows the address map for the RTC and RAM registers. The RTC registers and control register are located in address locations 00h–07h. The RAM registers are located in address locations 08h–3Fh. During a multibyte access, when the register pointer reaches 3Fh (the end of RAM space) it wraps around to location 00h (the beginning of the clock space). On an I2C START, or register pointer incrementing to location 00h, the current time and date is transferred to a second set of registers. The time and date in the secondary registers are read in a multibyte data transfer, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The clock can be halted whenever the timekeeping functions are not required, which minimizes V_{BAT} current (I_{BATDAT}) when V_{CC} is not applied.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the DS1308. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The DS1308 runs in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit, with logic high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). If the 12/$\overline{24}$-hour mode select is changed, the hours register must be re-initialized to the new format.

Table 3. RTC and RAM Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	CH	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Hours	1–12 + AM/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	01–31
05h	0	0	0	10 Month	Month				Month	01–12
06h	10 Year				Year				Year	00–99
07h	OUT	ECLK	OSF	SQWE	LOS	BBCLK	RS1	RS0	Control	
08h–3Fh									RAM 56 x 8	00h–FFh

Note: *Bits listed as "0" always read as a 0.*

Control Register (07h)

The control register controls the operation of the SQW/CLKIN pin and provides oscillator status.

Bit #	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Name	OUT	ECLK	OSF	SQWE	LOS	BBCLK	RS1	RS0
POR	1	0	1	1	1	1	1	1

Bit 7: Output Control (OUT). Controls the output level of the SQW/CLKIN pin when the square-wave output is disabled and V_{CC}>V_{PF}. If SQWE = 0, the logic level on the SQW/CLKIN pin is 1 if OUT = 1; it is 0 if OUT = 0. See Table 4.

Bit 6: Enable Clock Input (ECLK). This bit controls the direction of the SQW/CLKIN pin (see Table 4). When ECLK = 1, the SQW/CLKIN pin is an input, with the expected input rate defined by the states of RS1 and RS0. When ECLK = 0, the SQW/CLKIN pin is an output, with the square-wave frequency defined by the states of RS1 and RS0.

Bit 5: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and can be used to judge the validity of the clock and calendar data. This bit is edge triggered, and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that may cause the OSF bit to be set:

The first time power is applied.
The voltage present on V_{CC} and V_{BAT} are insufficient to support oscillation.
The CH bit is set to 1, disabling the oscillator.
External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bit 4: Square-Wave Enable (SQWE). When set to logic 1, this bit enables the oscillator output to operate with either V_{CC} or V_{BAT} applied. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits.

Bit 3: Loss of Signal (LOS). This status bit indicates the state of the CLKIN pin. The LOS bit is set to 1 when the RTC counter is no longer conditioned by the external clock. This occurs when 1) ECLK = 0, or 2) when the CLKIN input signal stops toggling, or 3) when the CLKIN frequency differs by more than ±0.8% from the selected input frequency. This bit remains a 1 until written to 0. Attempting to write LOS = 1 leaves the value unchanged. Clearing the LOS flag when the CLKIN frequency is invalid inhibits subsequent detections of the input frequency deviation.

Bit 2: Battery Backup Clock (BBCLK). When set to logic 1, this bit enables the SQW/CLKIN I/O while the part is powered by V_{BAT}. When set to logic 0, this bit disables the SQW/CLKIN I/O while the part is powered by V_{BAT}.

Bits 1 and 0: Rate Select (RS1 and RS0). These bits control the frequency of the SQW/CLKIN output when the square-wave has been enabled (SQWE = 1). Table 4 lists the square-wave frequencies that can be selected with the RS bits.

Table 4. SQW/CLKIN Pin Functions

OUT	ECLK	SQWE	RS1	RS0	SQW/CLKIN
X	0	1	0	0	1Hz output
X	0	1	0	1	4.096kHz output
X	0	1	1	0	8.192kHz output
X	0	1	1	1	32.768kHz output
0	0	0	X	X	0
1	0	0	X	X	1
X	1	X	0	0	1Hz input
X	1	X	0	1	50Hz input
X	1	X	1	0	60Hz input
X	1	X	1	1	32.768kHz input

X = Don't care.

External Synchronization

When an external clock reference is used, the input from SQW/CLKIN is divided down to 1Hz. The 1Hz from the divider (Ext-1Hz, see *Functional Diagram*) is used to correct the 1Hz that is derived from the 32.768kHz oscillator (Osc-1Hz). As Osc-1Hz drifts in relation to Ext-1Hz, Osc-1Hz is digitally adjusted.

As shown in the *Functional Diagram*, the three highest frequencies driving the SQW/CLKIN pin are derived from the uncorrected oscillator, while the 1Hz output is derived from the adjusted Osc-1Hz signal.

Conceptually, the circuit can be thought of as two 1Hz signals, one derived from the internal oscillator and the other from the external reference clock, with the oscillator-derived 1Hz signal being locked to the 1Hz signal derived from the external reference clock. The edges of the 1Hz signals do not need to be aligned with each other. While the external clock source is present and within tolerance, the Ext-1Hz and Osc-1Hz maintain their existing lock, regardless of their edge alignment, with periodic correction of the Osc-1Hz signal. If the external signal is lost and then regained sometime later, the signals re-lock with whatever new alignment exists (Figure 4).

The Ext-1Hz is used by the device as long as it is within tolerance, which is about 0.8% of Osc-1Hz. While Ext-1Hz is within tolerance, the skew between the two signals may shift until a change of about 7.8ms accumulates, after which Osc-1Hz signal is adjusted (Figure 5). The adjustment is accomplished by digitally adjusting the 32kHz oscillator divider chain.

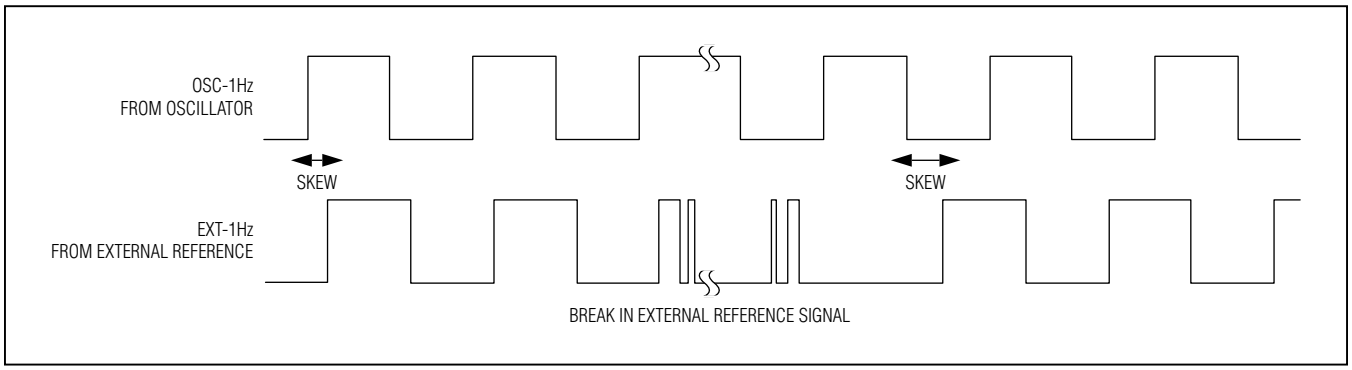


Figure 4. Loss and Reacquisition of External Reference Clock

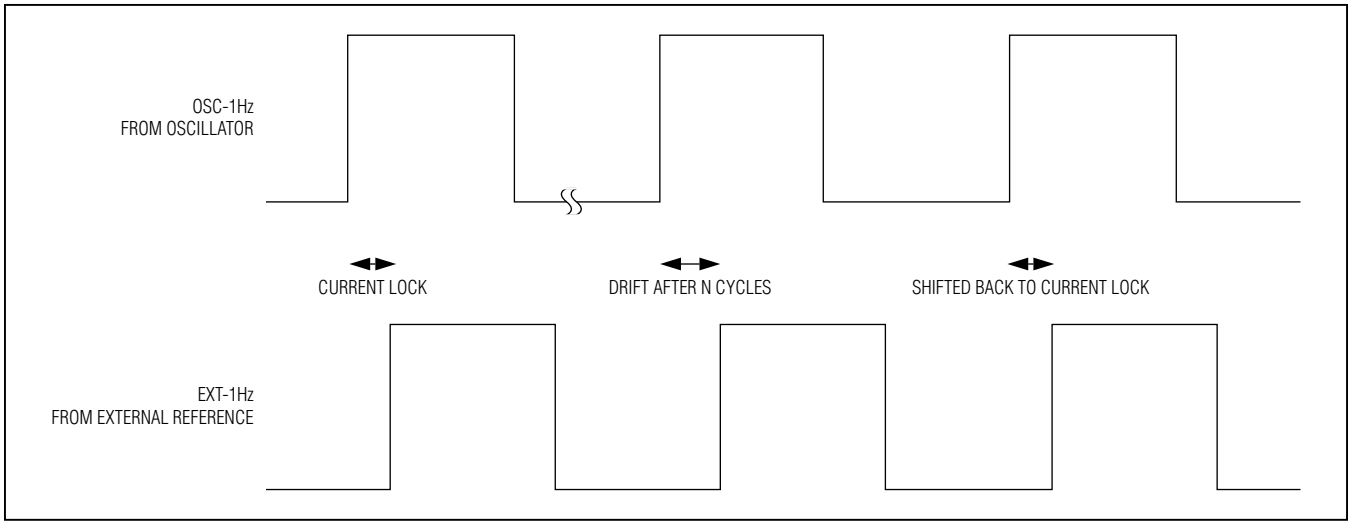


Figure 5. Drift Adjustment of Internal 1Hz to External Reference Clock

If the difference between Ext-1Hz and Osc-1Hz is greater than about 0.8%, Osc-1Hz runs unadjusted (see Figure 4) and the loss of signal (LOS) is set, provided the enable external clock input bit (ECLK) is set.

I2C Serial Port Operation

I2C Slave Address

The DS1308's slave address byte is D0h. The first byte sent to the device includes the device identifier and the R/$\overline{W}$ bit (Figure 6). The device address sent by the I2C master must match the address assigned to the device.

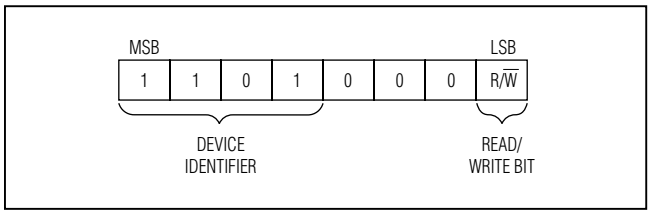


Figure 6. Slave Address Byte

I2C Definitions

The following terminology is commonly used to describe I2C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 1 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 1 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it immediately initiates a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 1 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read (Figure 1). The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An acknowledge (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data

bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The slave address is D0h and cannot be modified by the user. When the R/$\overline{W}$ bit is 0 (such as in D0h), the master is indicating it writes data to the slave. If R/$\overline{W}$ = 1, (D1h in this case), the master is indicating it wants to read from the slave. If an incorrect slave address is written, the DS1308 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the starting memory address, writes multiple data bytes, and generates a STOP condition.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is

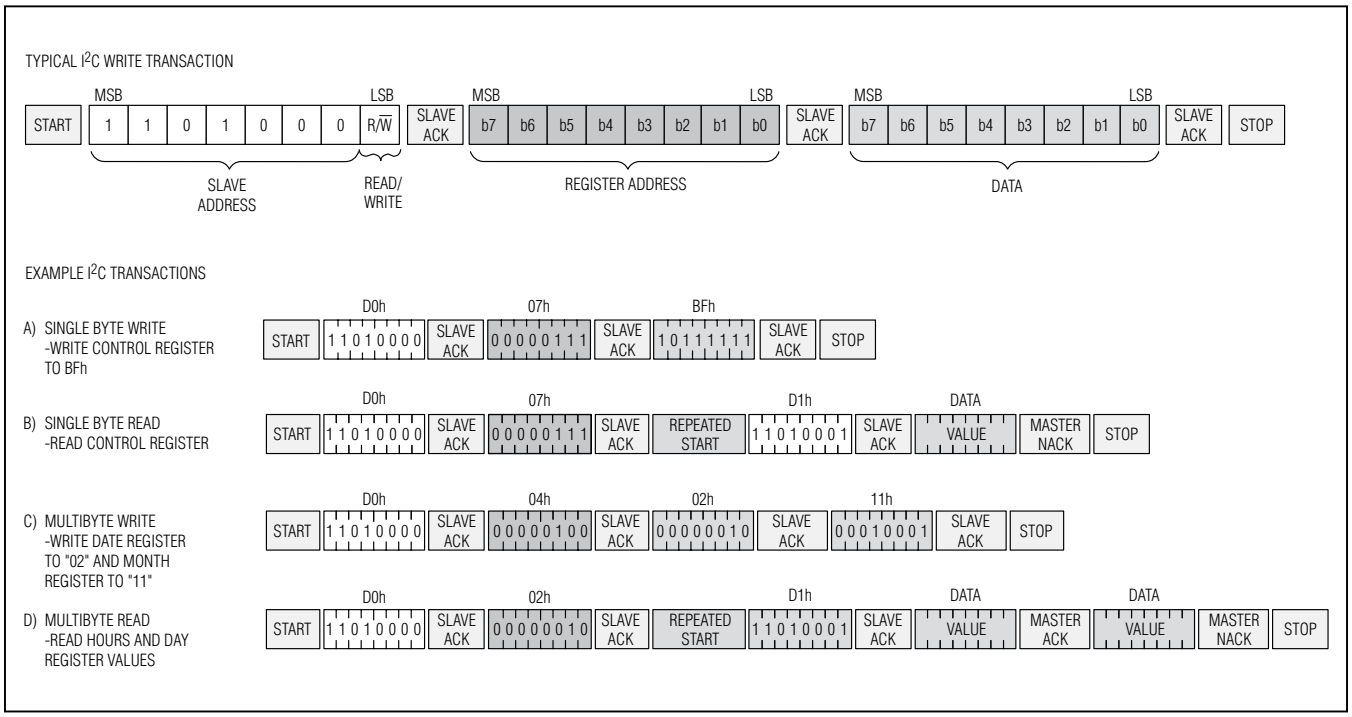


Figure 7. I²C Transactions

impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. See Figure 7 for a read example using the repeated START condition to specify the starting memory location.

Reading Multiple Bytes From a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and then it generates a STOP condition.

Bus Timeout

To avoid an unintended I²C interface timeout, SCL should not be held low longer than $t_{TIMEOUTMIN}$. The I²C interface is in the reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. When the part detects this condition, SDA is released and allowed to float. For the timeout function to work, the oscillator must be enabled and running.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS1308, decouple the V_{CC} power supply with a 0.01µF and/or 0.1µF capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Using Open-Drain Outputs

The SQW/CLKIN output is open drain and therefore requires an external pullup resistor to realize a logic-high output level.

SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high output level.

Because the DS1308 does not use clock cycle stretching, a master using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

Battery Charge Protection

The DS1308 contains Maxim's redundant battery-charge protection circuit to prevent any charging of an external battery. The DS1308 is recognized by Underwriters Laboratories (UL) under file E141114.

Handling, PCB Layout, and Assembly

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line.

The lead(Pb)-free/RoHS package can be soldered using a reflow profile that complies with JEDEC J-STD-020.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

Chip Information

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1308U-18+	-40°C to +85°C	8 µSOP
DS1308U-3+*	-40°C to +85°C	8 µSOP
DS1308U-33+	-40°C to +85°C	8 µSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µSOP	U8+1	21-0036	90-0092

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—
1	4/13	Added -18 ordering variant and UL certification number	2, 15
2	7/14	Added missing specs for 3.0V version	2
3	4/15	Revised *Benefits and Features* section	1

