3V 10-Tap Silicon Delay Line

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground .....-0.5V to +6.0V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C, V_{CC} = 2.7V to 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7	3.3	3.6	V
High-Level Input Voltage	V_{IH}	(Note 1)	2.2		V_{CC} + 0.3	V
Low-Level Input Voltage	V_{IL}	(Note 1)	-0.3		+0.8	V
Input Leakage Current	I_I	$0V \le V_I \le V_{CC}$	-1.0		+1.0	µA
Active Current	I_{CC}	V_{CC} = max, period = min (Note 2)		40	150	mA
High-Level Output Current	I_{OH}	V_{CC} = min, V_{OH} = 2.3V			-1.0	mA
Low-Level Output Current	I_{OL}	V_{CC} = min, V_{OL} = 0.5V	12			mA

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C, V_{CC} = 2.7V to 3.6V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	t_{WI}	(Note 6)	10% of tap 10			ns
Input to Tap Delay (Delays ≤ 40ns)	t_{PLH} t_{PHL}	+25°C, 3.3V (Notes 3, 5, 6, 7, 9)	-2	Table 1	+2	ns
		0°C to +70°C (Notes 4–7)	-3	Table 1	+3	
		-40°C to +85°C (Notes 4–7)	-4	Table 1	+4	
Input to Tap Delay (Delays > 40ns)	t_{PLH} t_{PHL}	+25°C, 3.3V (Notes 3, 5, 6, 7, 9)	-5	Table 1	+5	%
		0°C to +70°C (Notes 4–7)	-8	Table 1	+8	
		-40°C to +85°C (Notes 4–7)	-13	Table 1	+13	
Power-Up Time	t_{PU}				100	ms
Input Period	Period	(Note 8)	2 (t_{WI})			ns

CAPACITANCE

(T_A = +25°C.)

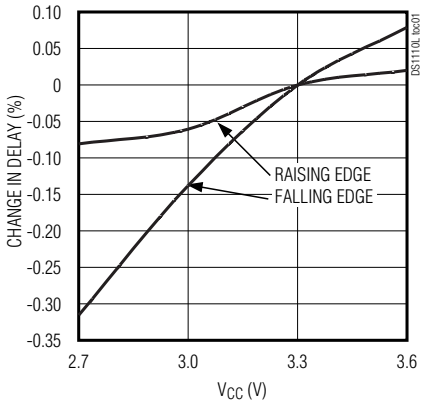
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}			5	10	pF

Note 1: All voltages are referenced to ground.
Note 2: Measured with outputs open.
Note 3: Initial tolerances are ± with respect to the nominal value at +25°C and V_{CC} = 3.3V for both leading and trailing edges.
Note 4: Temperature and voltage tolerances are with respect to the nominal delay value over stated temperature range and a 2.7V to 3.6V range.
Note 5: Intermediate delay values are available on a custom basis.
Note 6: See *Test Conditions* section.
Note 7: All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if tap 1 slows down, all other taps also slow down; tap 3 can never be faster than tap 2.
Note 8: Pulse width and period specifications may be exceeded; however, accuracy is application sensitive (decoupling, layout, etc.).
Note 9: For Tap 1 delays greater than 20ns, the tolerance is ±3ns or ±5%, whichever is greater.

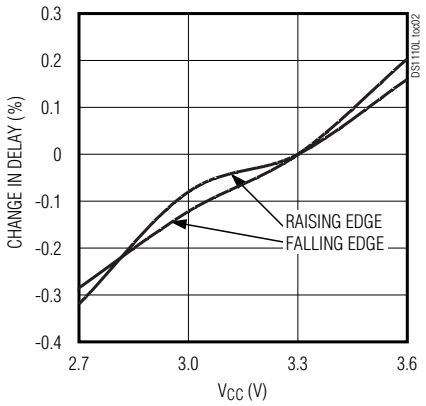
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

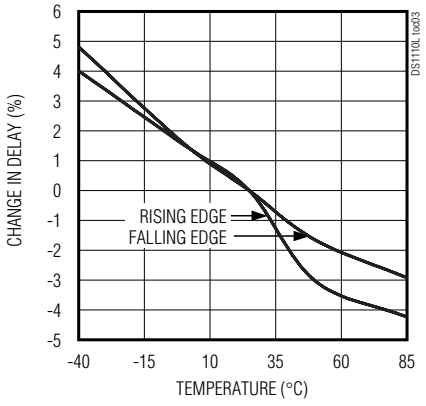
DELAY CHANGE (%) vs. V_{CC} DS1110L-500



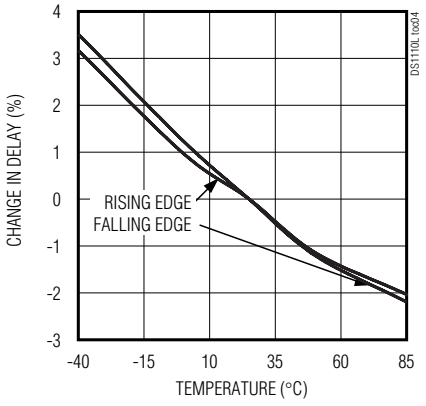
DELAY CHANGE (%) vs. V_{CC} DS1110L-250



CHANGE IN DELAY (%) vs. TEMPERATURE DS1110L-500



CHANGE IN DELAY (%) vs. TEMPERATURE DS1110L-250

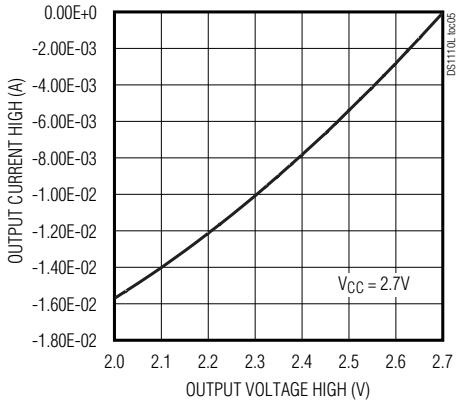


3V 10-Tap Silicon Delay Line

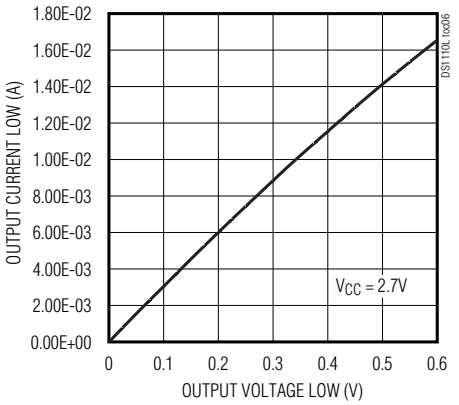
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

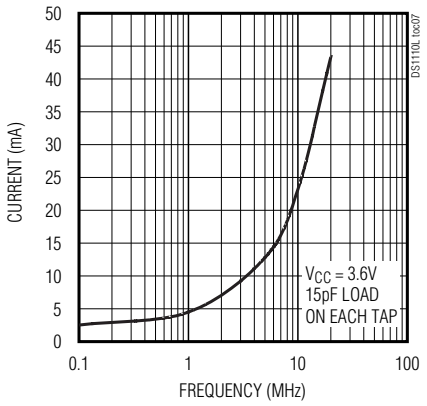
OUTPUT CURRENT HIGH vs. OUTPUT VOLTAGE HIGH



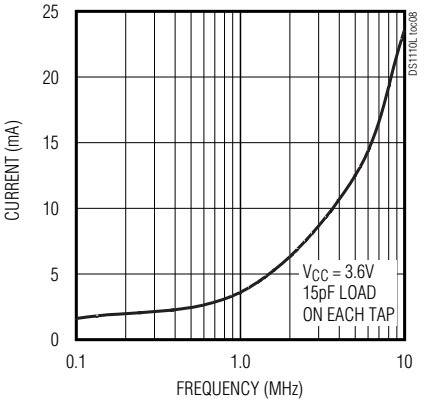
OUTPUT CURRENT LOW vs. OUTPUT VOLTAGE LOW



ACTIVE CURRENT vs. INPUT FREQUENCY DS1110L-250



ACTIVE CURRENT vs. INPUT FREQUENCY DS1110L-500



Pin Description

PIN	NAME	FUNCTION
1	IN	Input
2	N.C.	No Connection
7	GND	Ground
13, 3, 12, 4, 11, 5, 10, 6, 9, 8	Tap 1–Tap 10	Tap Output Number
14	VCC	2.7V to 3.6V

Detailed Description

The DS1110L 10-tap delay line is a 3V version of the DS1110. It has 10 equally spaced taps providing delays from 10ns to 500ns. The device is offered in a standard 14-pin TSSOP. The DS1110L series delay lines provide a nominal accuracy of ±5% or ±2ns, whichever is greater, at 3.3V and +25°C. The DS1110L is characterized to operate from 2.7V to 3.6V. The DS1110L reproduces the input-logic state at the tap 10 output after a fixed delay as specified by the dash-number suffix of the part number (Table 1). The DS1110L produces both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to 10 74LS-type loads. Dallas Semiconductor can customize standard products to meet specific needs. Figure 1 is the DS1110_L logic diagram and Figure 2 shows the timing diagram for the silicon delay line.

Table 1. Part Number by Delay (t_{PHL}, t_{PLH})

PART	TOTAL DELAY (ns)	DELAY/TAP (ns)
DS1110LE-100	100	10
DS1110LE-125	125	12.5
DS1110LE-150	150	15
DS1110LE-175	175	17.5
DS1110LE-200	200	20
DS1110LE-250	250	25
DS1110LE-300	300	30
DS1110LE-350	350	35
DS1110LE-400	400	40
DS1110LE-450	450	45
DS1110LE-500	500	50

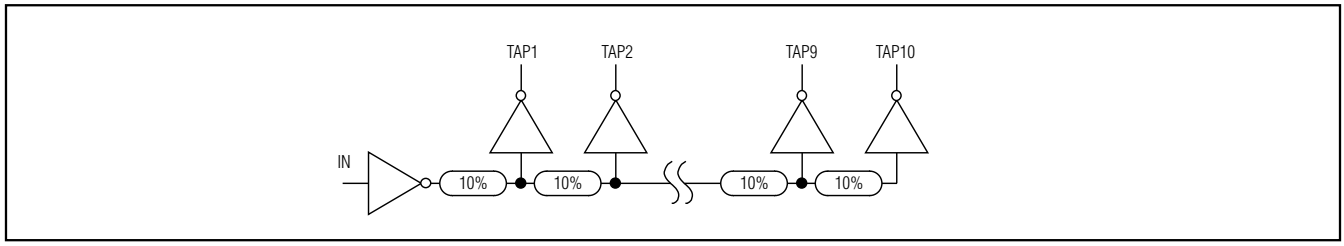


Figure 1. Logic Diagram

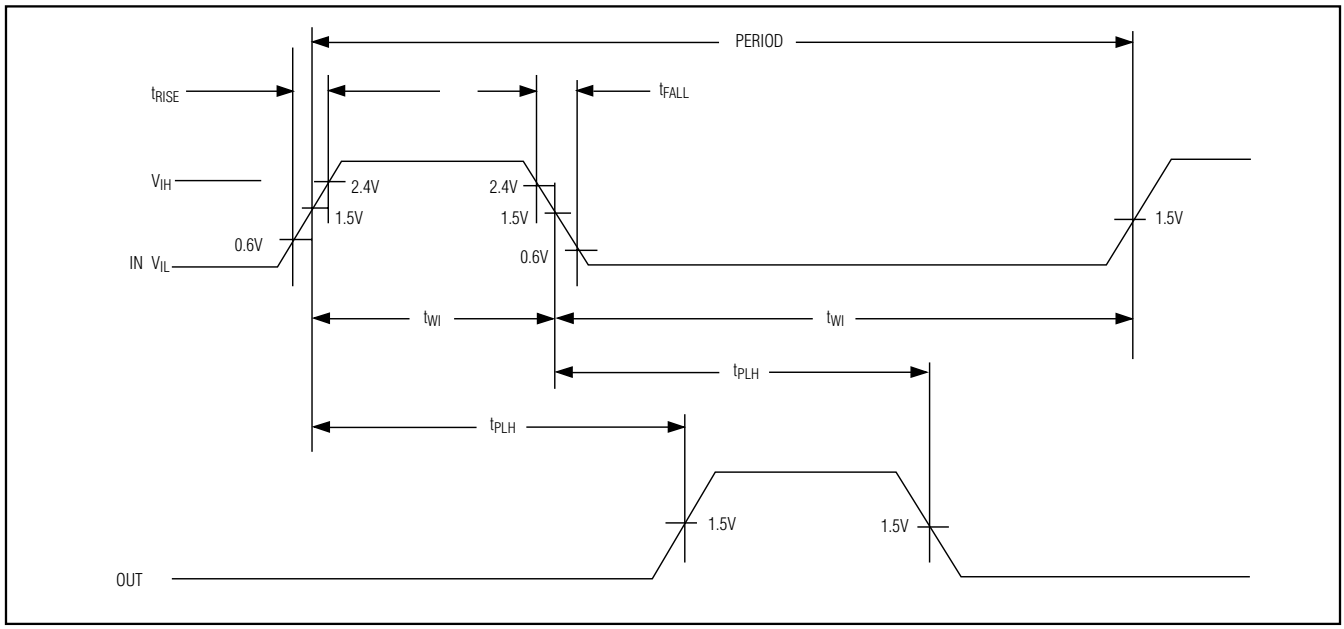


Figure 2. Timing Diagram: Silicon Delay Line

3V 10-Tap Silicon Delay Line

Terminology

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1110L. A precision pulse generator under software control produces the input waveform. Time delays are measured by a time interval counter (20ps resolution) connected

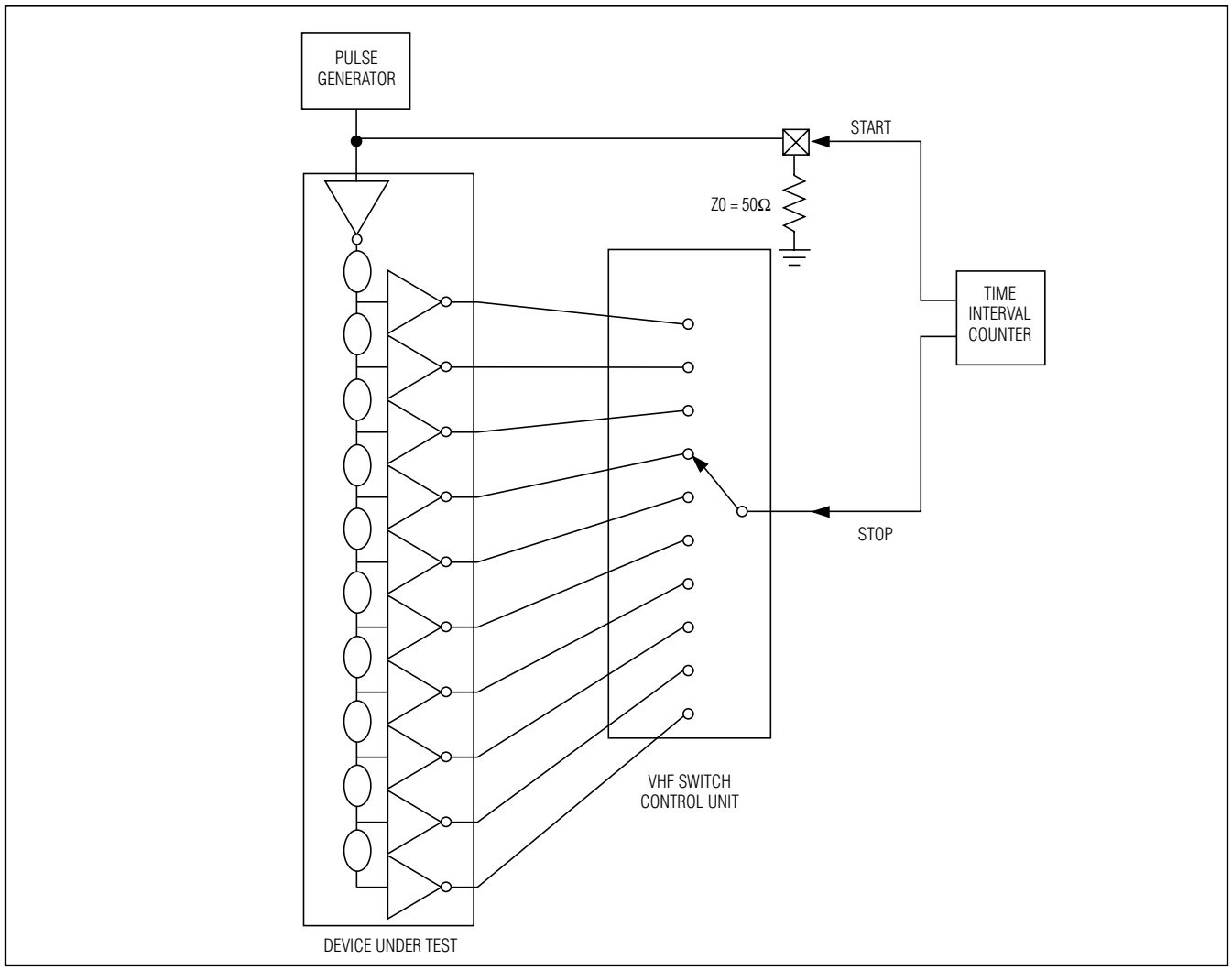


Figure 3. Test Circuit

between the input and each tap. Each tap is selected and connected to the counter by a VHF switch-control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE-488 bus.

Output

Each output is loaded with the equivalent of one 450Ω resistor in parallel with a 15pF capacitor. Delay is measured at the 1.5V level on the rising and falling edge.

Table 2. Test Conditions

INPUT	CONDITION
Ambient Temperature	+25°C ±3°C
Supply Voltage (V_{CC})	3.3V ±0.1V
Input Pulse	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance	50Ω max
Rise and Fall Time	2ns max
Pulse Width	500ns (1µs for - 500ns)
Period	1µs (2µs for - 500ns)

Note: *Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.*

Chip Information

TRANSISTOR COUNT: 6813

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.