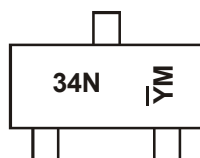
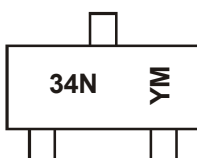


Marking Information



Chengdu A/T Site



Shanghai A/T Site

34N = Product Type Marking Code
 YM = Date Code Marking for SAT (Shanghai Assembly/Test site)
 YM = Date Code Marking for CAT (Chengdu Assembly/Test site)
 Y or $\bar{Y}$ = Year (ex: I = 2021)
 M = Month (ex: 9 = September)

Date Code Key

Year	2009		2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	W		I	J	K	L	M	N	O	P	R	S

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage (Notes 6, 7)			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = -40°C	I _D	4.6	A
		T _A = +25°C		4.2	
		T _A = +85°C		3.0	
Continuous Drain Current (Note 7) V _{GS} = 10V	Steady State	T _A = -40°C	I _D	6.2	A
		T _A = +25°C		5.8	
		T _A = +85°C		4.0	
Continuous Drain Current (Note 7) V _{GS} = 4.5V	Steady State	T _A = -40°C	I _D	5.2	A
		T _A = +25°C		4.8	
		T _A = +85°C		3.2	
Continuous Drain Current (Note 7) V _{GS} = 3V	Steady State	T _A = -40°C	I _D	2.2	A
		T _A = +25°C		2.0	
		T _A = +85°C		1.0	
Pulsed Drain Current			I _{DM}	30	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 6)	P_D	0.72	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$	$R_{\theta JA}$	173	$^\circ\text{C/W}$
Power Dissipation (Note 7)	P_D	1.4	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$	$R_{\theta JA}$	90	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Notes: 6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1.0	μA	$V_{DS} = 30V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance $T_J = -40^\circ\text{C}$ (Note 9)	$R_{DS(on)}$	—	23	27	—	$V_{GS} = 4.5V, I_D = 4.8A$
		—	57	74	—	$V_{GS} = 3V, I_D = 2A$
Static Drain-Source On-Resistance $T_J = +25^\circ\text{C}$	$R_{DS(on)}$	—	24	28	m Ω	$V_{GS} = 10V, I_D = 5.8A$
		—	33	42		$V_{GS} = 4.5V, I_D = 4.8A$
		—	63	82		$V_{GS} = 3V, I_D = 2A$
Static Drain-Source On-Resistance $T_J = +85^\circ\text{C}$ (Note 9)	$R_{DS(on)}$	—	71	95	m Ω	$V_{GS} = 3V, I_D = 2A$
Forward Transfer Admittance	$ Y_{fs} $	—	10	—	S	$V_{DS} = 5V, I_D = 5.8A$
Diode Forward Voltage	V_{SD}	—	0.75	1.0	V	$V_{GS} = 0V, I_S = 1A$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	498	—	pF	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	52	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	45	—	pF	
Gate Resistance	R_g	—	1.75	2.8	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 3V$)	Q_g	—	3.8	5.3	nC	$V_{GS} = 3V, V_{DS} = 15V, I_D = 1A$
Total Gate Charge ($V_{GS} = 4.5V$)	Q_g	—	5.3	7.5	nC	$V_{GS} = 10V/4.5V, V_{DS} = 15V, I_D = 5.8A$
Total Gate Charge ($V_{GS} = 10V$)	Q_g	—	11.3	16	nC	
Gate-Source Charge	Q_{gs}	—	1.4	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.1	—	nC	$V_{DD} = 15V, V_{GS} = 10V, R_L = 2.6\Omega, R_G = 3\Omega$
Turn-On Delay Time	$t_{D(on)}$	—	3.41	10	ns	
Turn-On Rise Time	t_r	—	6.18	13	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	13.92	28	ns	
Turn-Off Fall Time	t_f	—	2.84	10	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
 9. Guaranteed by design and 25°C data. Not subject to production testing
 10. Guaranteed by design. Not subject to production testing.

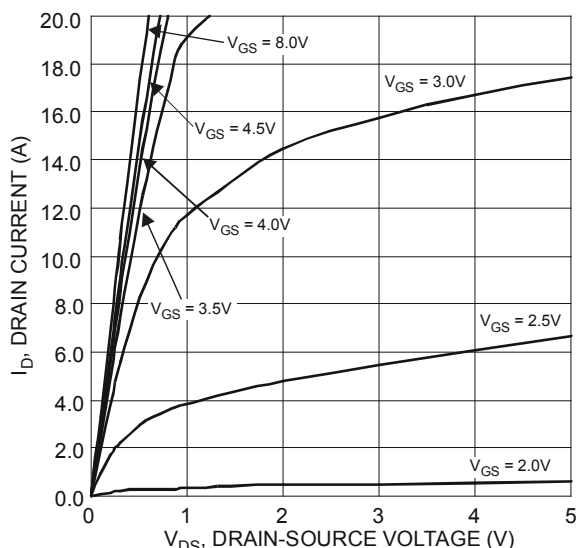


Figure 1 Typical Output Characteristics

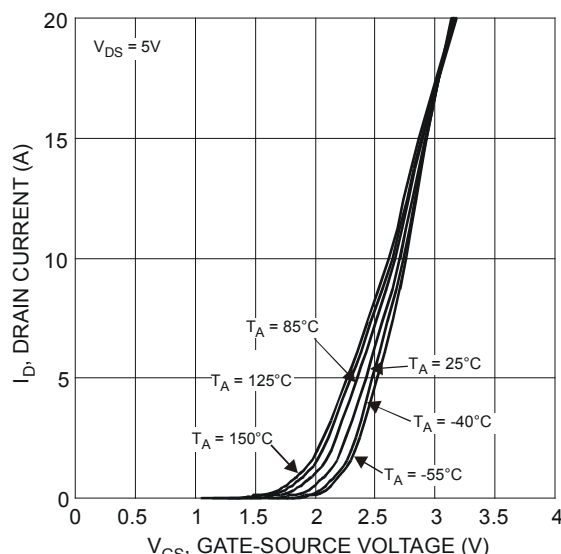
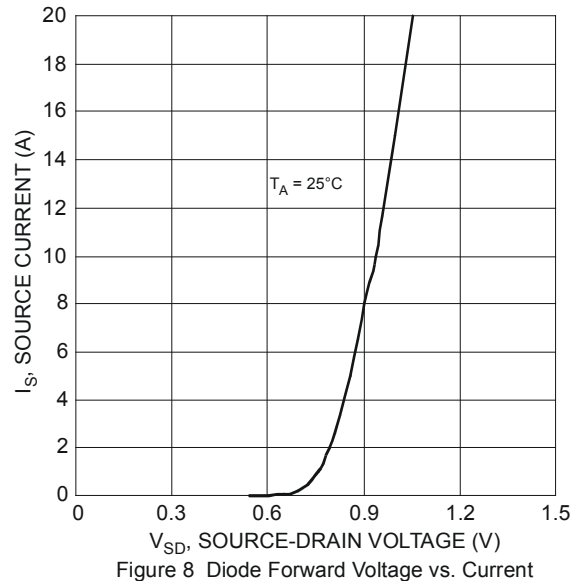
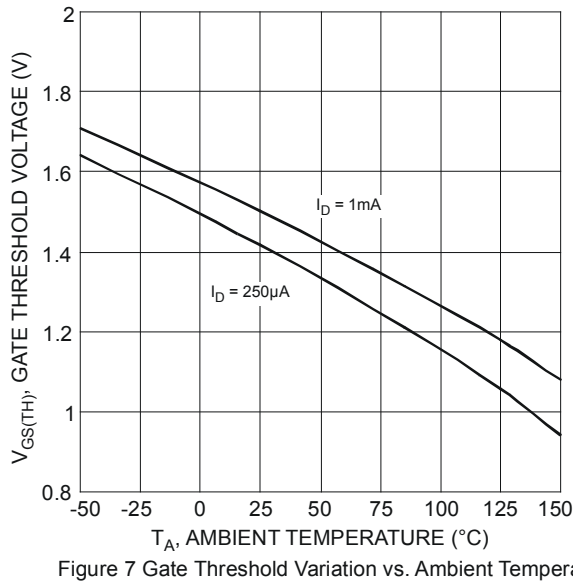
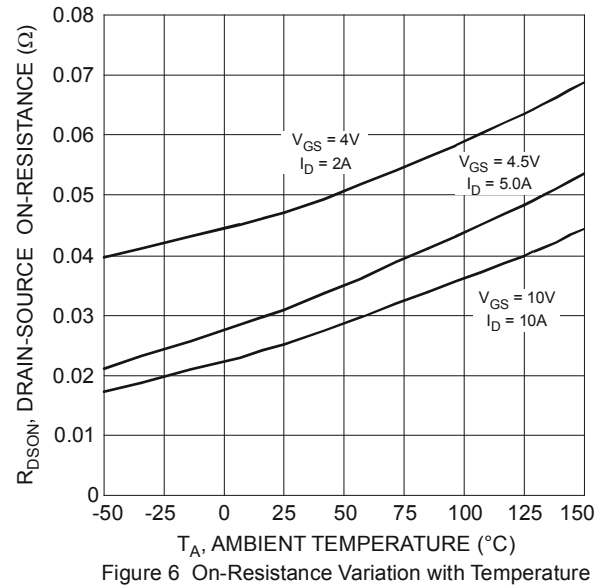
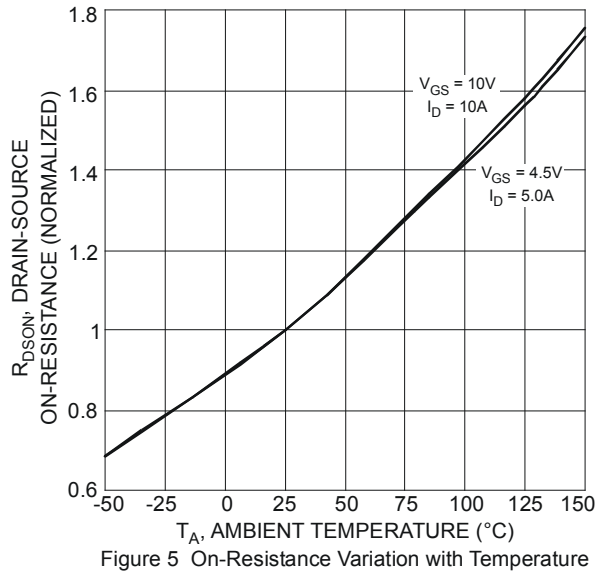
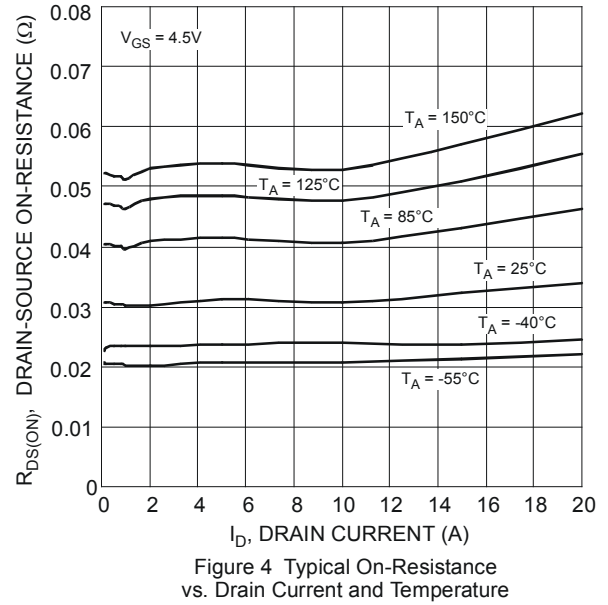
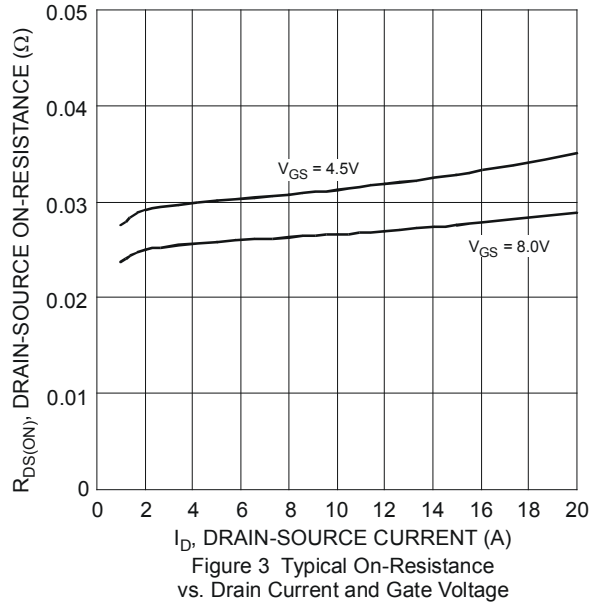
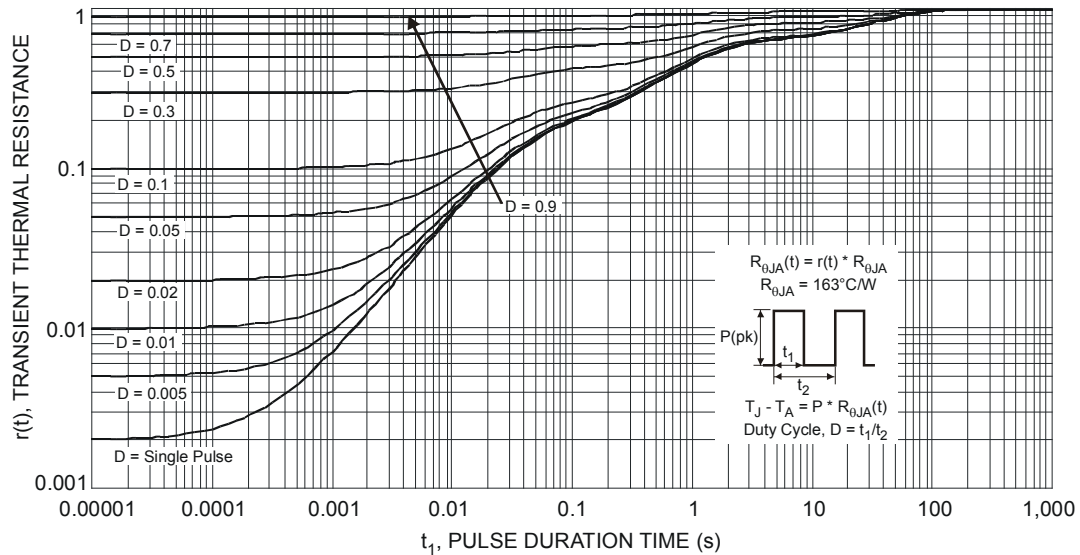
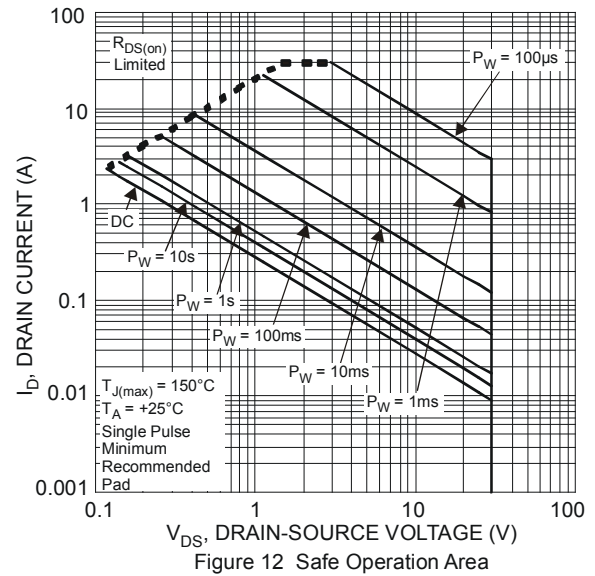
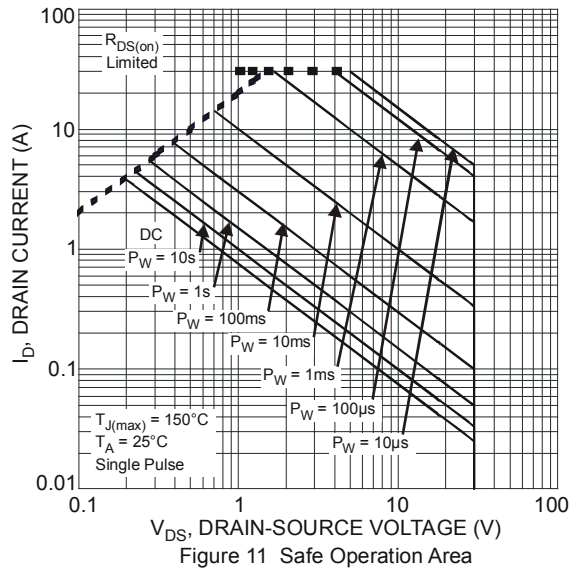
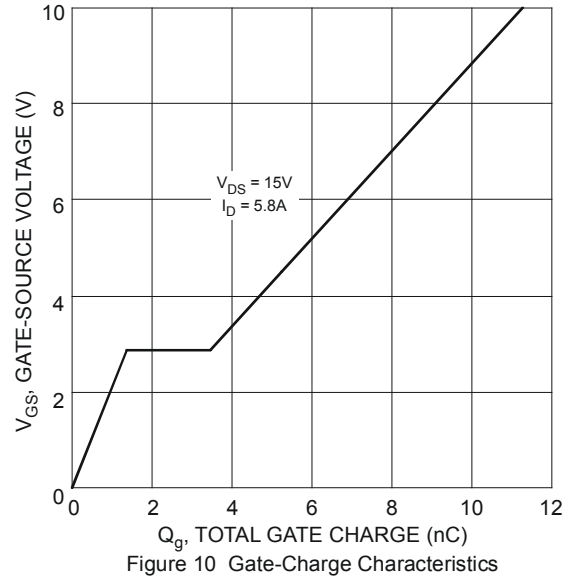
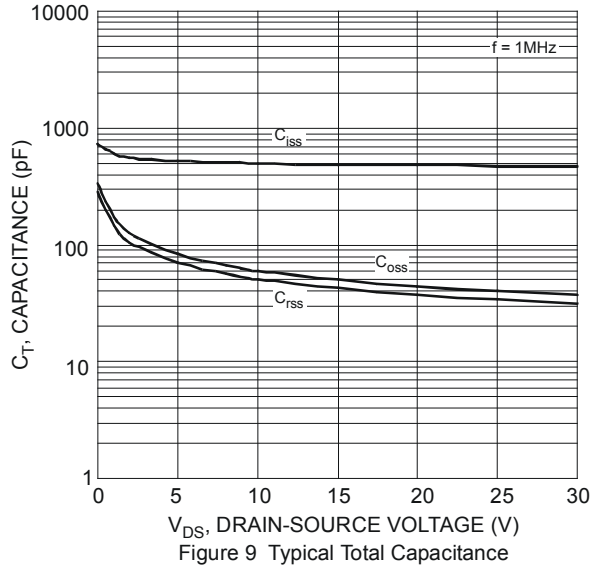
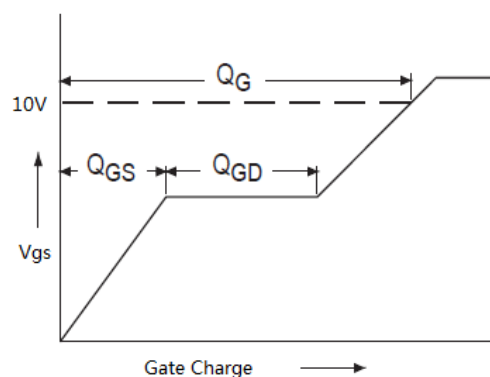
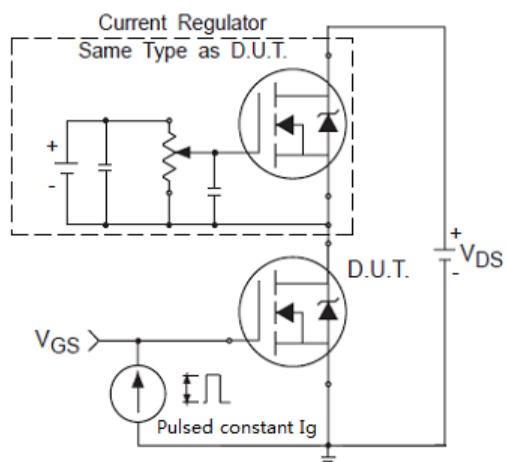


Figure 2 Typical Transfer Characteristics

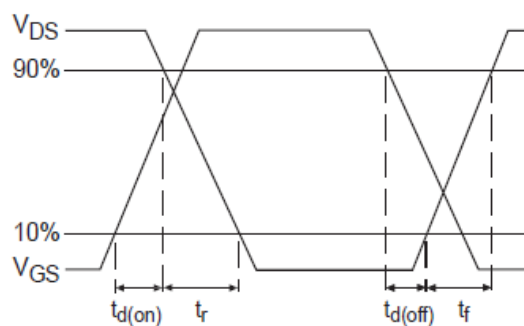
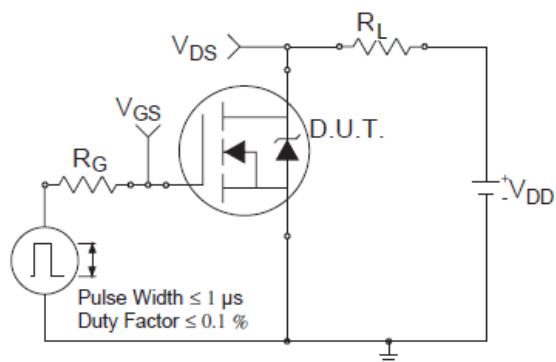




Gate Charge Test Circuit and Waveform



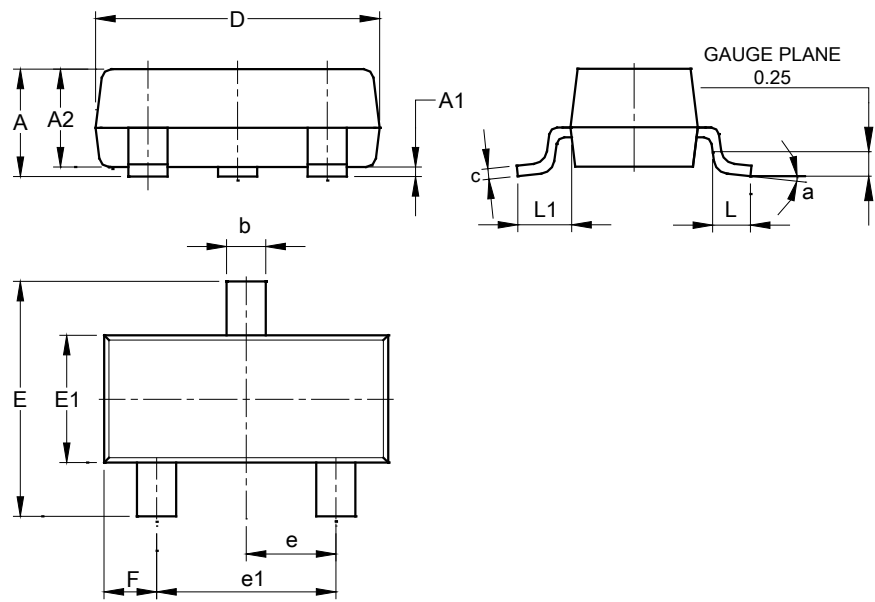
Switching Test Circuit and Waveform



Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT23 (Standard)

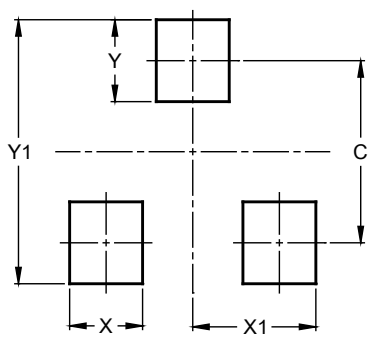


SOT23 (Standard)			
Dim	Min	Max	Typ
A	0.90	1.15	1.025
A1	0.00	0.10	0.05
A2	0.85	1.10	0.975
b	0.30	0.51	0.40
c	0.080	0.202	0.11
D	2.80	3.00	2.90
E	2.25	2.55	2.40
E1	1.20	1.40	1.30
e	0.89	1.03	0.915
e1	1.78	2.05	1.83
F	0.40	0.60	0.535
L1	0.45	0.61	0.55
L	0.25	0.55	0.40
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT23 (Standard)



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9

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