Maximum Ratings Q1 N-CHANNEL (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 7) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	450 350	mA
	t<5s	T_A = +25°C T_A = +70°C	I_D	520 410	mA
Continuous Drain Current (Note 7) V_{GS} = 1.8V	Steady State	T_A = +25°C T_A = +70°C	I_D	330 260	mA
	t<5s	T_A = +25°C T_A = +70°C	I_D	390 310	mA
Maximum Continuous Body Diode Forward Current (Note 7)			I_S	440	mA
Pulsed Drain Current (Note 8)			I_{DM}	800	mA

Maximum Ratings Q2 P-CHANNEL (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-310 -240	mA
	t<5s	T_A = +25°C T_A = +70°C	I_D	-360 -280	mA
Continuous Drain Current (Note 5) V_{GS} = -1.8V	Steady State	T_A = +25°C T_A = +70°C	I_D	-240 -190	mA
	t<5s	T_A = +25°C T_A = +70°C	I_D	-280 -220	mA
Maximum Continuous Body Diode Forward Current (Note 7)			I_S	-440	mA
Pulsed Drain Current (Note 8)			I_{DM}	-800	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 7)		P_D	350	mW
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	360	°C/W
	t<5s		270	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 7. Device mounted on FR-4 PCB, with minimum recommended pad layout.
8. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.

Electrical Characteristics Q1 N-CHANNEL (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	-	-	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DSS}	-	-	100	nA	V_{DS} = 16V, V_{GS} = 0V
		-	-	50		V_{DS} = 5V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(th)}$	0.4	-	1.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	0.60	0.99	Ω	V_{GS} = 4.5V, I_D = 100mA
		-	0.75	1.2		V_{GS} = 2.5V, I_D = 50mA
		-	0.90	1.8		V_{GS} = 1.8V, I_D = 20mA
		-	1.2	2.4		V_{GS} = 1.5V, I_D = 10mA
		-	2.0	-		V_{GS} = 1.2V, I_D = 1mA
Forward Transfer Admittance	$\|Y_{fs}\|$	180	850	-	mS	V_{DS} = 5V, I_D = 125mA
Diode Forward Voltage	V_{SD}	-	0.6	1.0	V	V_{GS} = 0V, I_S = 10mA
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	-	27.6	-	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	4.0	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	2.8	-	pF	
Gate Resistance	R_G	-	113	-	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge	Q_g	-	0.5	-	nC	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 250mA
Gate-Source Charge	Q_{gs}	-	0.07	-	nC	
Gate-Drain Charge	Q_{gd}	-	0.07	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	4.0	-	ns	V_{DD} = 15V, V_{GS} = 4.5V, R_L = 47Ω, R_G = 2Ω, I_D = 200mA
Turn-On Rise Time	t_r	-	3.3	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	19.0	-	ns	
Turn-Off Fall Time	t_f	-	6.4	-	ns	

Electrical Characteristics Q2 P-CHANNEL (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	-	-	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DSS}	-	-	100	nA	V_{DS} = -16V, V_{GS} = 0V
		-	-	50		V_{DS} = -5V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	1.2	1.9	Ω	V_{GS} = -4.5V, I_D = -100mA
		-	1.5	2.4		V_{GS} = -2.5V, I_D = -50mA
		-	2.1	3.4		V_{GS} = -1.8V, I_D = -20mA
		-	2.5	5		V_{GS} = -1.5V, I_D = -10mA
		-	4.0	-		V_{GS} = -1.2V, I_D = -1mA
Forward Transfer Admittance	$\|Y_{fs}\|$	100	450	-	mS	V_{DS} = -5V, I_D = -125mA
Diode Forward Voltage	V_{SD}	-	-0.6	-1.0	V	V_{GS} = 0V, I_S = -10mA
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	-	28.7	-	pF	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	4.2	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	2.9	-	pF	
Gate Resistance	R_G	-	399	-	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge	Q_g	-	0.4	-	nC	V_{GS} = -4.5V, V_{DS} =- 10V, I_D = -250mA
Gate-Source Charge	Q_{gs}	-	0.08	-	nC	
Gate-Drain Charge	Q_{gd}	-	0.06	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	5.8	-	ns	V_{DD} = -15V, V_{GS} = -4.5V, R_G = 2Ω, I_D = -200mA
Turn-On Rise Time	t_r	-	5.7	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	31.1	-	ns	
Turn-Off Fall Time	t_f	-	16.4	-	ns	

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

Q1 N-CHANNEL

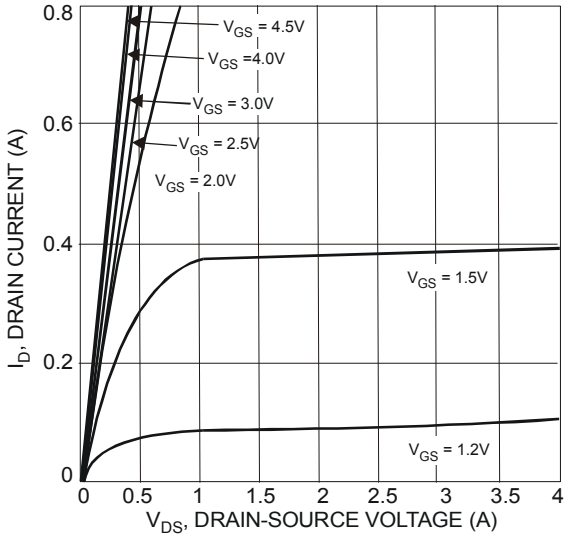


Fig. 1 Typical Output Characteristics

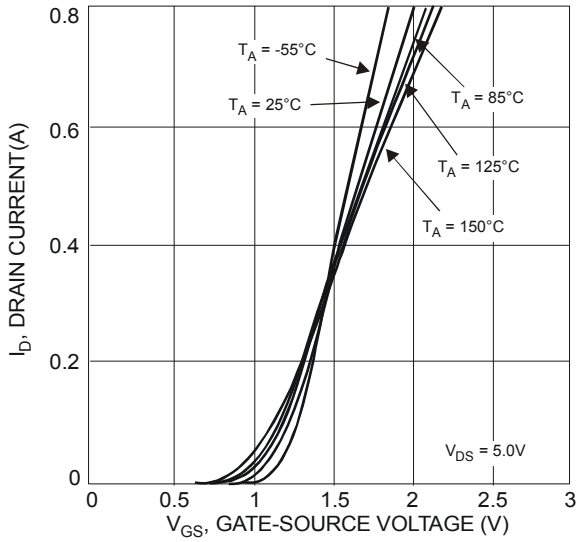


Fig. 2 Typical Transfer Characteristics

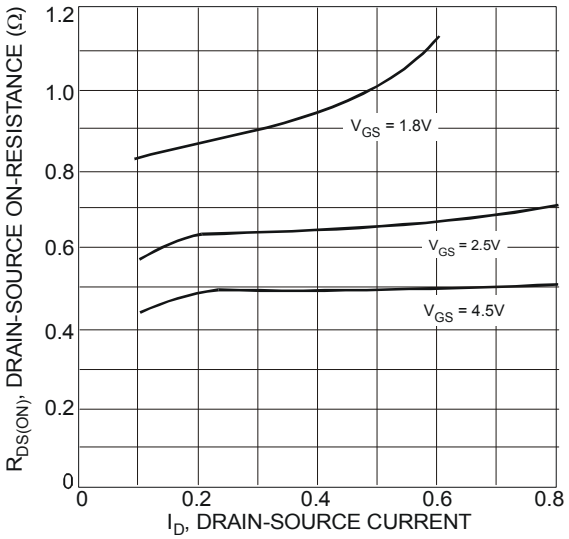


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

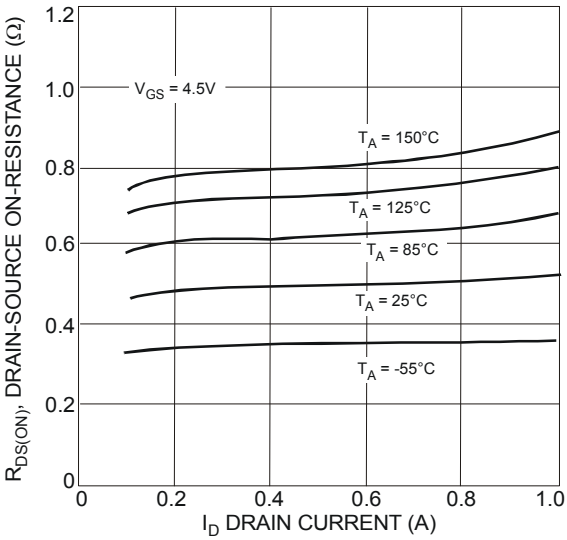


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

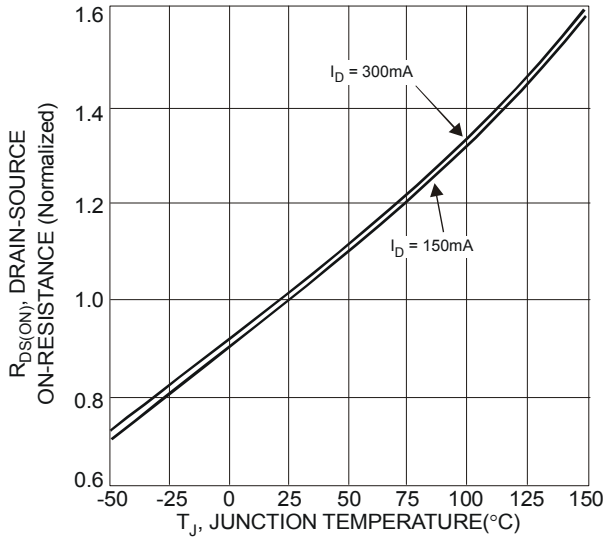


Fig. 5 On-Resistance Variation with Temperature

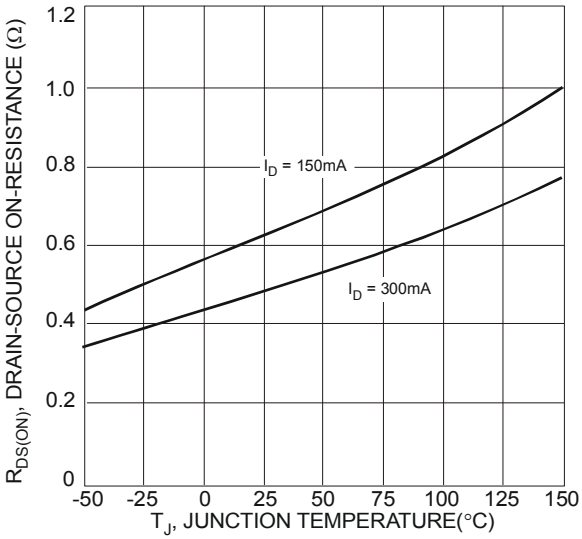


Fig. 6 On-Resistance Variation with Temperature

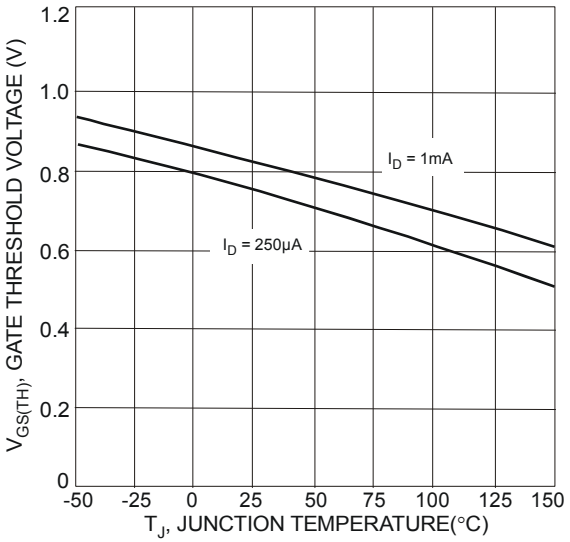


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

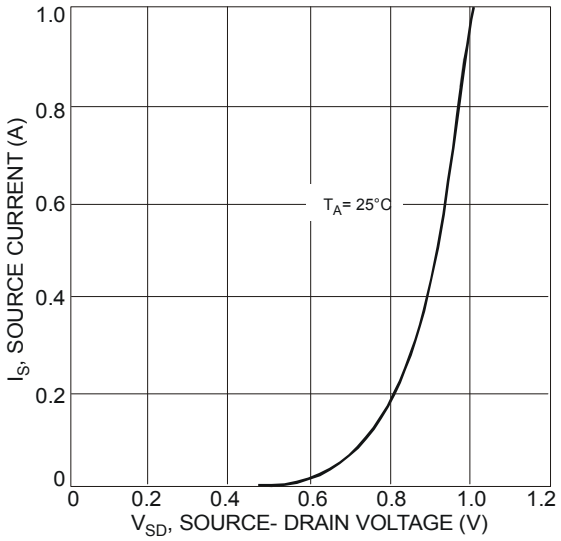


Fig. 8 Diodes Forward Voltage vs. Current

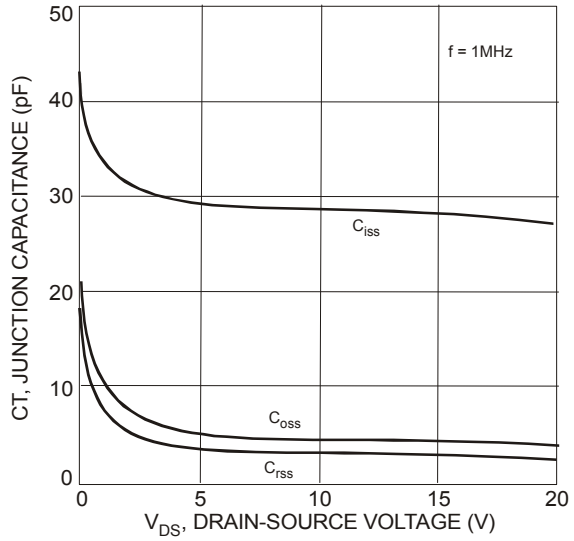


Fig. 9 Typical Junction Capacitance

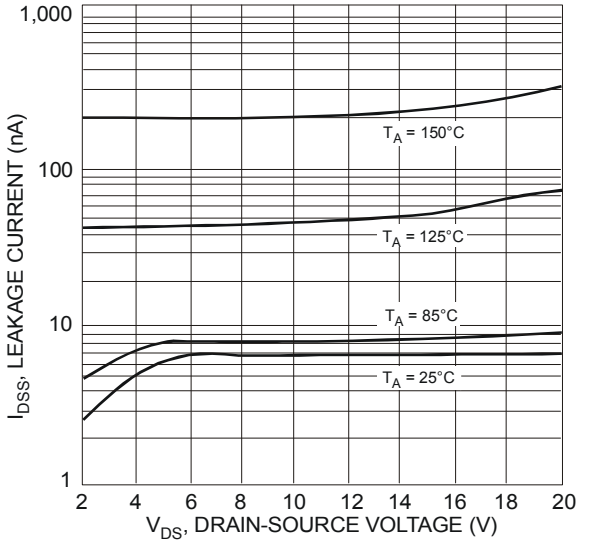


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

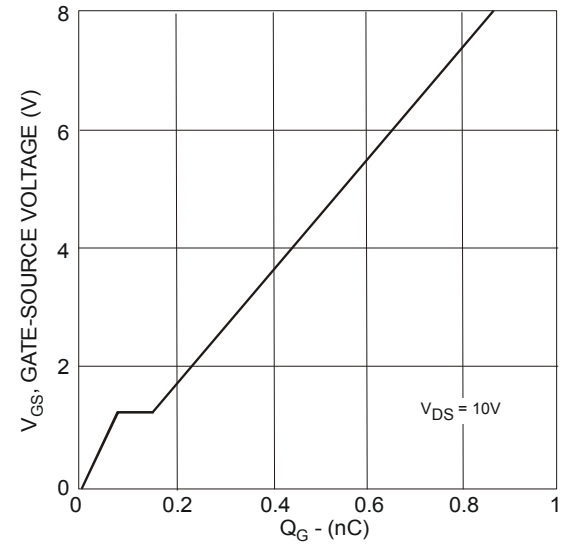


Fig. 11 Gate Charge Characteristics

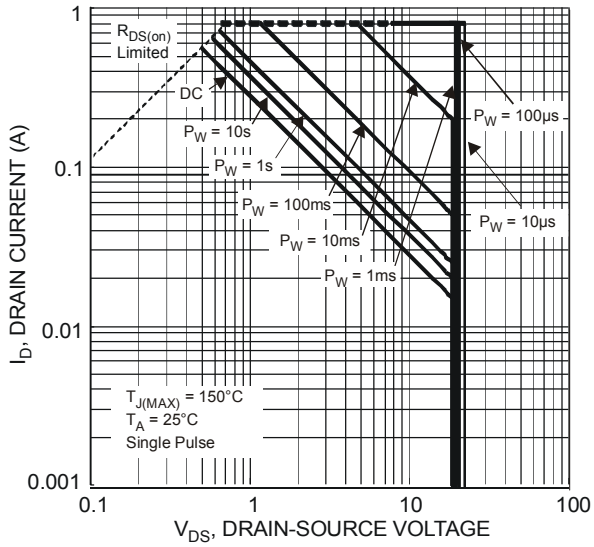


Fig. 12 SOA, Safe Operation Area

Q2 P-CHANNEL

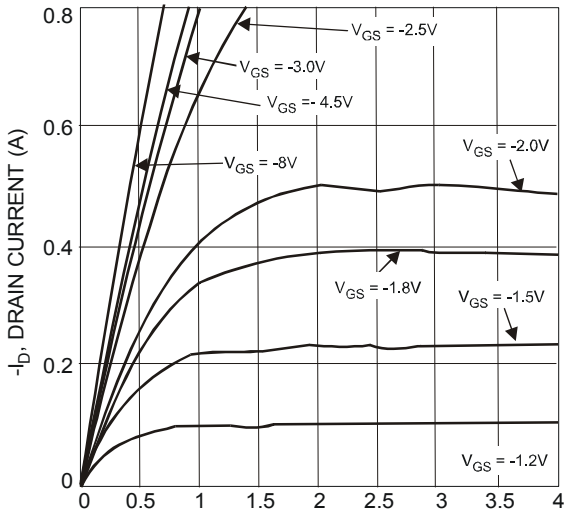


Fig. 13 Typical Output Characteristics

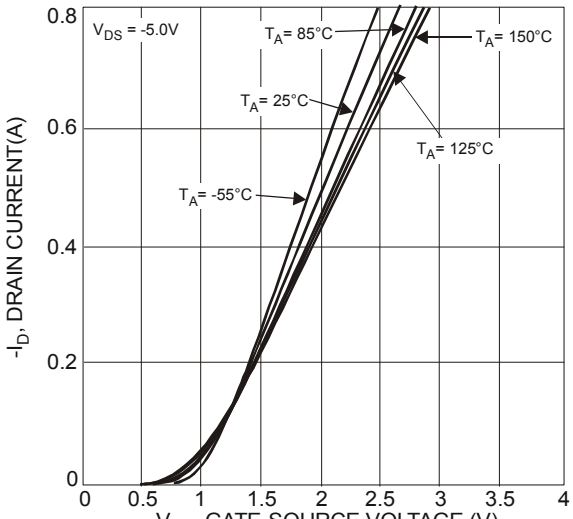


Fig. 14 Typical Transfer Characteristics

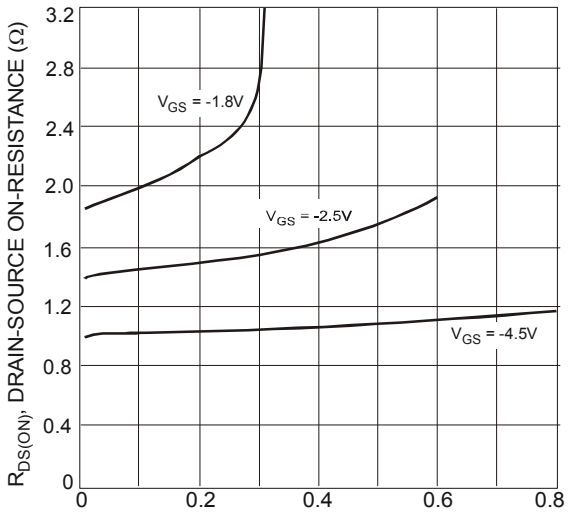


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

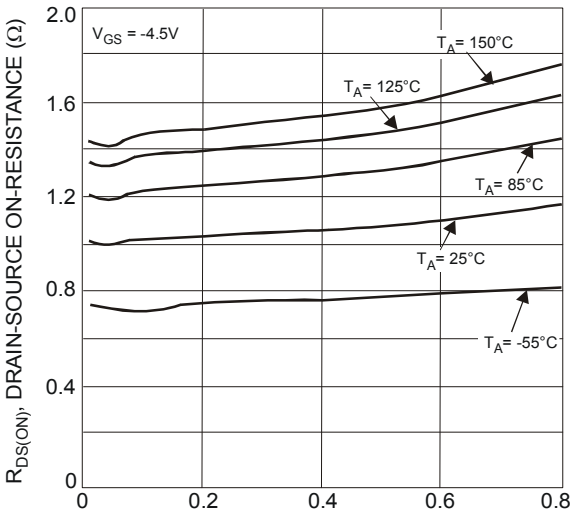


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

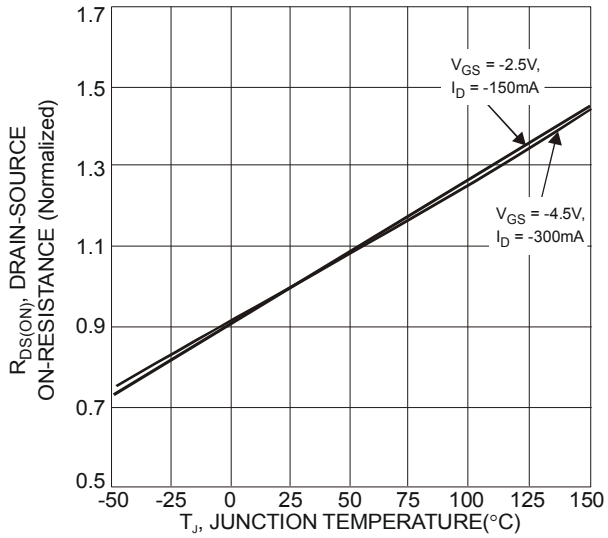


Fig. 17 On-Resistance Variation with Temperature

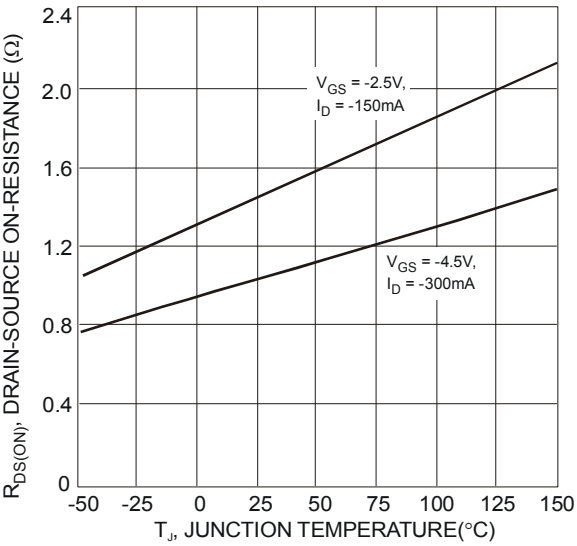


Fig. 18 On-Resistance Variation with Temperature

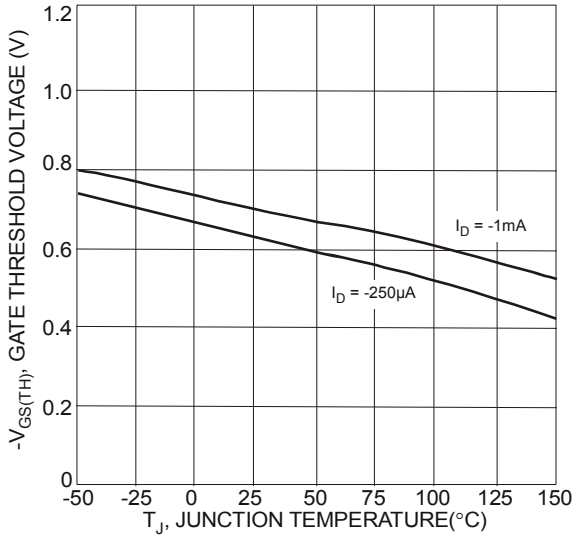


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

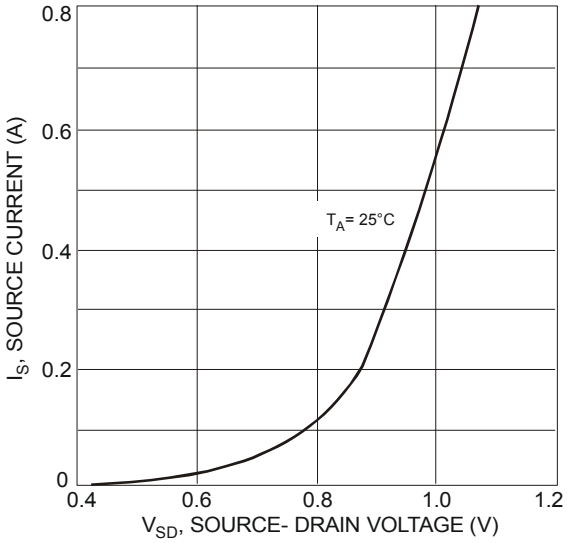


Fig. 20 Diodes Forward Voltage vs. Current

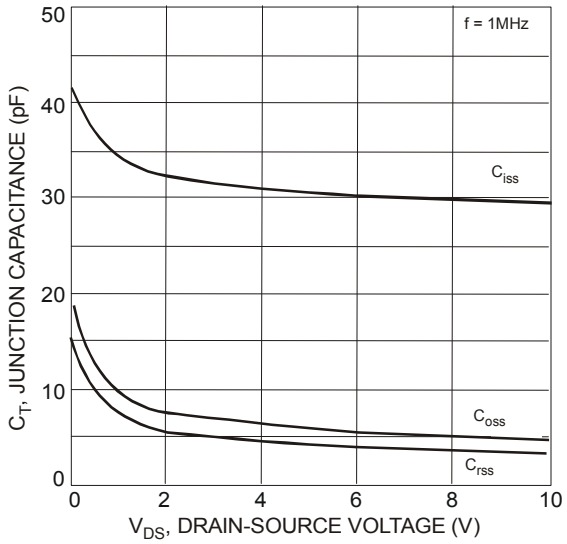


Fig. 21 Typical Junction Capacitance

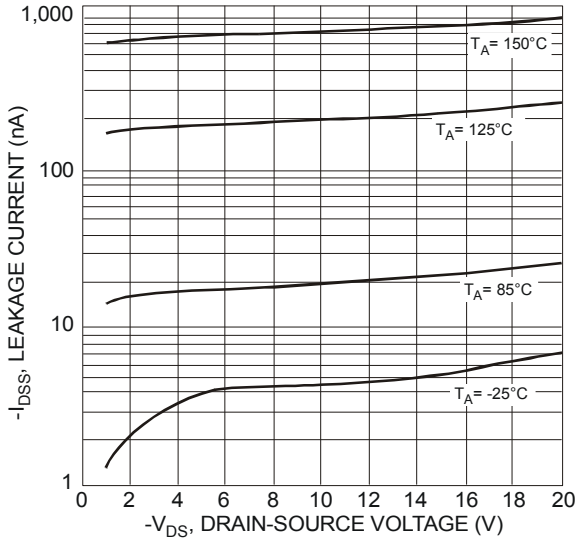


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

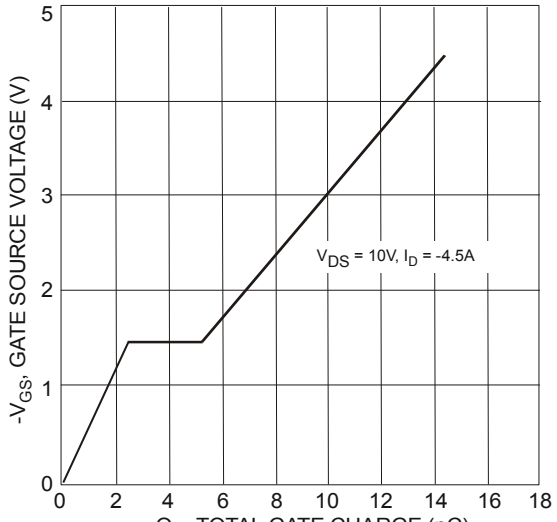


Fig. 23 Gate Charge Characteristics

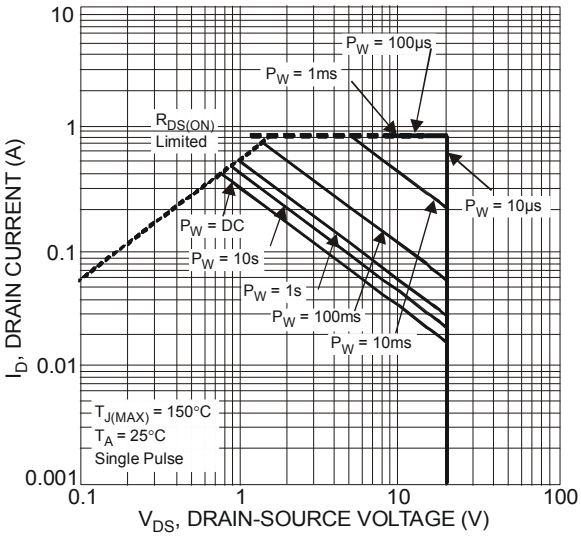


Fig. 24 SOA, Safe Operation Area

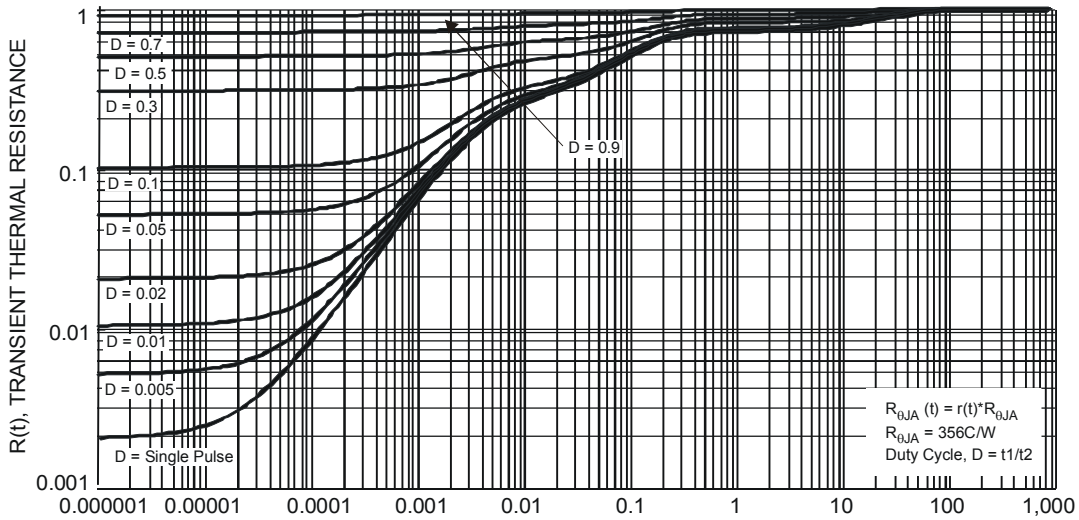
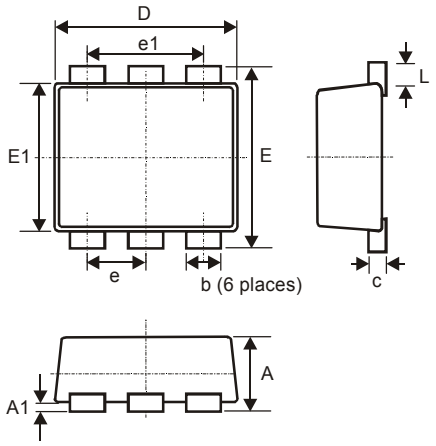


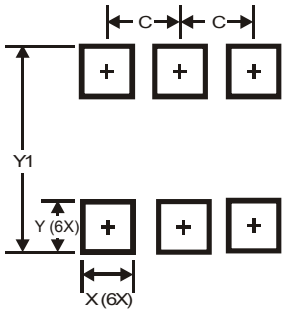
Fig. 25 Transient Thermal Resistance

Package Outline Dimensions



SOT963			
Dim	**Min**	**Max**	**Typ**
A	0.40	0.50	0.45
A1	0	0.05	-
c	0.120	0.180	0.150
D	0.95	1.05	1.00
E	0.95	1.05	1.00
E1	0.75	0.85	0.80
L	0.05	0.15	0.10
b	0.10	0.20	0.15
e	0.35 Typ		
e1	0.70 Typ		
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.350
X	0.200
Y	0.200
Y1	1.100

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