

ORDERING INFORMATION		
Temp Range	Package	Part Number
DG417B, DG418B		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG417BDJ DG417BDJ-E3
		DG418BDJ DG418BDJ-E3
	8-Pin Narrow SOIC	DG417BDY DG417BDY-E3 DG417BDY-T1 DG417BDY-T1-E3
		DG418BDY DG418BDY-E3 DG418BDY-T1 DG418BDY-T1-E3
	8-Pin MSOP	DG417BDQ-T1-E3
		DG418BDQ-T1-E3
DG419B		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG419BDJ DG419BDJ-E3
	8-Pin Narrow SOIC	DG419BDY DG419BDY-E3 DG419BDY-T1 DG419BDY-T1-E3
	8-Pin MSOP	DG419BDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
V-		- 20	V
V+		20	
GND		25	
V _L		(GND - 0.3) to (V+) + 0.3	
Digital Inputs ^a , V _S , V _D		(V-) - 2 V to (V+) + 2 or 30 mA, whichever occurs first	
Current, (Any Terminal) Continuous		30	mA
Current (S or D) Pulsed at 1 ms, 10 % Duty Cycle		100	
Storage Temperature		- 65 to 150	°C
Power Dissipation (Package) ^b	8-Pin Plastic MiniDIP ^c	400	mW
	8-Pin Narrow SOIC ^c	400	
	8-Pin MSOP ^d	400	
	8-Pin CerDIP ^e	600	

Notes:

a. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 5.3 mW/°C above 75 °C.

d. Derate 4 mW/°C above 70 °C.

e. Derate 8 mW/°C above 75 °C.

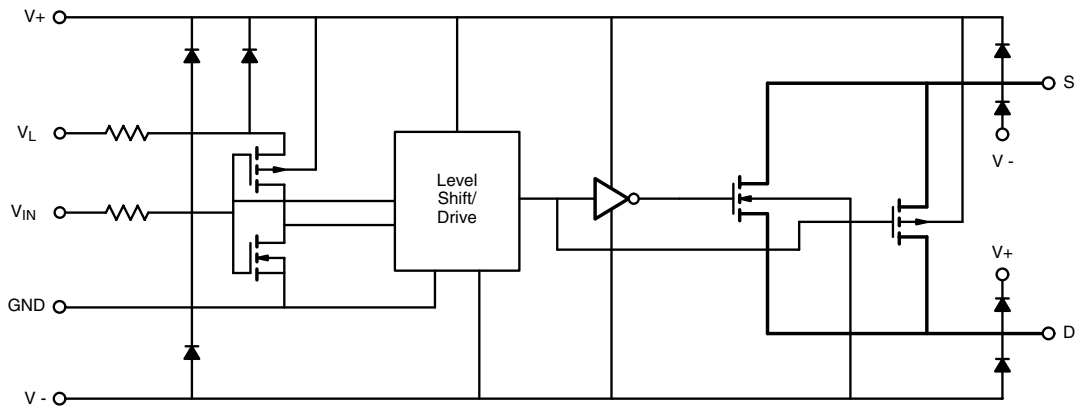
SCHEMATIC DIAGRAM Typical Channel


Figure 1.

SPECIFICATIONS ^a											
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
		Min. ^d	Max. ^d			Min. ^d	Max. ^d				
Analog Switch											
Analog Signal Range ^e	V _{ANALOG}			Full		- 15	15	- 15	15	V	
Drain-Source On-Resistance	R _{DS(on)}	I _S = - 10 mA, V _D = ± 12.5 V V ₊ = 13.5 V, V ₋ = - 13.5 V		Room Full	15		25 34		25 29	Ω	
Switch Off Leakage Current	I _{S(off)}	V ₊ = 16.5, V ₋ = - 16.5 V V _D = ± 15.5 V, V _S = ± 15.5 V		Room Full	- 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA	
	DG417B DG418B			Room Full	- 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5		
	DG419B			Room Full	- 0.1	- 0.75 - 60	0.75 60	- 0.75 - 12	0.75 12		
Channel On Leakage Current	I _{D(on)}	V ₊ = 16.5 V, V ₋ = - 16.5 V V _S = V _D = ± 15.5 V		DG417B DG418B	Room Full	- 0.4	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10	
				DG419B	Room Full	- 0.4	- 0.75 - 60	0.75 60	- 0.75 - 12	0.75 12	
Digital Control											
Input Current, V _{IN} Low	I _{IL}			Full		- 0.5	0.5	- 0.5	0.5	μA	
Input Current, V _{IN} High	I _{IH}			Full		- 0.5	0.5	- 0.5	0.5		
Dynamic Characteristics											
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = ± 10 V, See Switching Time Test Circuit		DG417B DG418B	Room Full	62		89 106		89 99	ns
Turn-Off Time	t _{OFF}			DG417B DG418B	Room Full	53		80 88		80 86	
Transition Time	t _{TRANS}	R _L = 300 Ω, C _L = 35 pF V _{S1} = ± 10 V, V _{S2} = ± 10 V		DG419B	Room Full	60		87 96		87 93	
Break-Before-Make Time Delay	t _D	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = ± 10 V		DG419B	Room	16	3		3		
Charge Injection	Q	C _L = 10 nF V _{gen} = 0 V, R _{gen} = 0 Ω		Room	38						pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz		Room	- 82						dB
Channel-to-Channel Crosstalk ^e	X _{TALK}			DG419B	Room	- 88					

SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics										
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V		Room	12					pF
Drain Off Capacitance ^e	C _{D(off)}		DG417B DG418B	Room	12					
Channel On Capacitance ^e	C _{D(on)}	f = 1 MHz, V _S = 0 V	DG417B DG418B	Room	50					
			DG419B	Room	57					
Power Supplies										
Positive Supply Current	I ₊	V ₊ = 16.5 V, V ₋ = - 16.5 V V _{IN} = 0 or 5 V		Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I ₋			Room Full	- 0.001	- 1 - 5		- 1 - 5		
Logic Supply Current	I _L			Room Full	0.001		1 5		1 5	
Ground Current	I _{GND}			Room Full	- 0.001	- 1 - 5		- 1 - 5		

SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 12 V, V ₋ = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}	I _S = - 10 mA, V _D = 3.8 V V ₊ = 10.8 V		Room Full	26		35 52		35 45	Ω
Dynamic Characteristics										
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = 8 V, See Switching Time Test Circuit		Room Full	100		125 155		125 143	ns
Turn-Off Time	t _{OFF}			Room Full	38		66 73		66 69	
Break-Before-Make Time Delay	t _D	R _L = 300 Ω, C _L = 35 pF	DG419B	Room	62	25		25		
Transition Time	t _{TRANS}	R _L = 300 Ω, C _L = 35 pF V _{S1} = 0 V, 8 V, V _{S2} = 8 V, 0 V		Room Full	95		119 153		119 141	
Charge Injection	Q	C _L = 10 nF, V _{gen} = 0 V, R _{gen} = 0 Ω		Room	18					pC
Power Supplies										
Positive Supply Current	I ₊	V ₊ = 13.2 V, V _L = 5.25 V V _{IN} = 0 or 5 V		Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I ₋			Room	- 0.001	- 1 - 5		- 1 - 5		
Logic Supply Current	I _L			Room	0.001		1 5		1 5	
Ground Current	I _{GND}			Room	- 0.001	- 1 - 5		- 1 - 5		

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, full = as determined by the operating temperature suffix.

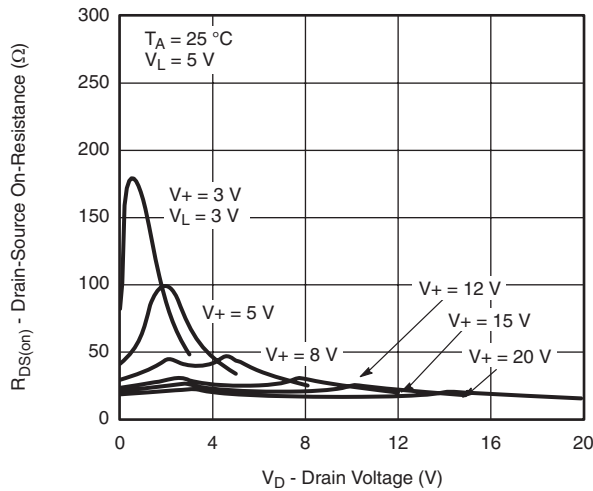
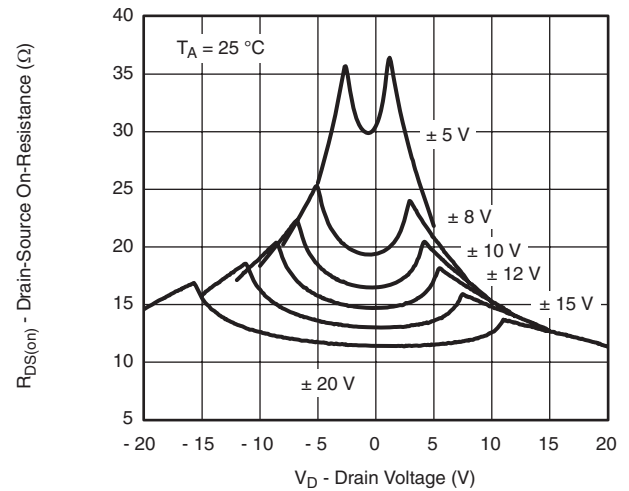
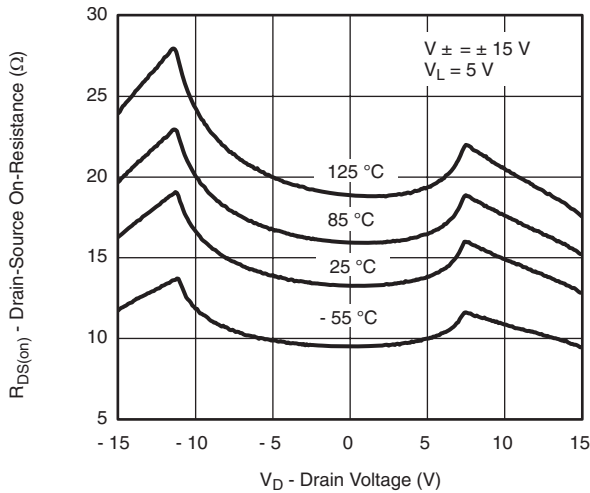
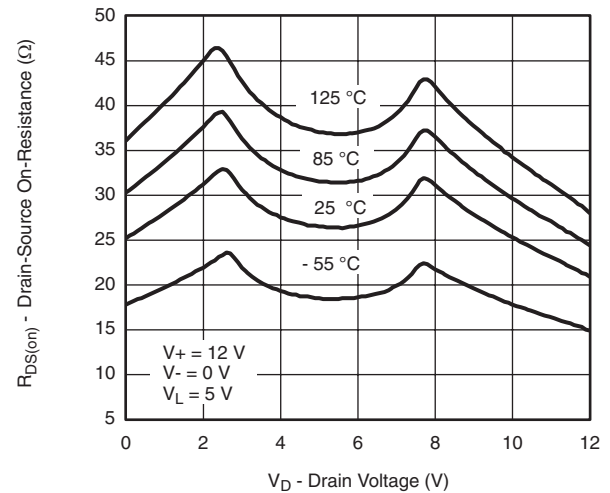
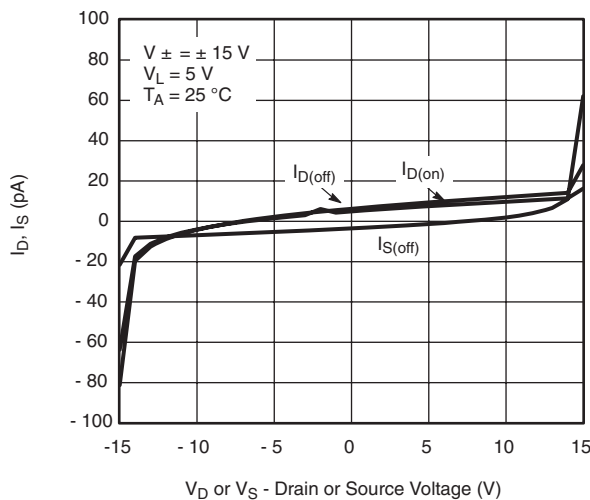
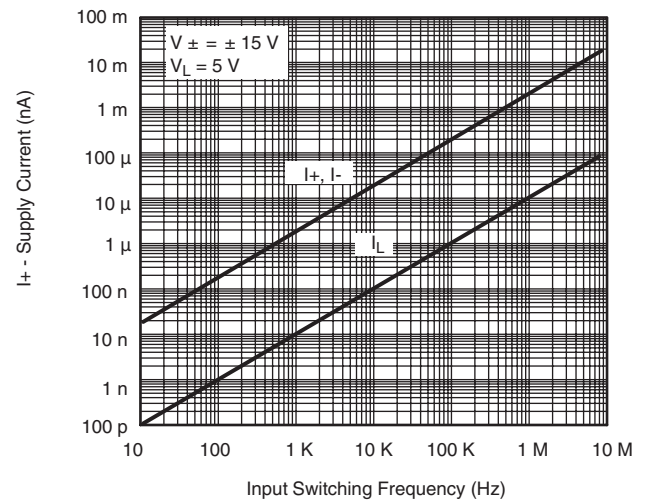
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

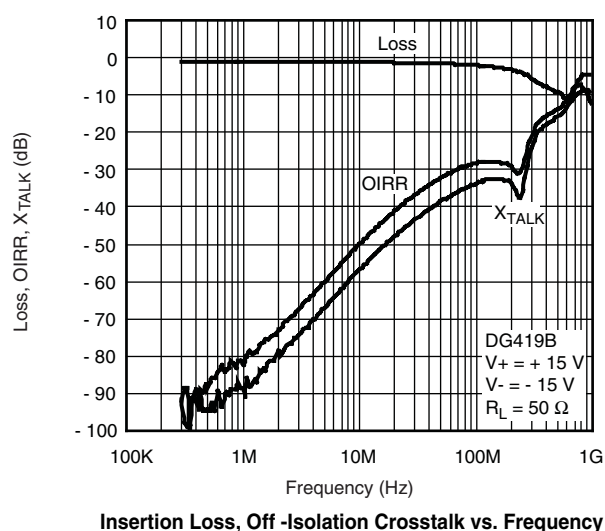
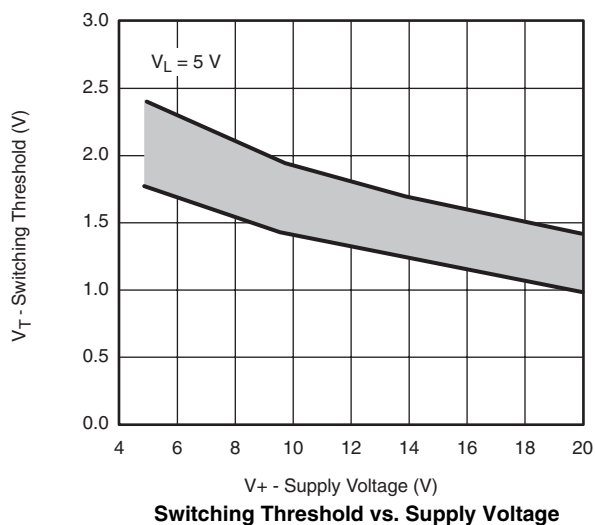
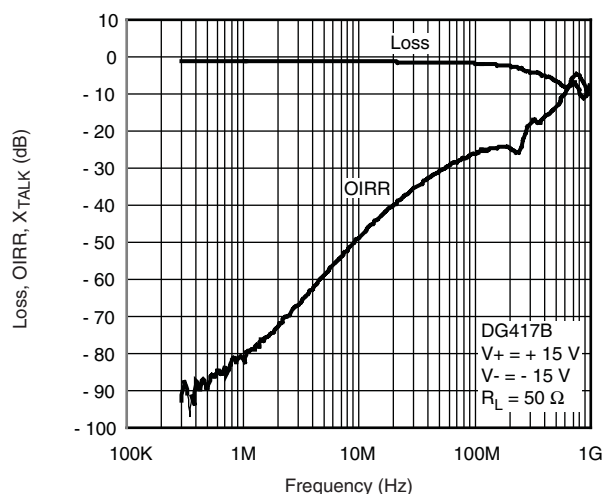
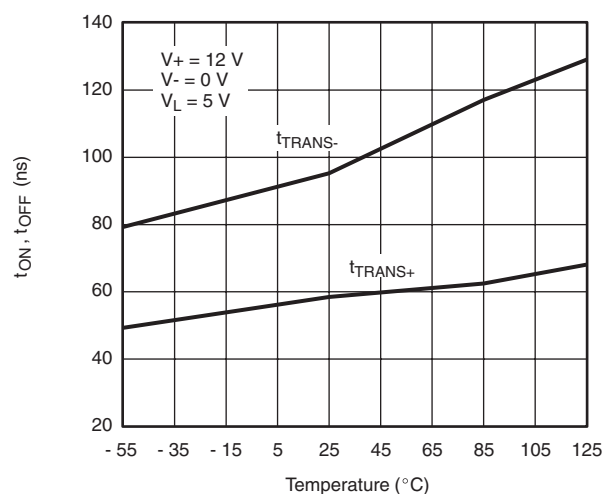
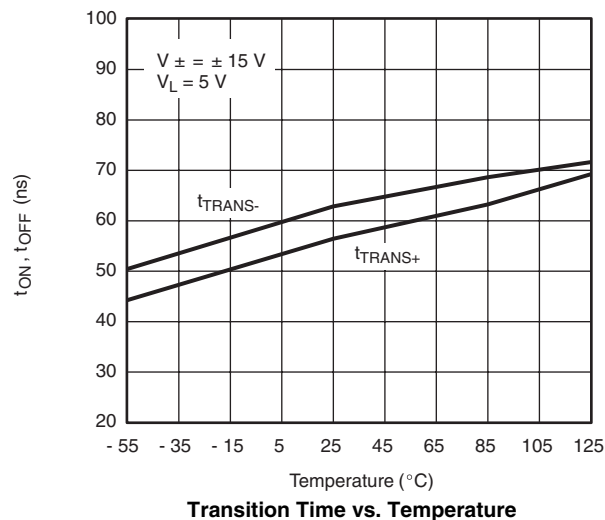
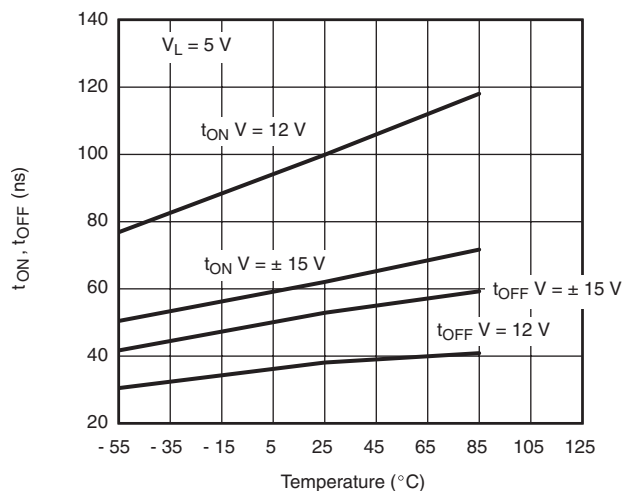
e. Guaranteed by design, not subject to production test.

f. V_{IN} = input voltage to perform proper function.

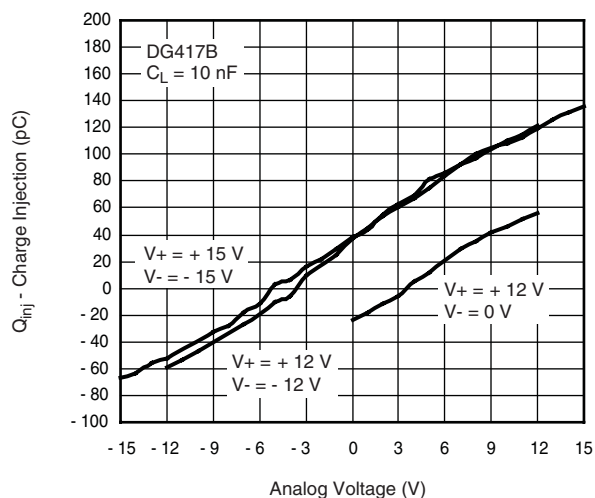
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted

On-Resistance vs. V_D and Unipolar Power Supply Voltage

On-Resistance vs. V_D and Dual Supply Voltage

On-Resistance vs. V_D and Temperature

On-Resistance vs. V_D and Temperature

Leakage vs. Analog Voltage

Supply Current vs. Input Switching Frequency

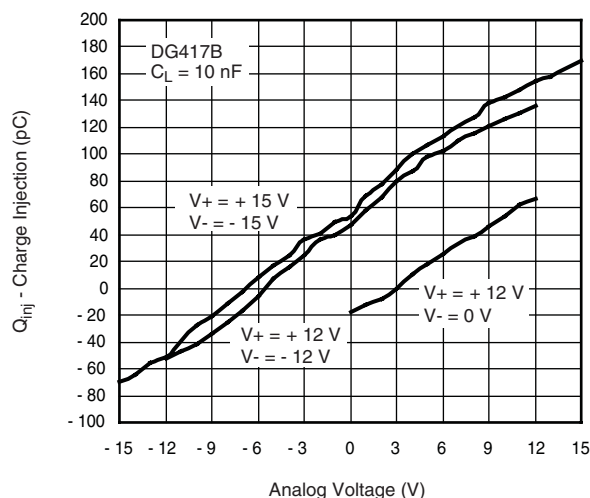
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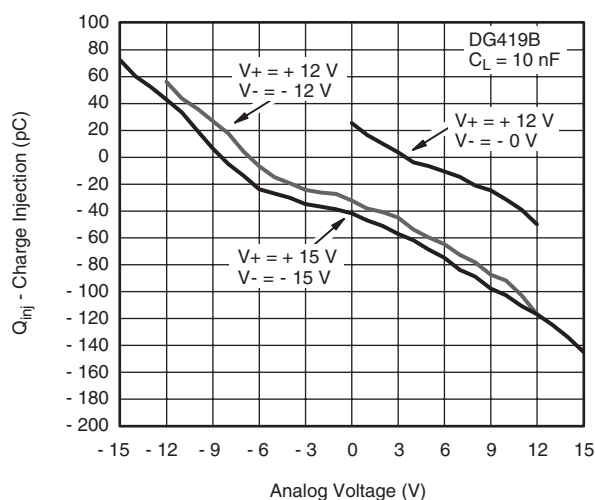
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



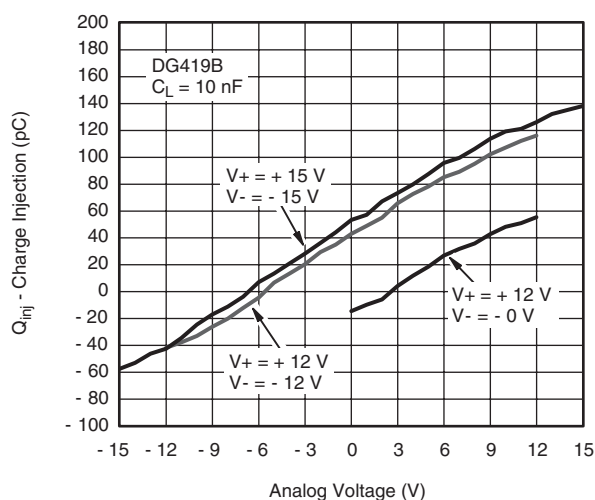
Charge Injection vs. Analog Voltage
(Measured at drain pin)



Charge Injection vs. Analog Voltage
(Measured at source pin)



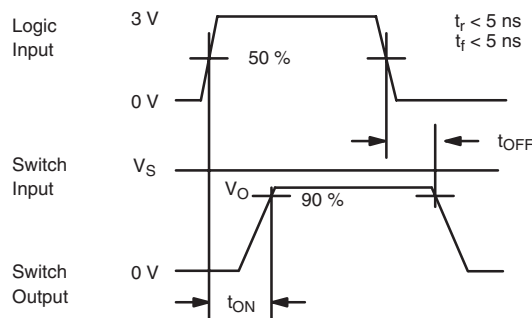
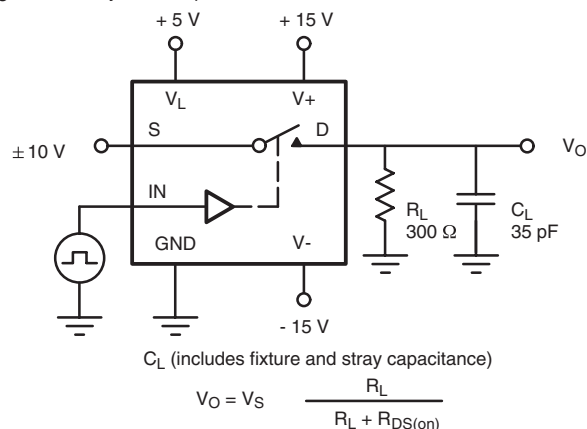
Charge Injection vs. Analog Voltage
(Measured at drain pin)



Charge Injection vs. Analog Voltage
(Measured at source pin)

TEST CIRCUITS

V_O is the steady state output with the switch on.



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417B/418B)

TEST CIRCUITS

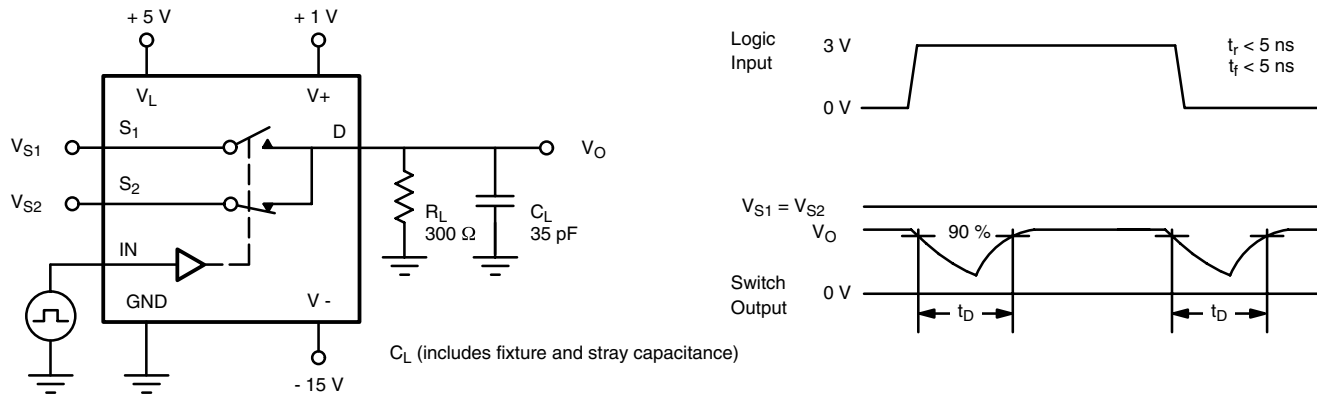


Figure 3. Break-Before-Make (DG419B)

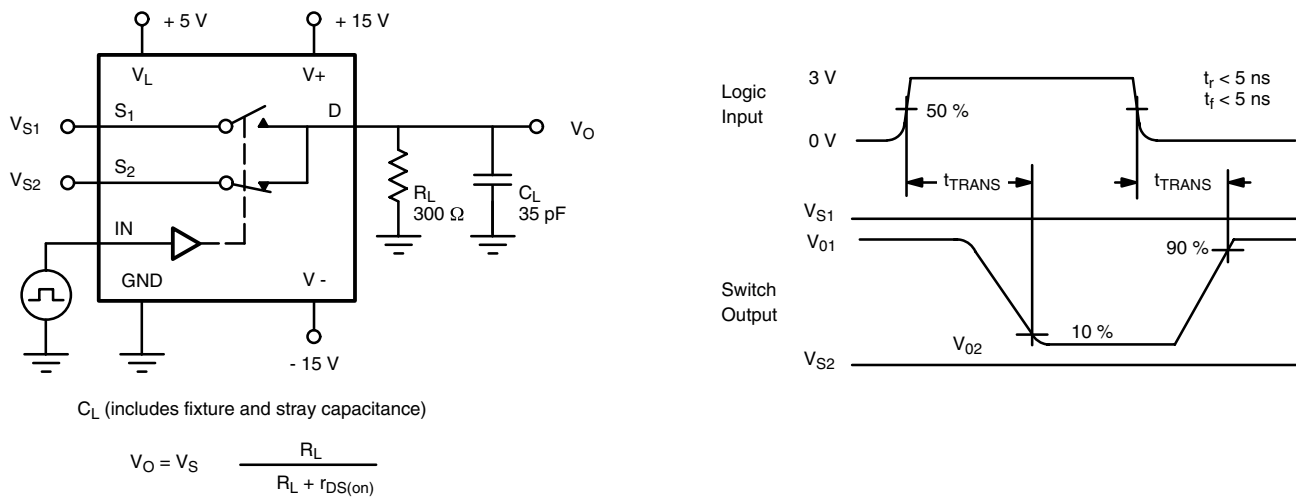


Figure 4. Transition Time (DG419B)

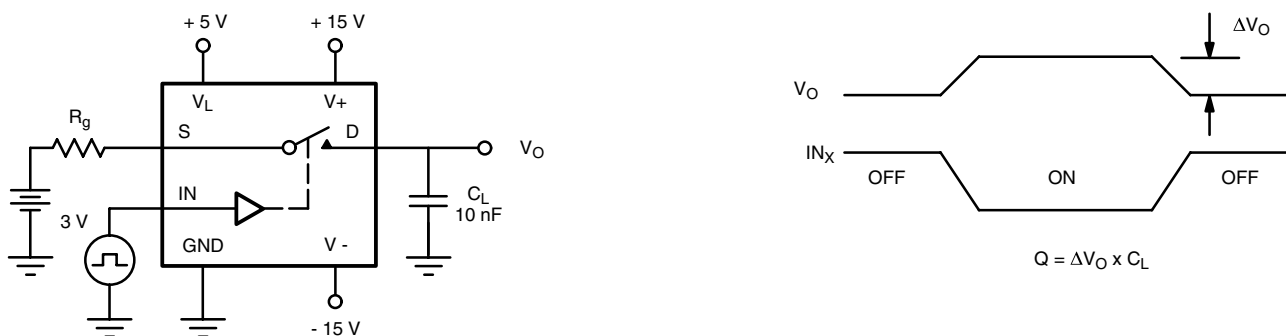
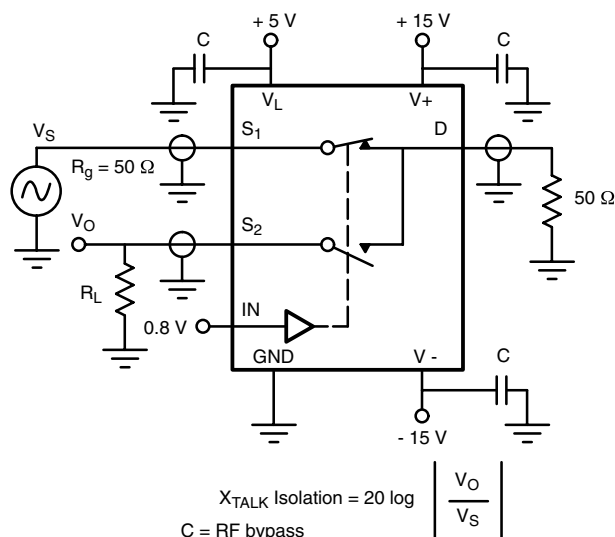
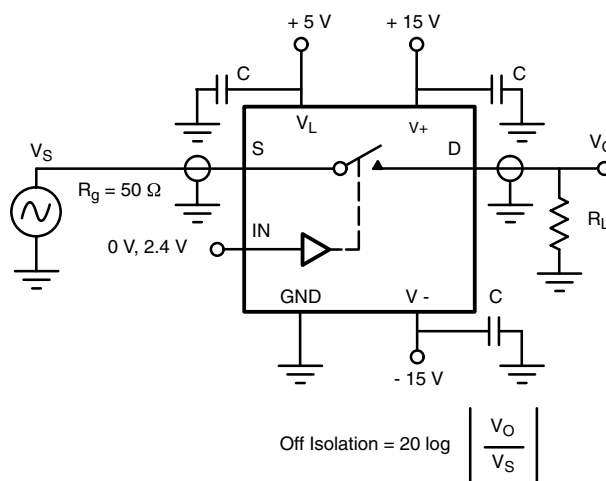
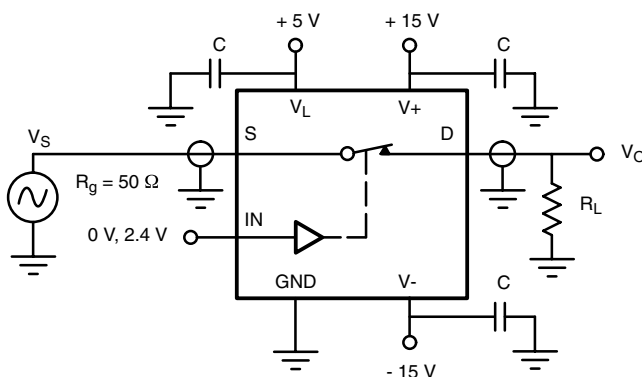
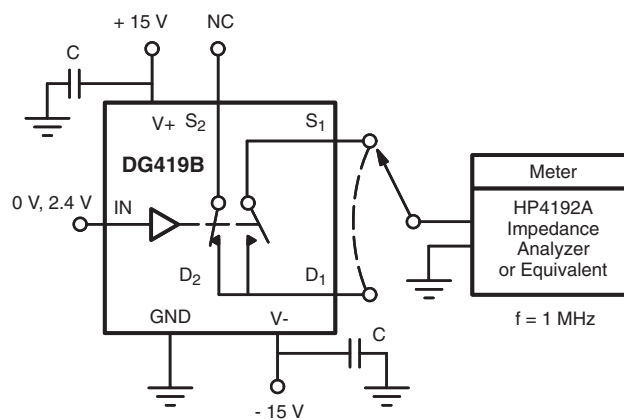
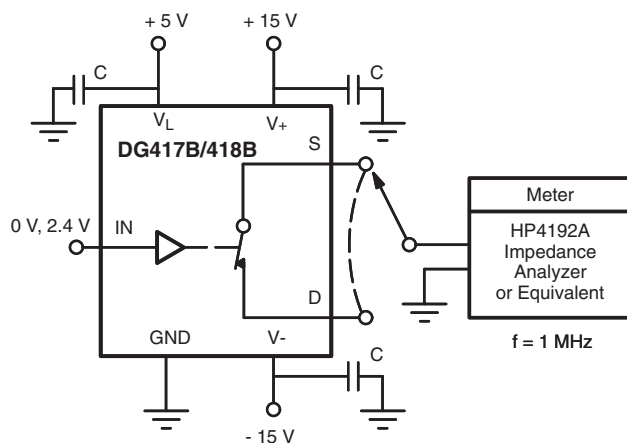


Figure 5. Charge Injection

TEST CIRCUITS

Figure 6. Crosstalk

Figure 7. Off isolation

Figure 8. Insertion Loss

Figure 9. Source/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72107.



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

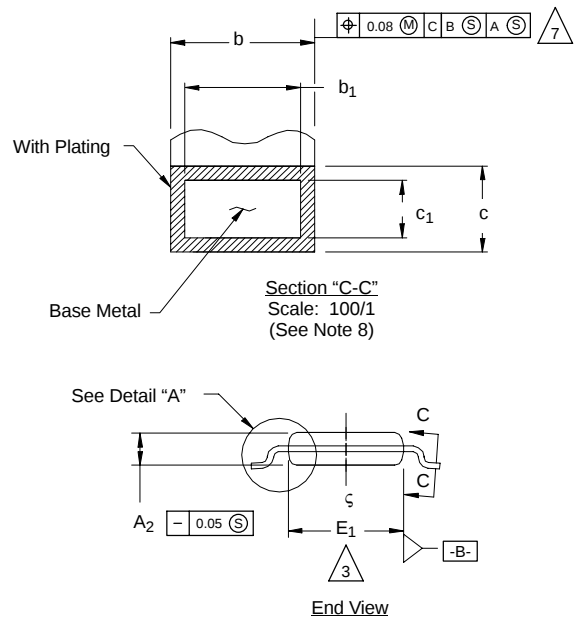
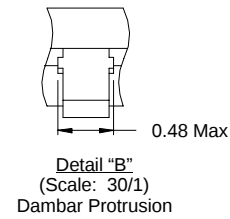
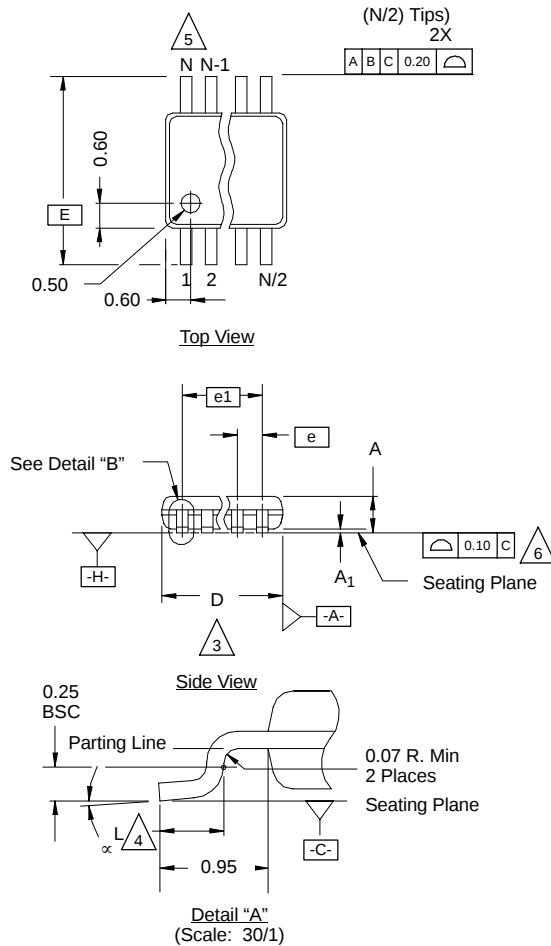


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



MSOP: 8-LEADS

JEDEC Part Number: MO-187, (Variation AA and BA)



NOTES:

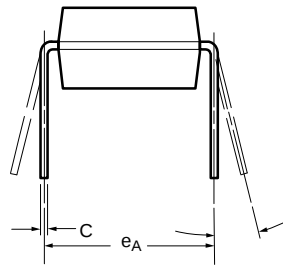
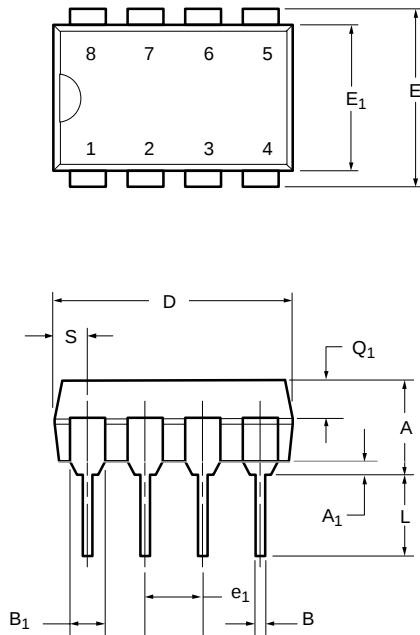
- Die thickness allowable is 0.203 ± 0.0127 .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane $\square H$, mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums $\square A$ and $\square B$ to be determined Datum plane $\square H$.
- Exposed pad area in bottom side is the same as the leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A ₁	0.05	0.10	0.15	
A ₂	0.75	0.85	0.95	
b	0.25	-	0.38	8
b ₁	0.25	0.30	0.33	8
c	0.13	-	0.23	
c ₁	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E ₁	2.90	3.00	3.10	3
e	0.65 BSC			
e ₁	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
α	0°	4°	6°	
ECN: T-02080—Rev. C, 15-Jul-02				
DWG: 5867				



PDIP: 8-LEAD

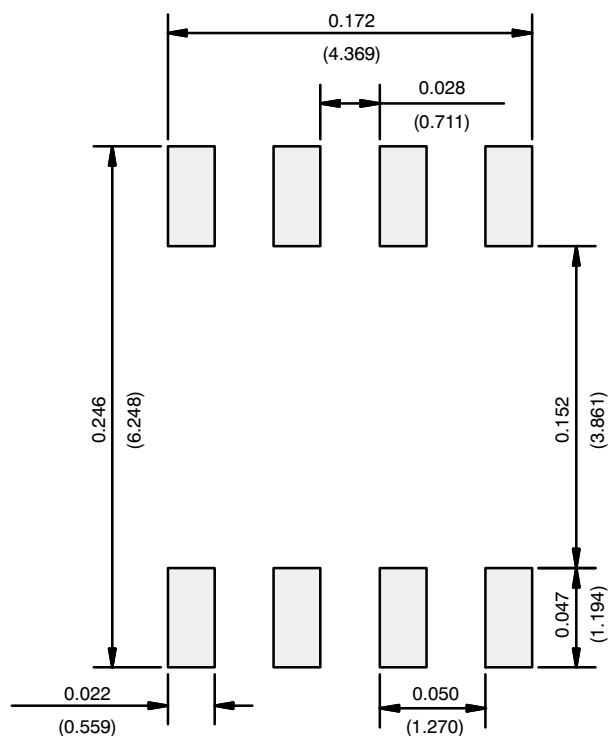


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065

ECN: S-03946—Rev. E, 09-Jul-01
DWG: 5478

NOTE: End leads may be half leads.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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