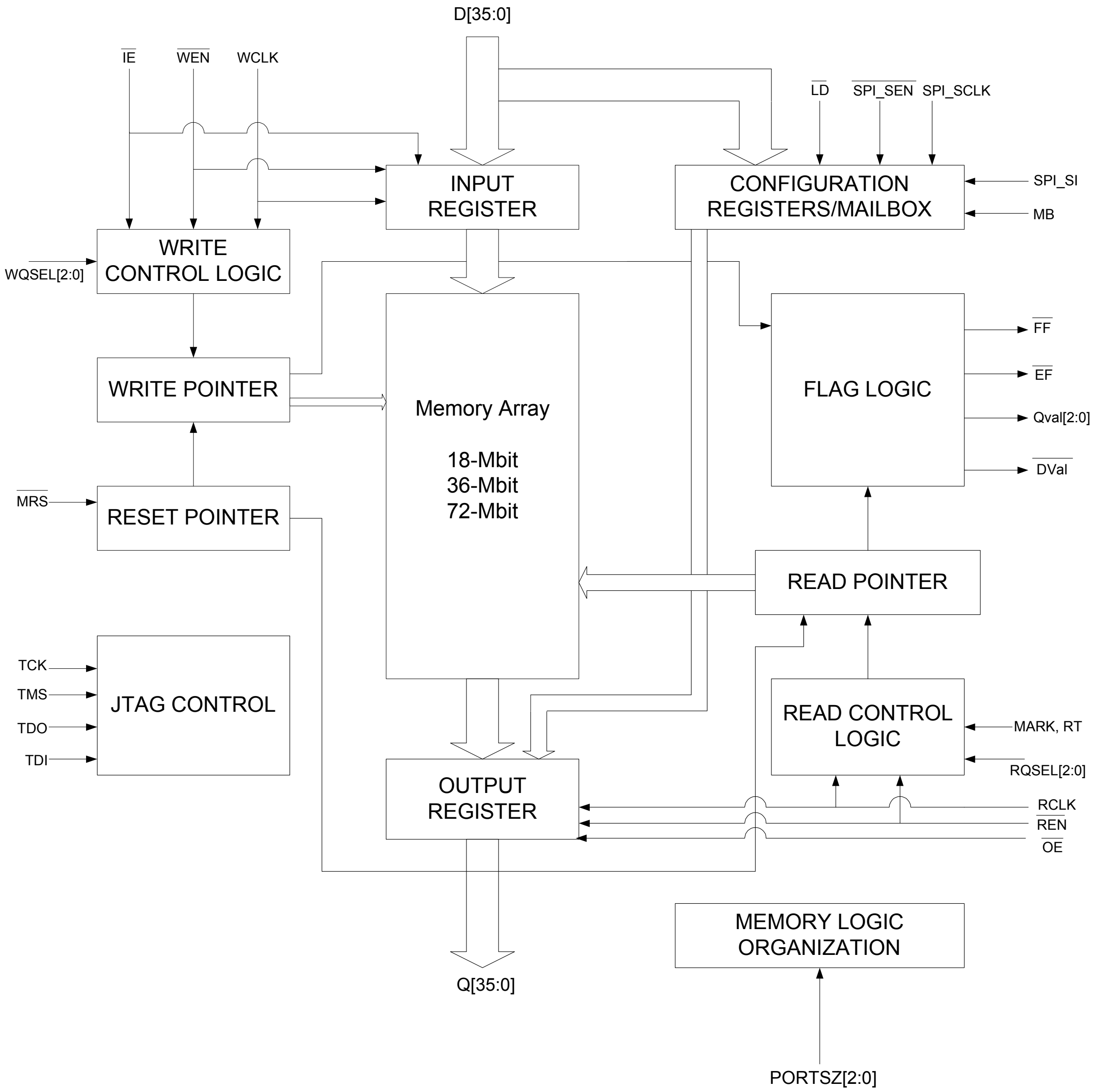
Logic Block Diagram



Contents

Pin Diagram for CYF2XXXVXXL

Figure 1. 209-ball FBGA (Top View) [1]

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{FF}$	D0	D1	WQSEL0	PORTSZ0	PORTSZ1	DNU	RQSEL0	RT	Q0	Q1
B	$\overline{EF}$	D2	D3	WQSEL1	DNU	PORTSZ2	DNU	RQSEL1	$\overline{REN}$	Q2	Q3
C	D4	D5	$\overline{WEN}$	WQSEL2	V_{CC1}	DNU	V_{CC1}	RQSEL2	RCLK	Q4	Q5
D	D6	D7	V_{SS}	V_{CC1}	DNU	$\overline{LD}$	DNU	V_{CC1}	V_{SS}	Q6	Q7
E	D8	D9	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CCIO}	V_{CCIO}	V_{CC2}	V_{CC2}	Q8	Q9
F	D10	D11	V_{SS}	V_{SS}	V_{SS}	DNU	V_{SS}	V_{SS}	V_{SS}	Q10	Q11
G	D12	D13	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q12	Q13
H	D14	D15	V_{SS}	V_{SS}	V_{SS}	V_{CC1}	V_{SS}	V_{SS}	V_{SS}	Q14	Q15
J	D16	D17	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q16	Q17
K	DNU	DNU	WCLK	DNU	V_{SS}	$\overline{IE}$	VSS	DNU	V_{CCIO}	V_{CCIO}	V_{CCIO}
L	D18	D19	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q18	Q19
M	D20	D21	V_{SS}	V_{SS}	V_{SS}	V_{CC1}	VSS	VSS	V_{SS}	Q20	Q21
N	D22	D23	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CC1}	V_{CCIO}	V_{CC2}	V_{CC2}	Q22	Q23
P	D24	D25	V_{SS}	V_{SS}	V_{SS}	$\overline{SPI\_SEN}$	V_{SS}	V_{SS}	V_{SS}	Q24	Q25
R	D26	D27	V_{CC2}	V_{CC2}	V_{CCIO}	V_{CCIO}	V_{CCIO}	V_{CC2}	V_{CC2}	Q26	Q27
T	D28	D29	V_{SS}	V_{CC1}	V_{CC1}	SPI_SI	V_{CC1}	V_{CC1}	V_{SS}	Q28	Q29
U	$\overline{DVal}$	DNU	D30	D31	DNU	DNU [2]	SPI_SCLK	V_{REF}	$\overline{OE}$	Q30	Q31
V	QVal1	QVal0	D32	D33	DNU	$\overline{MRS}$	MB	DNU	MARK	Q32	Q33
W	TDO	QVal2	D34	D35	TDI	DNU	TMS	TCK	DNU	Q34	Q35

Notes

[1] Pin Diagram for 18-Mbit, 36-Mbit & 72-Mbit; 1.8V & 3.3V IO voltage options.

[2] This pin should be tied to V_{SS} preferably or can be left floating to ensure normal operation.

Pin Definitions

Pin Name	I/O	Pin Description
MRS	Input	Master reset: MRS initializes the read and write pointers to zero, resets to 8 queue operating mode and sets the output register to all zeroes. During Master Reset, the configuration registers are all set to default values and the flags are reset.
PORTSZ [2:0]	Input	Port word size select: Port word width select pins (common for read and write ports).
WCLK	Input	Write clock: Data is written into the FIFO queue indicated by WQSEL[2:0] on the rising edge of WCLK provided writes are enabled (WEN low). Writes are performed either to the FIFO memory or configuration registers based on the status of the load signal (LD).
LD	Input	Load: When LD is LOW, D[7:0] (Q[7:0]) are written (read) into (from) the configuration registers. When LD is HIGH, D[35:0] (Q[35:0]) are written (read) into (from) the FIFO.
WEN	Input	Write enable: WEN enables WCLK to write data into the FIFO memory and configuration registers.
WQSEL[2:0]	Input	Write Queue select: Selects the FIFO queue to be written into based on the operating mode.
IE	Input	Input enable: IE is the data input enable signal that controls the enabling and disabling of the 36-bit data input pins. If it is enabled, data on the D[35:0] pins is written into the FIFO. The internal write address pointer is always incremented at rising edge of WCLK if WEN is enabled, regardless of the IE level. This is used for 'write masking' or incrementing the write pointer without writing into a location.
D[35:0]	Input	Data inputs: Data inputs for a 36-bit bus.
RCLK	Input	Read clock: Data is read from the FIFO queue indicated by RQSEL[2:0] on each rising edge of RCLK provided reads are enabled (REN low). LD determines whether the data is read from FIFO memory or configuration registers.
REN	Input	Read enable: REN enables RCLK to read data from the FIFO memory and configuration registers.
RQSEL[2:0]	Input	Read Queue select: Selects the FIFO queue to be read from based on the operating mode.
OE	Input	Output enable: When OE is LOW, FIFO data outputs are enabled; when OE is HIGH, the FIFO's outputs are in High Z (high impedance) state.
Q[35:0]	Output	Data outputs: Data outputs for a 36-bit bus.
DVal	Output	Data valid: Active low data valid signal to indicate valid data on Q[35:0].
QVal[2:0]	Output	Queue valid: Validate with DVal to indicate the Queue for which data is being read out on Q[35:0] DVal = 0 and QVal = 000 valid data read out from Queue-0 on Q[35:0] DVal = 0 and QVal = 001 valid data read out from Queue-1 on Q[35:0] DVal = 0 and QVal = 010 valid data read out from Queue-2 on Q[35:0] DVal = 0 and QVal = 011 valid data read out from Queue-3 on Q[35:0] DVal = 0 and QVal = 100 valid data read out from Queue-4 on Q[35:0] DVal = 0 and QVal = 101 valid data read out from Queue-5 on Q[35:0] DVal = 0 and QVal = 110 valid data read out from Queue-6 on Q[35:0] DVal = 0 and QVal = 111 valid data read out from Queue-7 on Q[35:0]
MARK	Input	Mark for retransmit: When this pin is asserted the memory location corresponding to valid data present on the output bus is marked. Any subsequent retransmit operation resets the read pointer to this memory location.
RT	Input	Retransmit: A HIGH pulse on RT resets the internal read pointer to a physical location in the FIFO which is marked by the user (using MARK pin). With every valid read cycle after retransmit, previously accessed data is read until the FIFO is empty.
MB	Input	Mailbox: When asserted the reads and writes happen to flow-through mailbox register.
EF	Output	Empty flag: When EF is LOW, the Queue is empty. EF is synchronized to RCLK.
FF	Output	Full flag: When FF is LOW, the Queue is full. FF is synchronized to WCLK.
SPI_SCLK	Input	Serial clock: A rising edge on SPI_SCLK clocks the serial data present on the SPI_SI input into the offset registers if SPI_SEN is enabled.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
SPI_SI	Input	Serial input: Serial input when SPI_SEN is enabled.
SPI_SEN	Input	Serial enable: Enables serial loading of configuration registers.
TCK	Input	Test clock (TCK) pin for JTAG.
TMS	Input	Test mode select (TMS) pin for JTAG.
TDI	Input	Test data in (TDI) pin for JTAG.
TDO	Output	Test data out (TDO) for JTAG.
V_{REF}	Input Reference	Reference voltage: Reference voltage of 0.75V (regardless of I/O standard used).
V_{CC1}	Power Supply	Core voltage supply 1: 1.8 V supply voltage
V_{CC2}	Power Supply	Core voltage supply 2: 1.5 V supply voltage
V_{CCIO}	Power Supply	Supply for I/Os
V_{SS}	Ground	Ground
DNU	–	Do not use: These pins need to be left floating.

Architecture

The CYF2072V, CYF2036V, and CYF2018V are memory arrays of 72-Mbit, 36-Mbit, and 18-Mbit respectively. The memory organization is user configurable and word sizes can be selected as × 9, × 12, × 16, × 18, × 20, × 24, × 32, or × 36. The logic blocks to implement the FIFO functionality and the associated features are built around these memory arrays.

The input and output data buses have a maximum width of 36 bits. The input data bus goes to an input register and the data flow from the input register to the memory is controlled by the write control logic. The inputs to the write logic block are WCLK, WEN, IE and WQSEL[2:0]. When the writes are enabled through WEN and inputs are enabled through IE, data on the input bus is written into the FIFO queue indicated by WQSEL[2:0] at the rising edge of WCLK. This also increments the write pointer for the corresponding FIFO queue. Enabling writes but disabling the data input through IE only increments the write pointer without doing any writes or altering the contents of the location.

Similarly, the output register is connected to the data output bus. Transfer of contents from the memory to the output register is controlled by the read control logic. The inputs to the read control logic include RCLK, REN, RQSEL[2:0], MARK and RT. RQSEL[2:0] selects the Queue to be read. When reads are enabled by REN and outputs are enabled through OE, data from the FIFO queue is transferred to the output data bus at the rising edge of RCLK along with active low DVal. Qval[2:0] indicates the Queue number to which the read data belongs. If OE is disabled and the reads are enabled, the outputs are in high impedance state, but internally the read pointer for the corresponding RQSEL[2:0] is incremented.

The MARK signal is used to ‘mark’ the location from which data can be retransmitted when requested and RT is asserted to retransmit the data from the marked location.

During write operation, the number of writes performed is always an even number (i.e., minimum write burst length is two and number of writes always a multiple of two). Whereas during read operation, the number of reads performed can be even or odd (i.e., minimum read burst length is one).

It is possible to divide the whole memory space into 2, 4 or 8 equal sized arrays. By default, the FIFO is accessed as a 8Q device. For more explanation please refer to Multi-Queue Operation on page 7.

Reset Logic

A Master Reset cycle is required after power up before accessing the FIFO. MRS resets the configuration registers which configures the device to Multi-Queue (8Q) mode and sets the output register to zero. It also initializes the read and write pointers to zero, and sets the flags to their default condition (FF deasserted and EF asserted) for all eight Queues. The mark address is also set to the default physical location for each queue.

After MRS, a minimum latency of 1024 clocks is necessary before the first access. The word size is configured through PORTSZ pins; values of the three PORTSZ pins are latched on rising edge of MRS.

Multi-Queue Operation

In this mode, the entire memory space is divided into equal sized memory arrays and each individual memory array can be accessed as an independent FIFO. These equally sized memory arrays are referred to as Queues and they are numbered Queue-0 to Queue-7. For example, when the 72M device, is configured in eight queue mode, the entire memory space of 72M is divided into eight memory arrays of 9M capacity. These queues can be accessed independently using the queue select signals WQSEL[2:0] and RQSEL[2:0].

It is also possible to configure the whole memory space of CYF2072V into 4 or 2 equal sized arrays. This is equivalent to having four or two independent Queues inside the FIFO.

The device can be used as a single FIFO by configuring the FIFO in single queue mode. In this case, the entire memory space is accessed as a single Queue.

The number of Queues is configured based on the value of D2, D1 & D0 bit of configuration register 0x3 (refer to Table 2 on page 9). Table 3 on page 9 shows the value to be set in D2, D1 & D0 of configuration register 0x3 to configure the device in 1/2/4/8 Queue modes.

Table 1. FIFO Depth - Word Size & Operating Mode

PORTSZ[2:0]	Word Size	FIFO Depth/queue [3] (No. of locations)				Memory Size [3]	Active Input Data Pins D[N:0]	Active Output Data Pins Q[N:0]
		1Q mode	2Q mode	4Q mode	8Q mode			
000	× 9	8 M	4 M	2 M	1 M	72-Mbit	D[8:0]	Q[8:0]
001	× 12	4 M	2 M	1 M	512 K	48-Mbit	D[11:0]	Q[11:0]
010	× 16	4 M	2 M	1 M	512 K	64-Mbit	D[15:0]	Q[15:0]
011	× 18	4 M	2 M	1 M	512 K	72-Mbit	D[17:0]	Q[17:0]
100	× 20	2 M	1 M	512 K	256 K	40-Mbit	D[19:0]	Q[19:0]
101	× 24	2 M	1 M	512 K	256 K	48-Mbit	D[23:0]	Q[23:0]
110	× 32	2 M	1 M	512 K	256 K	64-Mbit	D[31:0]	Q[31:0]
111	× 36	2 M	1 M	512 K	256 K	72-Mbit	D[35:0]	Q[35:0]

Selecting Word Sizes

The word sizes are configured based on the logic levels on the PORTSZ pins during the master reset ($\overline{\text{MRS}}$) cycle only (latched on low to high edge). The port size cannot be changed during normal mode of operation and these pins are ignored. Table 1 explains the pins of D[35:0] and Q[35:0] that will have valid data in modes where the word size is less than × 36. If word size is less than × 36, the unused output pins are tri-stated by the device.and unused input pins will be ignored by the internal logic. The pins with valid data input D[N:0] and output Q[N:0] is given in Table 1.

Memory Organization for Different Port Sizes

The 72-Mbit memory has different organizations for different port sizes. Table 1 shows the depth of the FIFO for all port sizes.

Note that for all port sizes, four to eight locations are not available for writing the data and are used to safeguard against false synchronization of empty and full flags.

Data Valid Signal ($\overline{\text{DVal}}$)

Data valid ($\overline{\text{DVal}}$) is an active LOW signal, synchronized to RCLK signal and is provided to check for the data on output bus. When a read operation is performed, the $\overline{\text{DVal}}$ signal goes low along with output data. This helps user to capture the data without having to keep track of $\overline{\text{REN}}$ to data output latency. This signal also helps when write and read operations are performed continuously at different frequencies by indicating when valid data is available at the output port Q[35:0]. In multi-queue mode, this signal should be used along with Queue Valid Signal (QVal[2:0]) to determine the queue from which data is being read.

Queue Valid Signal (QVal[2:0])

Queue Valid (Qval[2:0]) is a three bit output that indicates the Queue from which valid data is being read. When $\overline{\text{DVal}}$ signal is high, the values on this bus should be ignored.

Write Mask and Read Skip Operation

As mentioned in Architecture on page 6, enabling writes but disabling the inputs ($\overline{\text{IE}}$ HIGH) increments the write pointer without doing any write operations or altering the contents of the location.

This feature is called Write Mask and allows user to move the write pointer without actually writing to the locations. This “write masking” ability is useful in some video applications such as Picture In Picture (PIP).

Similarly, during a read operation, if the outputs are disabled ($\overline{\text{OE}}$ high). The read data does not appear on the output bus; however, the read pointer is incremented. This feature is referred to as a Read Skip Operation.

Note

[3] For all port sizes, four to eight locations are not available for writing the data.

Flow-through mailbox Register

This register transfers data from input to output directly bypassing the FIFO sequence. When MB signal is asserted the data present on D[35:0] will be available on Q[35:0] after two WCLK cycles. Normal read and write operations are not allowed during flow-through mailbox operation. Before starting Flow-through mailbox operation FIFO read should be completed to make data valid (DVal) high in order to avoid data loss from FIFO. The width of flow-through mailbox register always corresponds to port size.

Flag Operation

This device provides two flags to indicate the condition of the FIFO Queues.

Full Flag

Full Flag (FF) LOW indicates whether the queue accessed by WQSEL[2:0] is full and it operates on double word (burst length of two) boundaries. Write operations are inhibited whenever FF is LOW regardless of the state of WEN. FF is synchronized to WCLK, that is, it is exclusively updated by each rising edge of WCLK. The worst case assertion latency for Full Flag is four. As the user cannot know that the FIFO is full for four clock cycles, it is possible that user continues writing data during this time. In this case, the four data words written will be stored to prevent data loss and these words have to be read back in order for full flag to get de-asserted. In 2Q or 4Q or 8Q mode, FF indicates the status of the queue selected by WQSEL[2:0]. The minimum number of reads required to de-assert full-flag are two and the maximum number of reads required to de-assert full flag are six. The assertion and de-assertion latencies of Full Flag are given in Latency Table on page 17.

Empty Flag

Empty Flag (EF) LOW indicates that the queue accessed by RQSEL[2:0] is empty and its de-assertion depends on burst writes. Read operations are inhibited whenever EF is LOW, regardless of the state of REN. EF is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK. In 2Q/4Q/8Q mode, EF indicates the status of the queue selected by RQSEL[2:0]. The assertion and de-assertion latencies of Empty Flag are given in Latency Table on page 17.

Retransmit from Mark Operation

The retransmit feature is useful for transferring packets of data repeatedly. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. Initiation of a retransmit operation (using RT pin) resets the internal read pointer to a physical location of the FIFO that is marked by the user (using the MARK pin).

The retransmit feature can be used when two or more data words have been written to the queue. When the MARK pin is asserted, the memory location corresponding to valid data (DVal signal LOW) present on the output bus is marked. QVal[2:0] signals can be used to validate the queue for which the mark operation is being performed. A mark operation is mandated prior to initiating a retransmit operation for a queue.

In this device the RT signal is validated with RQSEL[2:0], i.e., Retransmit function will be performed for the Queue that is selected by RQSEL[2:0]. With every valid read cycle after retransmit, previously accessed data is read until the queue becomes empty. Data written to the queue (Queue on which retransmit operation is being performed) after activation of RT are also transmitted. The full depth of the queue can be repeatedly retransmitted. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Refer to the latency table for the associated flag update latencies after initiation of a retransmit cycle.

A retransmit operation should not be initiated when reads or writes are in progress. User should wait for four RCLK cycles after disabling reads before RT is asserted to ensure that the reads are completed.

On initiation of RT the ‘marked’ location becomes the new Full Boundary. If user continues to write the data after initiation of a retransmit operation, FF will be asserted when this boundary is reached i.e. FF is asserted once the write pointer reaches the marked location.This prevents overwriting and data-loss. During RT reads the full boundary remains frozen to the marked location and is released when the FIFO becomes empty. i.e. FF remains LOW until the entire FIFO is read. Full flag is deasserted $L_{FF\_RELEASE}$ cycles after the EF is asserted. Full boundary is also released on a reset operation (MRS).

Refer to Latency Table on page 17 for more details.

Programming Configuration Registers

The CYF2072V has ten 8-bit user configurable registers. These registers are used to configure the number of queues & to set the Fast CLK Bit.

These registers can be programmed in one of two ways: serial loading or parallel loading method. The loading method is selected using the SPI_SEN (Serial Enable) pin. A LOW on the SPI_SEN selects the serial method for writing into the registers whereas a HIGH on SPI_SEN selects parallel loading method. For serial programming, there is a separate SCLK and a Serial Input (SI). In parallel mode, the load (LD) pin is used to perform write and read operations on these registers. The write and read operations are performed in a sequence from the first location(0x1) to the last location (0xA) when the LD pin is held LOW. If LD is HIGH, the FIFO queues are written or read.

Register values can be read through the parallel output port regardless of the programming mode selected (serial or parallel). Register values cannot be read serially. The configuration registers should be programmed only once after master reset to ensure accurate flag operation, regardless of whether serial or parallel programming is selected.

See Table 4 on page 10 and Table 5 on page 11 for access to configuration registers in serial and parallel modes.

In parallel mode, the read and write operations loop back when the maximum address location of the configuration registers is reached. Simultaneous read and write operations must be avoided on the configuration registers. Any change in configuration registers will take effect after eight write clock cycles (WCLK) cycles.

Table 2. Configuration Registers

ADDR	Configuration Register	Default	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
0x1	Reserved	0x00	X	X	X	X	X	X	X	X
0x2	Reserved	0x00	X	X	X	X	X	X	X	X
0x3	Number of Queues	0x07	X	X	X	X	X	D2	D1	D0
0x4	Reserved	0x7F	X	X	X	X	X	X	X	X
0x5	Reserved	0x00	X	X	X	X	X	X	X	X
0x6	Reserved	0x00	X	X	X	X	X	X	X	X
0x7	Reserved	0x7F	X	X	X	X	X	X	X	X
0x8	Reserved	0x00	X	X	X	X	X	X	X	X
0x9	Reserved	0x00	X	X	X	X	X	X	X	X
0xA	Fast CLK Bit Register	1XXXXXXXb	Fast CLK bit	X	X	X	X	X	X	X

Table 3. Multi-Queue Configuration

Operating Mode (given by configuration register 0x3 [7:0])	RQSEL[2:0]/WQSEL[2:0]	Queue Number Selected
1Q mode (register 0x3[2:0] = 8’b0000 0000)	000	0
	001–111	Invalid
2Q mode (register 0x3[2:0] = 8’b0000 0001)	000	0
	001	1
	010–111	invalid
4Q mode (register 0x3[2:0] = 8’b0000 001X)	000	0
	001	1
	010	2
	011	3
	100–111	invalid
8Q mode (register 0x3[2:0] = 8’b0000 01XX)	000	0
	001	1
	010	2
	011	3
	100	4
	101	5
	110	6
	111	7

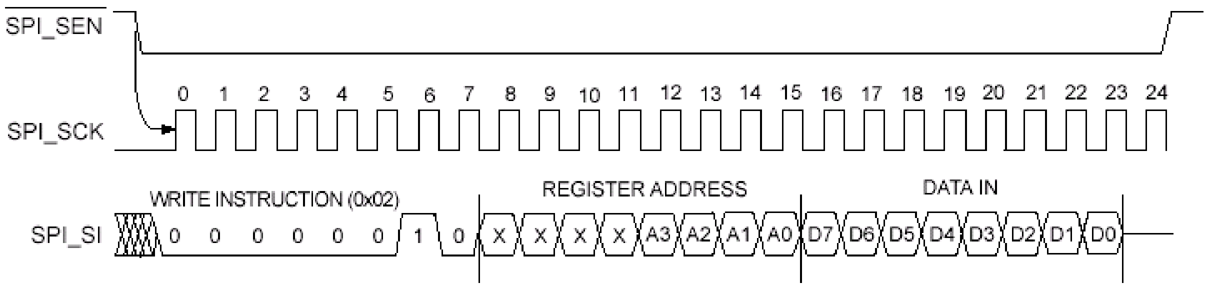
Table 4. Writing and Reading Configuration Registers in Parallel Mode

$\overline{\text{SPI\_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SPI_SCLK	Operation
1	0	0	1	↑ First rising edge because both $\overline{\text{LD}}$ and $\overline{\text{WEN}}$ are low	X	X	Parallel write to first register
1	0	0	1	↑ Second rising edge	X	X	Parallel write to second register
1	0	0	1	↑ Third rising edge	X	X	Parallel write to third register
1	0	0	1	↑ Fourth rising edge	X	X	Parallel write to fourth register
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	•	X	X	•
1	0	0	1	↑ Tenth rising edge	X	X	Parallel write to tenth register
1	0	0	1	↑ Eleventh rising edge	X	X	Parallel write to first register (roll back)
1	0	1	0	X	↑ First rising edge since both $\overline{\text{LD}}$ and $\overline{\text{REN}}$ are low	X	Parallel read from first register
1	0	1	0	X	↑ Second rising edge	X	Parallel read from second register
1	0	1	0	X	↑ Third rising edge	X	Parallel read from third register
1	0	1	0	X	↑ Fourth rising edge	X	Parallel read from fourth register
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	•	X	•
1	0	1	0	X	↑ Tenth rising edge	X	Parallel read from tenth register
1	0	1	0	X	↑ Eleventh rising edge	X	Parallel read from first register (roll back)
1	X	1	1	X	X	X	No operation
X	1	0	X	↑ Rising edge	X	X	Write to FIFO memory
X	1	X	0	X	↑ Rising edge	X	Read from FIFO memory
0	0	X	1	X	X	X	Illegal operation

Table 5. Writing into Configuration Registers in Serial Mode

$\overline{\text{SPI\_SEN}}$	$\overline{\text{LD}}$	$\overline{\text{WEN}}$	$\overline{\text{REN}}$	WCLK	RCLK	SCLK	Operation
0	1	X	X	X	X	↑ Rising edge	Each rising of the SCLK clocks in one bit from the SI (Serial In). Any of the 10 registers can be addressed and written to, following the SPI protocol.
X	1	0	X	↑ Rising edge	X	X	Parallel write to FIFO memory.
X	1	X	0	X	↑ Rising edge	X	Parallel read from FIFO memory.
1	0	1	1	X	X	X	This corresponds to parallel mode (refer to Table 4 on page 10).

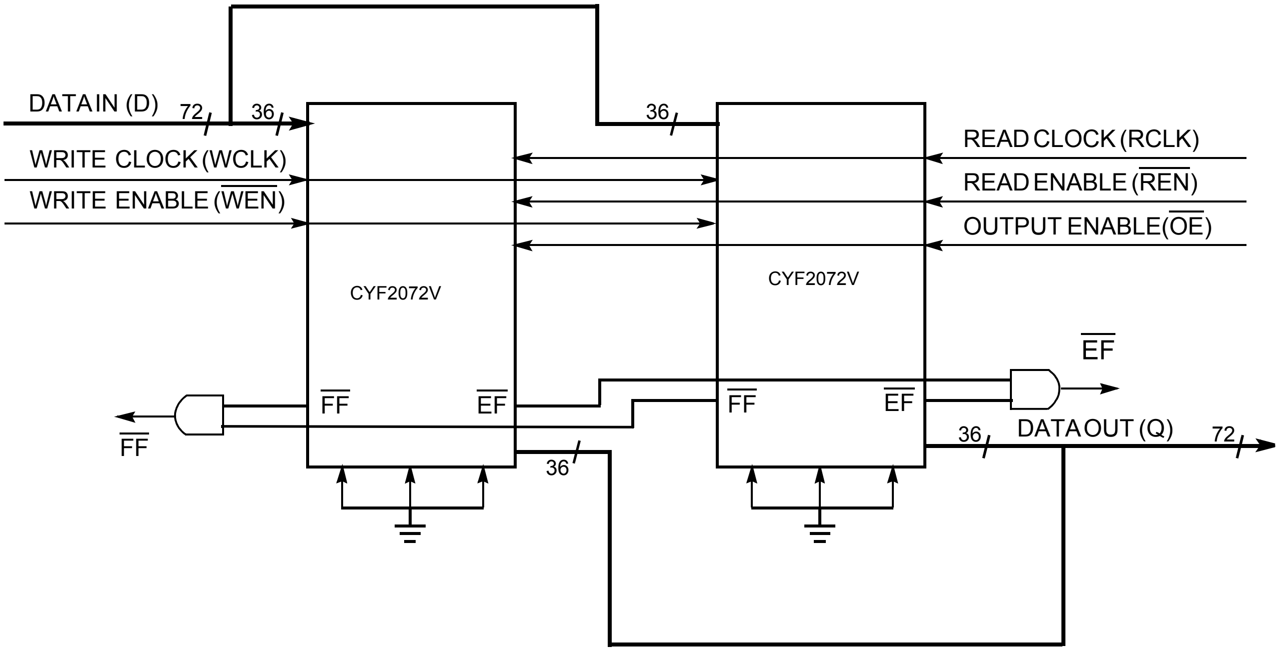
Figure 2. Serial WRITE to Configuration Register



Width Expansion Configuration

The width of CYF2072V can be expanded to provide word widths greater than 36 bits. During width expansion mode, all control line inputs are common and all flags are available. Empty (Full) flags are created by ANDing the Empty (Full) flags of every FIFO. This technique avoids reading data from or writing data to the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. Figure 3 demonstrates an example of a 72 bit-word width by using two 36-bit word CYF2072Vs.

Figure 3. Using Two CYF2072Vs for Width Expansion



Power Up

The device becomes functional after V_{CC1}, V_{CC2}, V_{CCIO}, and Vref attain minimum stable voltage required as given in Recommended DC Operating Conditions on page 16. The device can be accessed in t_{PU} time after these supplies attain the minimum required level (see Switching Characteristics on page 19). There is no power sequencing required for the device.

Read/Write Clock Requirements

The read and write clocks must satisfy the following requirements:

- Both read (RCLK) and write (WCLK) clocks should be free-running.
- The clock frequency for both clocks should be between the minimum and maximum range given in Switching Characteristics on page 19.
- The RCLK to WCLK ratio should be in the range of 0.5 to 2.

For proper FIFO operation, the device must determine which of the input clocks – RCLK or WCLK – is faster. This is evaluated by using counters after the MRS cycle. The device uses two 9-bit counters inside (one running on RCLK and other on WCLK), which count 256 cycles of read and write clock after MRS. The clock of the counter which reaches its terminal count first is used as master clock inside the FIFO.

When there is change in the relative frequency of RCLK and WCLK during normal operation of FIFO, user can specify it by using "Fast CLK bit" in the configuration register (0xA).

"1" - indicates f_{req} (WCLK) > f_{req} (RCLK)

"0" - indicates f_{req} (WCLK) < f_{req} (RCLK)

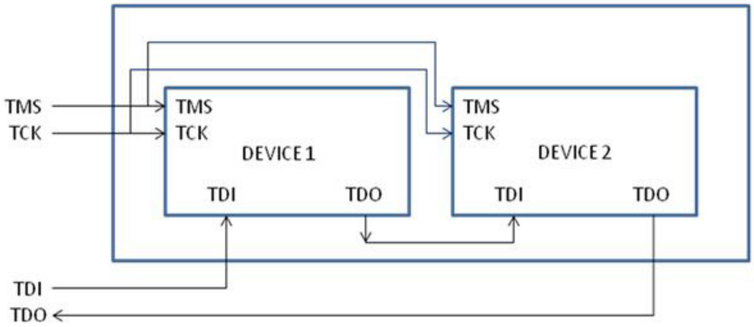
The result of counter evaluated frequency is available in this register bit. User can override the counter evaluated frequency for faster clock by changing this bit.

Whenever there is a change in this bit value, user must wait t_{PLL} time before issuing the next read or write to FIFO.

JTAG Operation

The Programmable Multi-Queue FIFO has two devices connected internally in a JTAG chain as shown in Figure 4.

Figure 4. JTAG Operation



Test Access Port

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven on the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP CONTROLLER State Diagram. TDI is internally pulled up and can be left unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any of the TAP registers.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any of the TAP registers.

Note: Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in Figure 5. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a Reset state.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the device with minimal delay.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the device. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the device input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD instructions can be used to capture the contents of the input and output ring. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the device and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Table 6.

JTAG IDCODES

Table 6. JTAG IDCODES

	IR Register Length	Device ID (HEX)	Bypass Register Length
Device-1	3	“Ignore”	1
Device-2	8	1E3261CF	1

OPCODES Supported

Table 7. OPCODES Supported

Device-1	Opcode (Binary)		Device-2	Opcode (Binary)
BYPASS	111		BYPASS	11111111
			EXTEST	00000000
			HIGHZ	00000111
			SAMPLE/PRELOAD	00000001
			IDCODE	00001111

JTAG Instructions

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power-up or whenever the TAP controller is supplied a Test-Logic-RST state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required; i.e. while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

HIGHZ

The HIGHZ instruction mode is used to set all the user I/O pins to an inactive drive state. These pins are tri-stated until a new JATG instruction is executed. When this instruction is selected, the bypass register is connected between the TDI and TDO ports.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

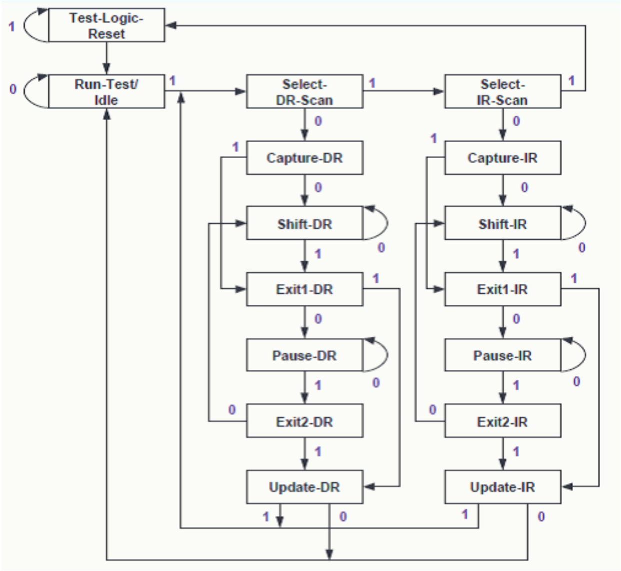
Instruction Update and Bypass

1. Every time an instruction is loaded through JTAG port, BYPASS command needs to be loaded on device 1. For Ex; to push PRELOAD command, BYPASS to device-1 "111" + PRELOAD to device-2 "00000001" needs to be sent.
2. When both devices are put on BYPASS, any pattern sent in should be observed on TDO after two TCK delay.

TAP Controller State Diagram

TAP controller is a Finite State Machine with 16 states as shown in Figure 5. State change is determined by the state of TMS on rising edge of TCK. Figure 5 shows the value of TMS for each state transition.

Figure 5. TAP Controller State Diagram



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature (without bias) .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Core supply voltage 1 (VCC1) to ground potential ....–0.3 V to 2.5 V

Core supply voltage 2 (VCC2) to ground potential ....–0.3 V to 1.65 V

Latch-up current .... > 100 mA

I/O port supply voltage (VCCIO) ....–0.3 V to 3.7 V

Voltage applied to I/O pins ....–0.3 V to 3.75 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (per MIL–STD–883, Method 3015) .... > 2001 V

Operating Range

Range	Ambient Temperature
Industrial	–40 °C to +85 °C

Recommended DC Operating Conditions

Parameter [4]	Description		Min	Typ	Max	Unit
V_{CC1}	Core supply voltage 1		1.70	1.80	1.90	V
V_{CC2}	Core supply voltage 2		1.425	1.5	1.575	V
V_{REF}	Reference voltage (irrespective of I/O standard used)		0.7	0.75	0.8	V
V_{CCIO}	I/O supply voltage, read and write banks.	LVCMOS33	3.00	3.30	3.60	V
		LVCMOS18	1.70	1.8	1.90	V

Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CC}	Active current	$V_{CC1} = V_{CC1MAX}$	–	–	300	mA
		$V_{CC2} = V_{CC2MAX}$, All I/O switching, 100 MHz	–	–	500	mA
		$V_{CCIO} = V_{CCIOMAX}$ (All outputs disabled)	–	–	100	mA
I_I	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V	–15	–	15	µA
I_{OZ}	I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V	–15	–	15	µA
C_P	Capacitance for TMS and TCK	–	–	–	16	pF
C_{PIO}	Capacitance for pins apart from TMS and TCK	–	–	–	8	pF

Note

[4] Device operation guaranteed for a supply rate > 1 V / µs.

I/O Characteristics

I/O Standard	Nominal I/O Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current (mA)	
		V_{IL}(max)	V_{IH}(min)	V_{OL}(max)	V_{OH}(min)	I_{OL}(max)	I_{OH}(max)
LVCMOS33	3.3 V	0.80	2.20	0.45	2.40	24	24
LVCMOS18	1.8 V	30% V_{CCIO}	65% V_{CCIO}	0.45	V_{CCIO} – 0.45	16	16

Latency Table

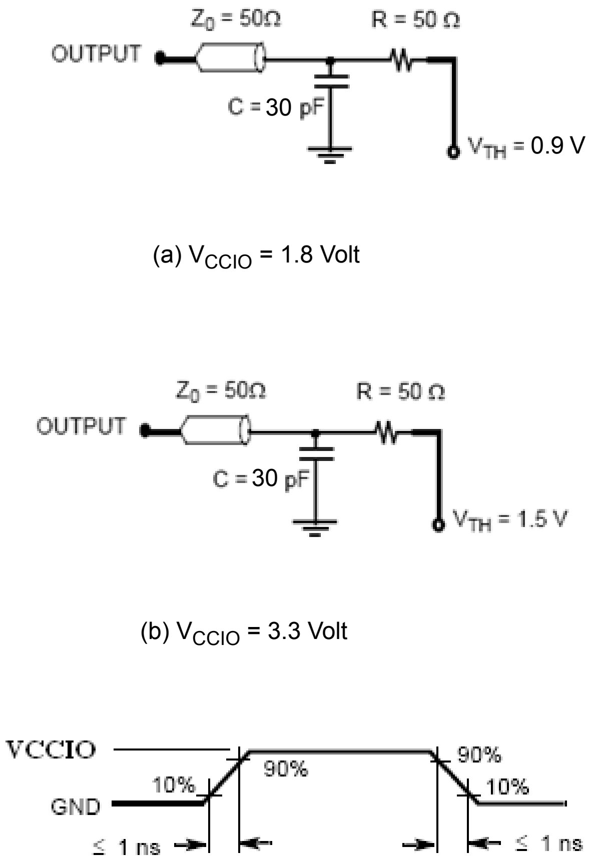
Latency Parameter	Number of Cycles [5]	Details
$L_{\overline{FF}\_ASSERT}$	Max = 4	Last data write to $\overline{FF}$ going low
$L_{\overline{EF}\_ASSERT}$	0	Last data read to $\overline{EF}$ going low
L_{RQSEL_CHANGE}	1	Minimum RCLK cycles before RQSEL[2:0] can change
L_{WQSEL_CHANGE}	2	Minimum WCLK cycles before WQSEL[2:0] can change
$L_{MAILBOX}$	2	Latency from write port to read port when MB = 1 (w.r.t. WCLK)
$L_{\overline{REN}\_TO\_DATA}$	4	Latency when $\overline{REN}$ is asserted low to first data output from FIFO
$L_{\overline{REN}\_TO\_CONFIG}$	4	Latency when $\overline{REN}$ is asserted along with $\overline{LD}$ to first data read from configuration registers
$L_{\overline{FF}\_DEASSERT}$	7	Read to $\overline{FF}$ going high
$L_{RT\_TO\_\overline{REN}}$	21	First RCLK posedge after RT goes low to initiation of reads by pulling $\overline{REN}$ low. Flags update within this period after initiation of a retransmit operation.
$L_{RT\_TO\_DATA}$	Max = 25	First RCLK posedge after RT goes LOW to valid data on Q[35:0].
L_{IN}	Max = 35	Initial latency for data read after FIFO goes empty during simultaneous read/write
$L_{\overline{EF}\_DEASSERT}$	Max = 32	Write to $\overline{EF}$ going high
$L_{\overline{FF}\_RELEASE}$	Max = 6	$\overline{EF}$ going low to $\overline{FF}$ de-assert during retransmit reads.

Note

[5] Latency mentioned in the latency table are applicable for clock ratio of 1.

AC Test Load Conditions

Figure 6. AC Test Load Conditions



(a) V_{CCIO} = 1.8 Volt

(b) V_{CCIO} = 3.3 Volt

(c) All Input Pulses

Switching Characteristics

Over the Operating Range

Parameter	Description		-100		Unit
			Min	Max	
t_{PU}	Power-up time after all supplies reach minimum value		–	2	ms
t_S	Clock cycle frequency	3.3 V LVCMOS	24	100	MHz
t_S	Clock cycle frequency	1.8 V LVCMOS	24	100	MHz
tA	Data access time		–	10	ns
t_{CLK}	Clock cycle time		10	41.67	ns
t_{CLKH}	Clock high time		4.5	–	ns
t_{CLKL}	Clock low time		4.5	–	ns
t_{DS}	Data setup time		3	–	ns
t_{DH}	Data hold time		3	–	ns
t_{QS}	RQSEL and WQSEL setup time		3	–	ns
t_{QH}	RQSEL and WQSEL hold time		3	–	ns
t_{ENS}	Enable setup time		3	–	ns
t_{ENH}	Enable hold time		3	–	ns
t_{ENS_SI}	Setup time for SI and SEN in SPI mode		5	–	ns
t_{ENH_SI}	Hold time for SI and SEN in SPI mode		5	–	ns
t_{RATE_SPI}	Frequency of SCLK		–	25	MHz
t_{RS}	Reset pulse width		100	–	ns
t_{PZS}	Port size select to MRS setup time		25	–	ns
t_{PZH}	MRS to port size select hold time		25	–	ns
t_{RSF}	Reset to flag output time		–	50	ns
t_{PRT}	Retransmit pulse width		5	–	RCLK cycles
t_{OLZ}	Output enable to output in Low Z		4	15	ns
t_{OE}	Output enable to output valid		–	15	ns
t_{OHZ}	Output enable to output in High Z		–	15	ns
t_{WFF}	Write clock to $\overline{FF}$		–	9.5	ns
t_{REF}	Read clock to $\overline{EF}$		–	9.5	ns
t_{PLL}	Time required to synchronize PLL		–	1024	cycles
t_{RATE_JTAG}	JTAG TCK cycle time		100	–	ns
t_{S_JTAG}	Setup time for JTAG TMS,TDI		8	–	ns
t_{H_JTAG}	Hold time for JTAG TMS,TDI		8	–	ns
t_{CO_JTAG}	JTAG TCK low to TDO valid		–	20	ns

Switching Waveforms

Figure 7. Write Cycle Timing

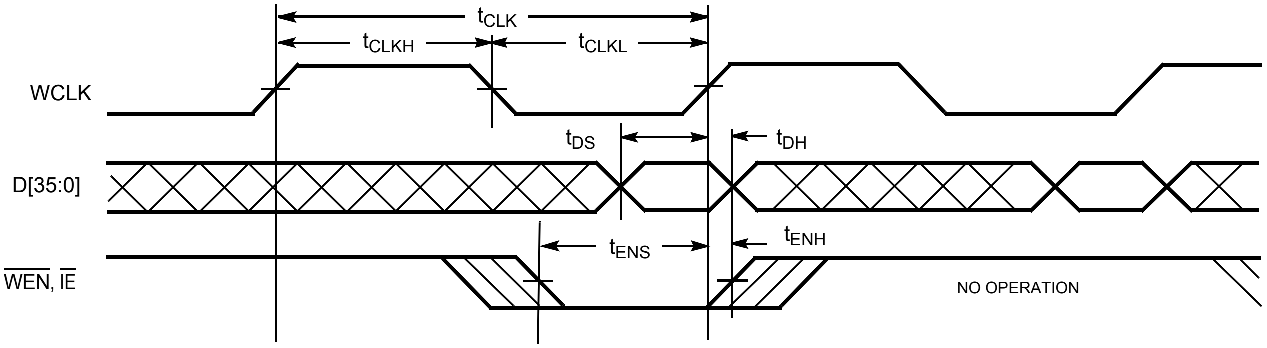


Figure 8. Read Cycle Timing

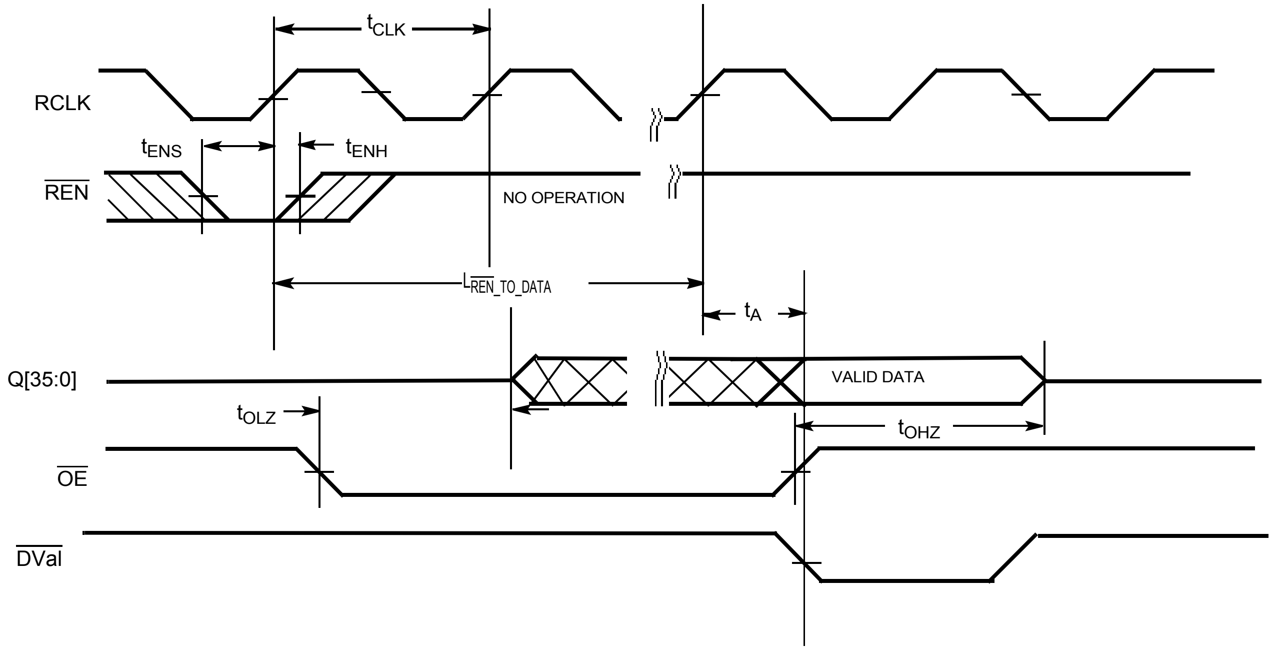
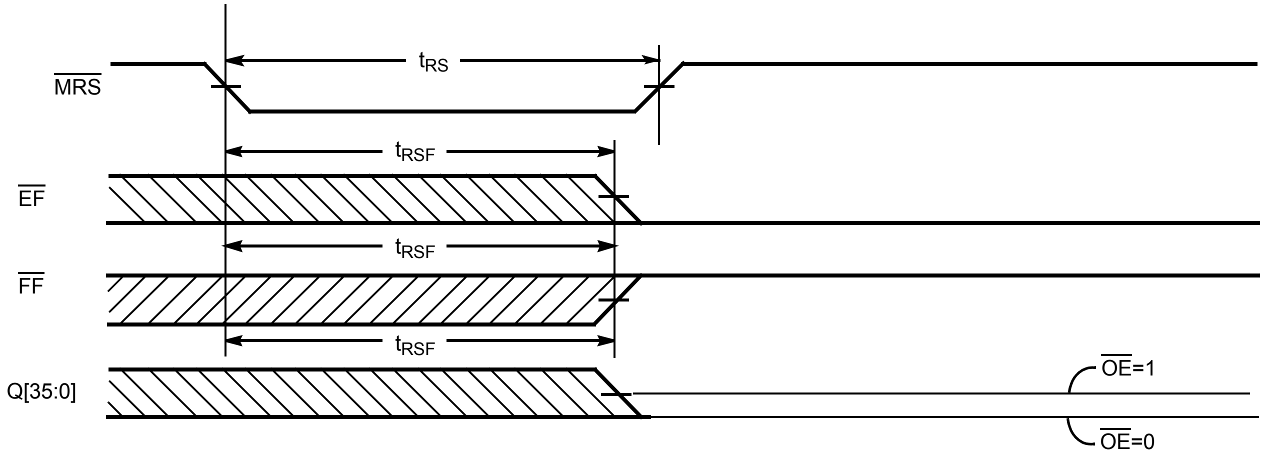


Figure 9. Reset Timing



Switching Waveforms (continued)

Figure 10. $\overline{\text{MRS}}$ to PORTSZ[2:0]

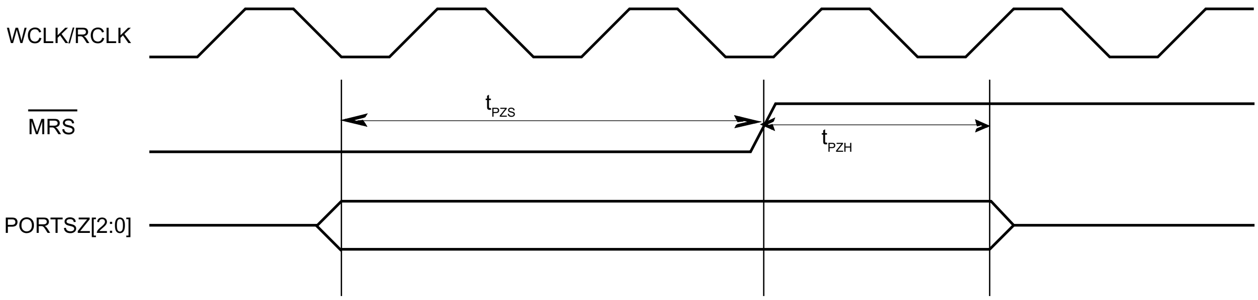
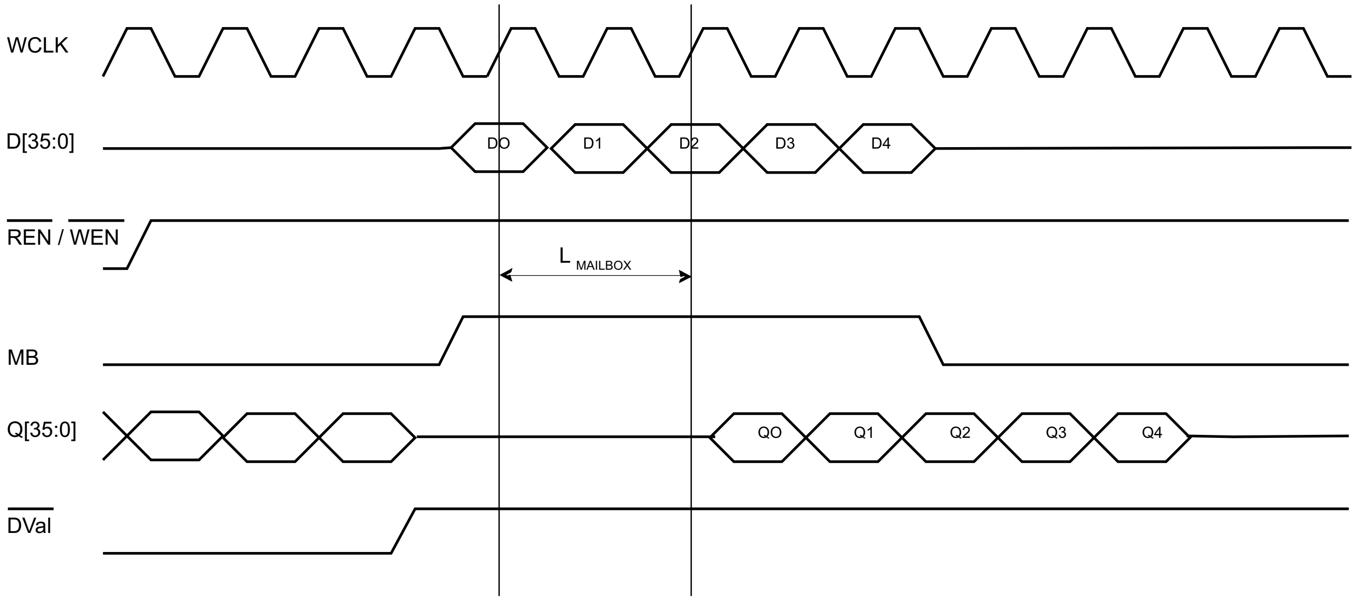


Figure 11. Flow-through mailbox Operation



Switching Waveforms (continued)

Figure 12. Configuration Register Write

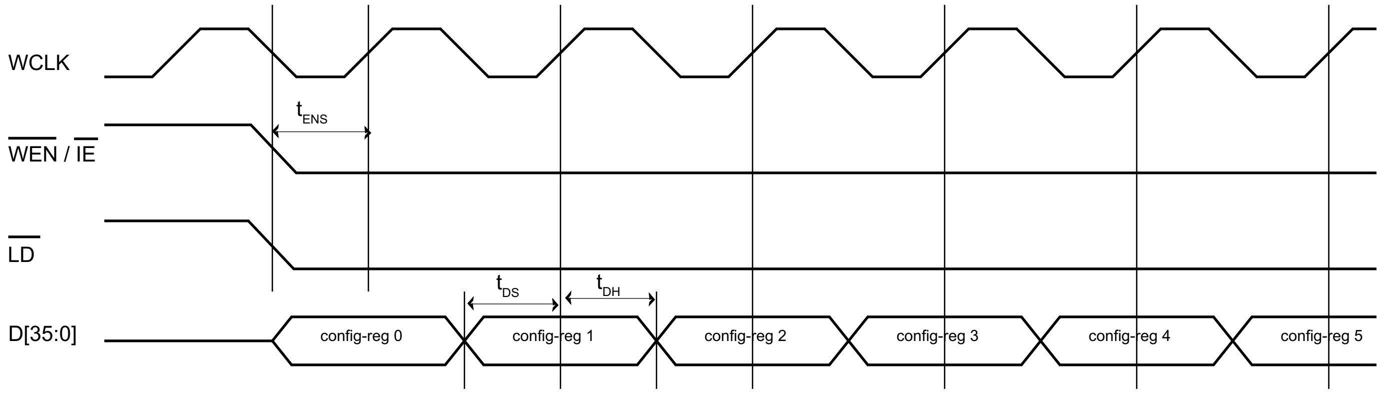


Figure 13. Configuration Register Read

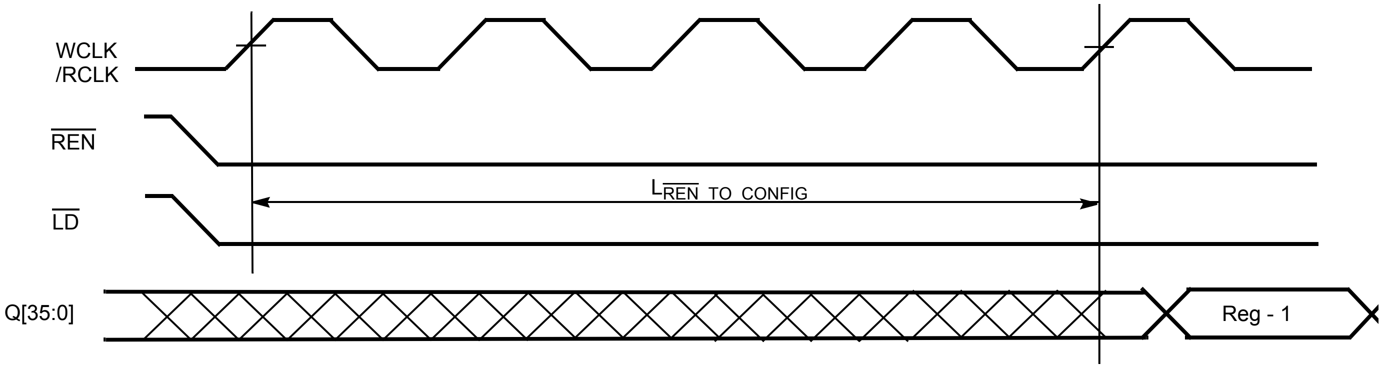
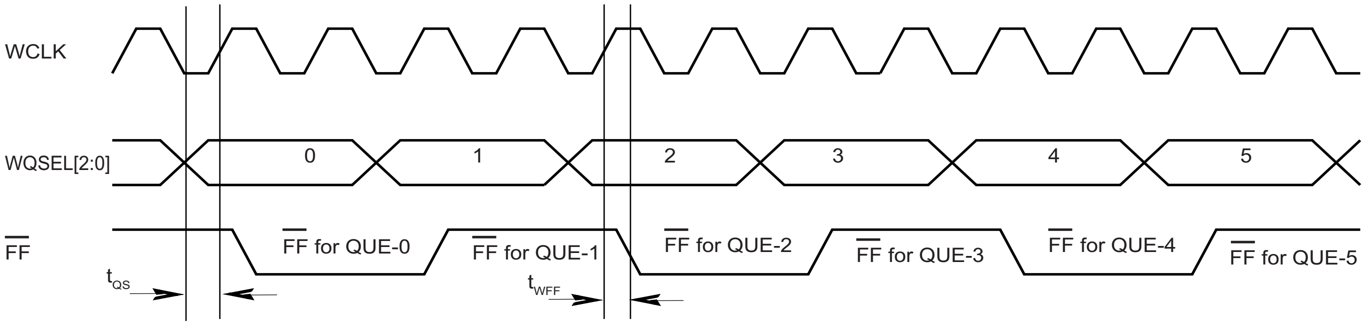


Figure 14. WQSEL to $\overline{FF}$



Switching Waveforms (continued)

Figure 15. RQSEL to $\overline{EF}$

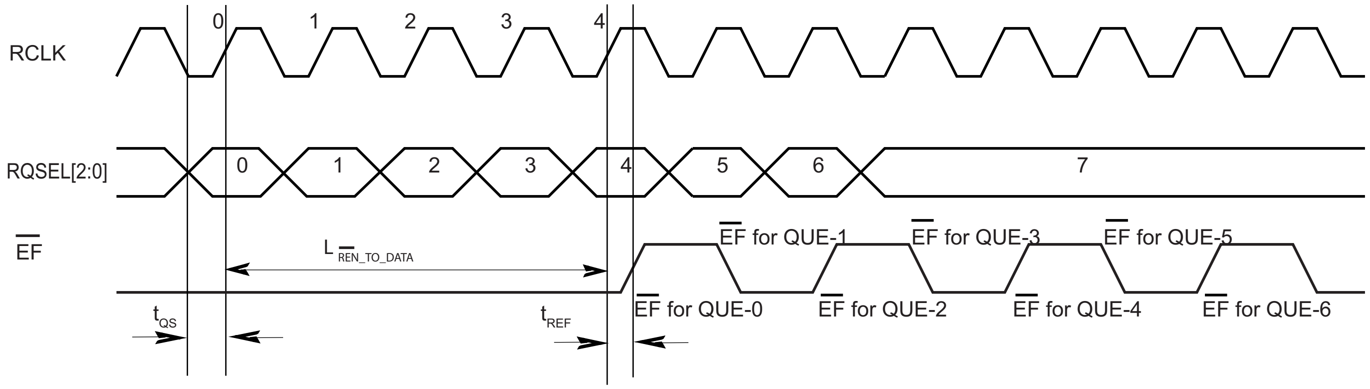
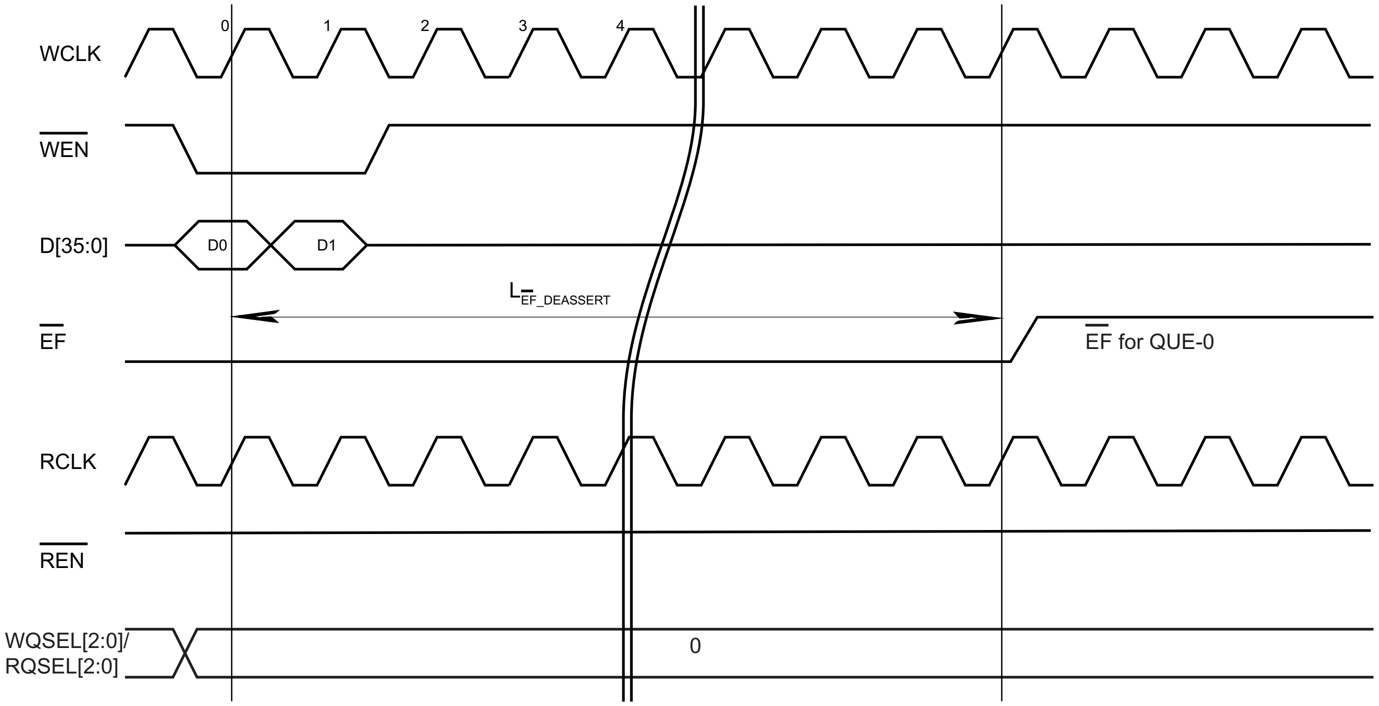

RCLK
0
1
2
3
4
RQSEL[2:0]
0
1
2
3
4
5
6
7
$\overline{EF}$
$L_{\overline{REN}\_TO\_DATA}$
t_{QS}
t_{REF}
$\overline{EF}$ for QUE-0
$\overline{EF}$ for QUE-1
$\overline{EF}$ for QUE-2
$\overline{EF}$ for QUE-3
$\overline{EF}$ for QUE-4
$\overline{EF}$ for QUE-5
$\overline{EF}$ for QUE-6

Figure 16. Write to Empty Flag De-assertion



Switching Waveforms (continued)

Figure 17. Read to Empty Flag Assertion

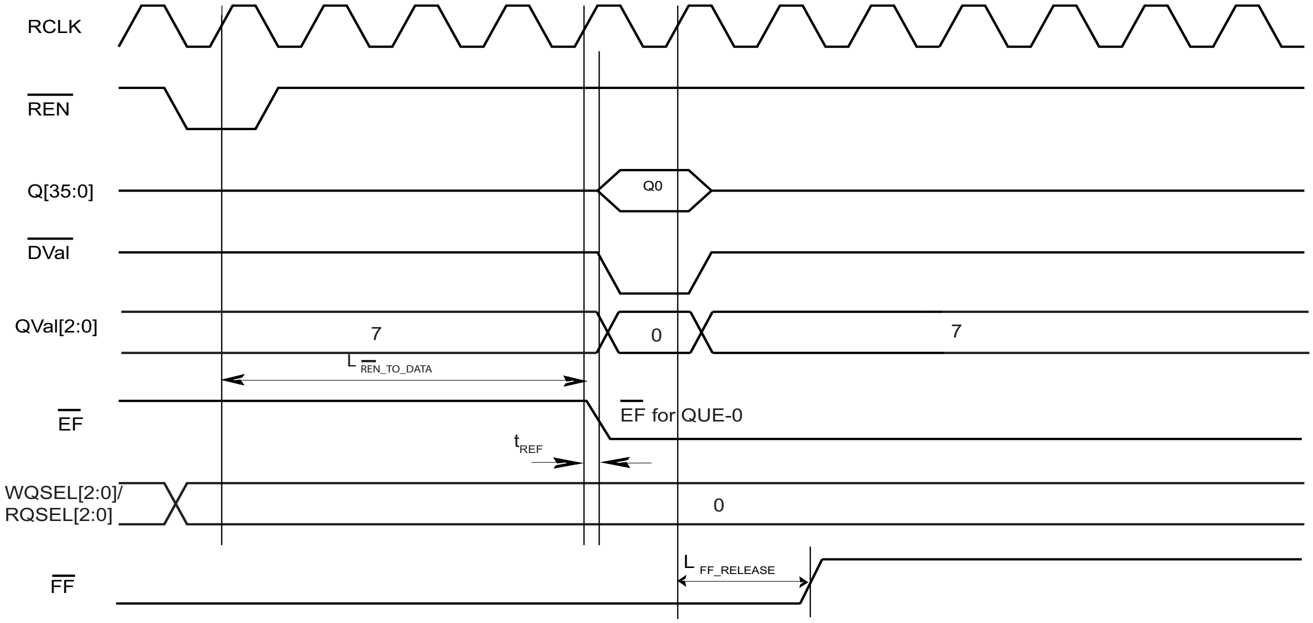
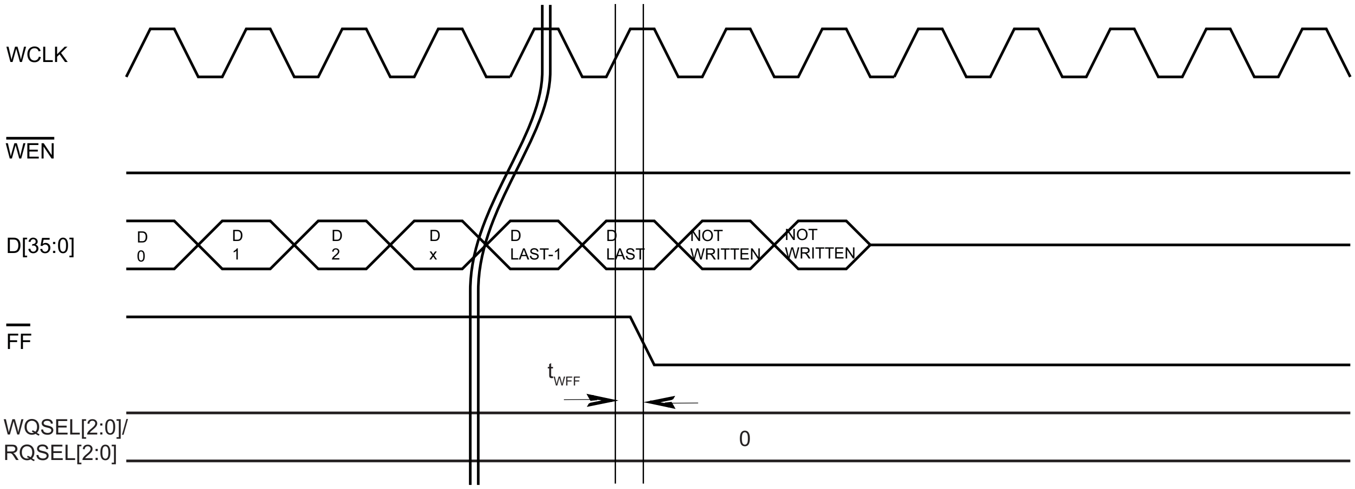


Figure 18. Full Flag Assertion



Switching Waveforms (continued)

Figure 19. Full Flag De-assertion

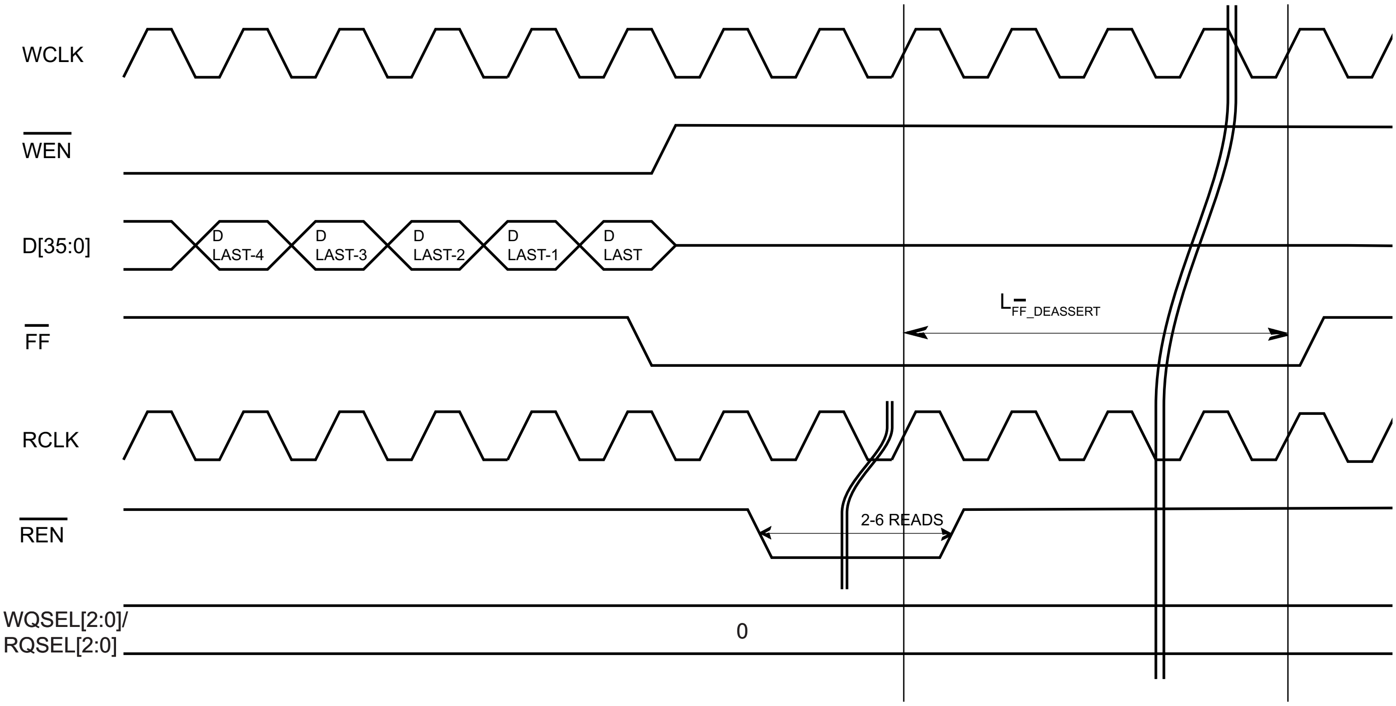
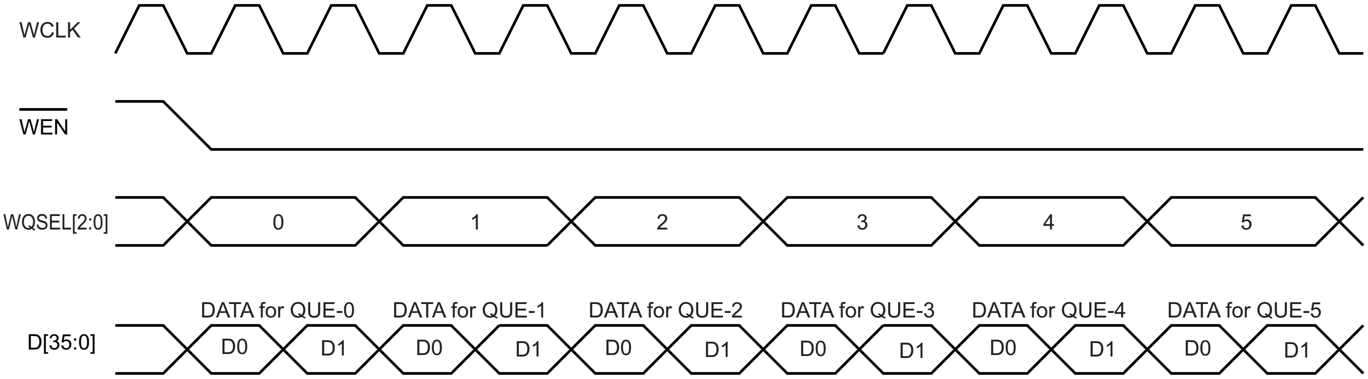
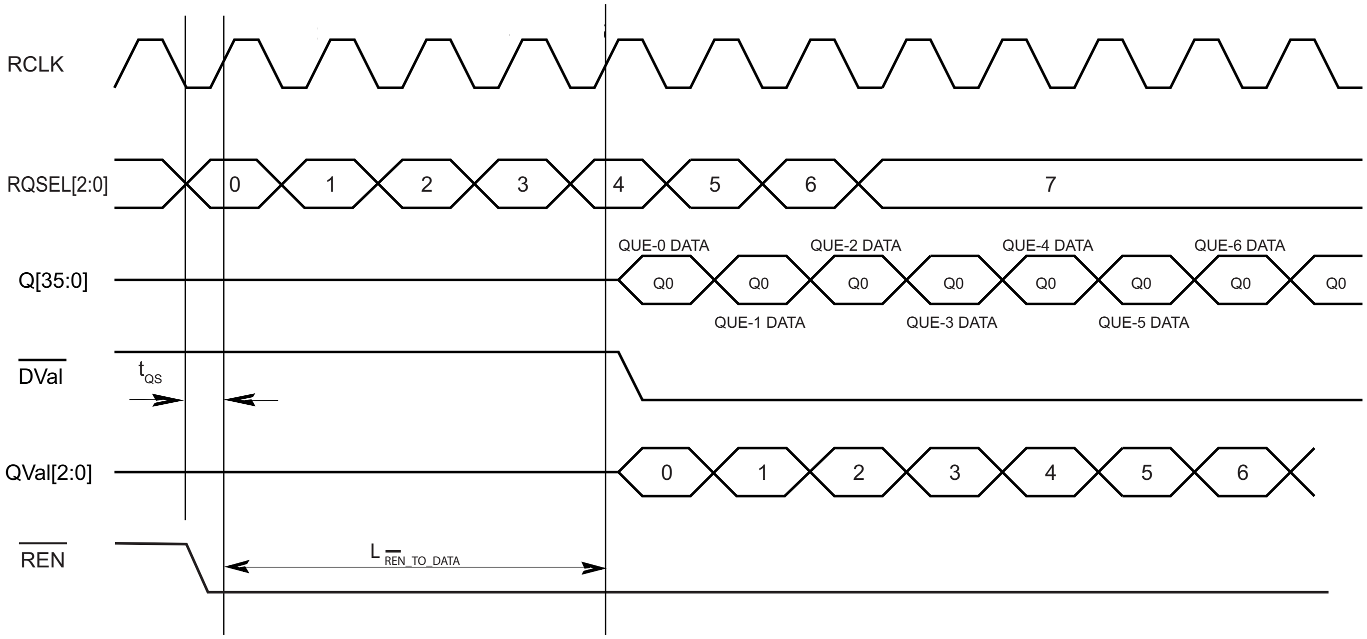


Figure 20. Switching between Queues - Write



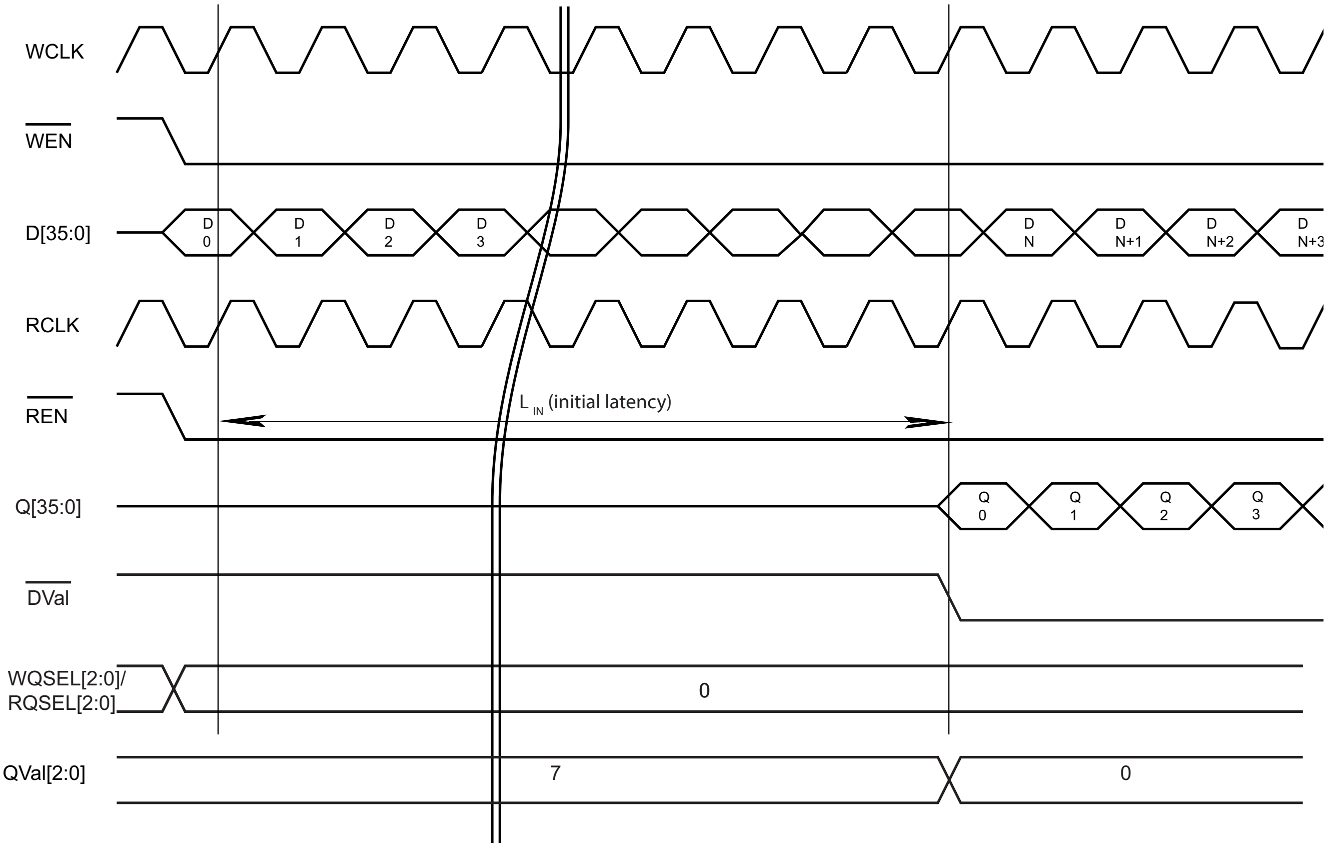
Switching Waveforms (continued)

Figure 21. Switching between Queues - Read



Switching Waveforms (continued)

Figure 22. Simultaneous Write & Read QUE - 0



Switching Waveforms (continued)

Figure 23. Mark

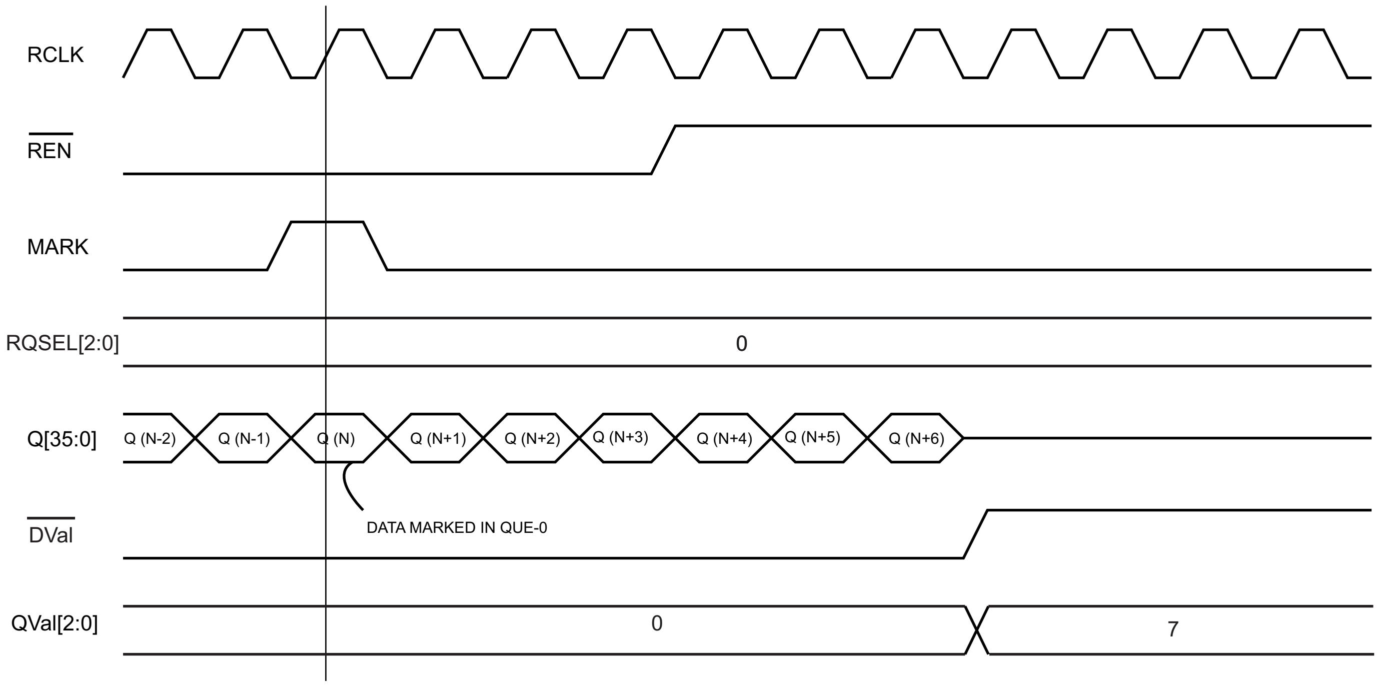
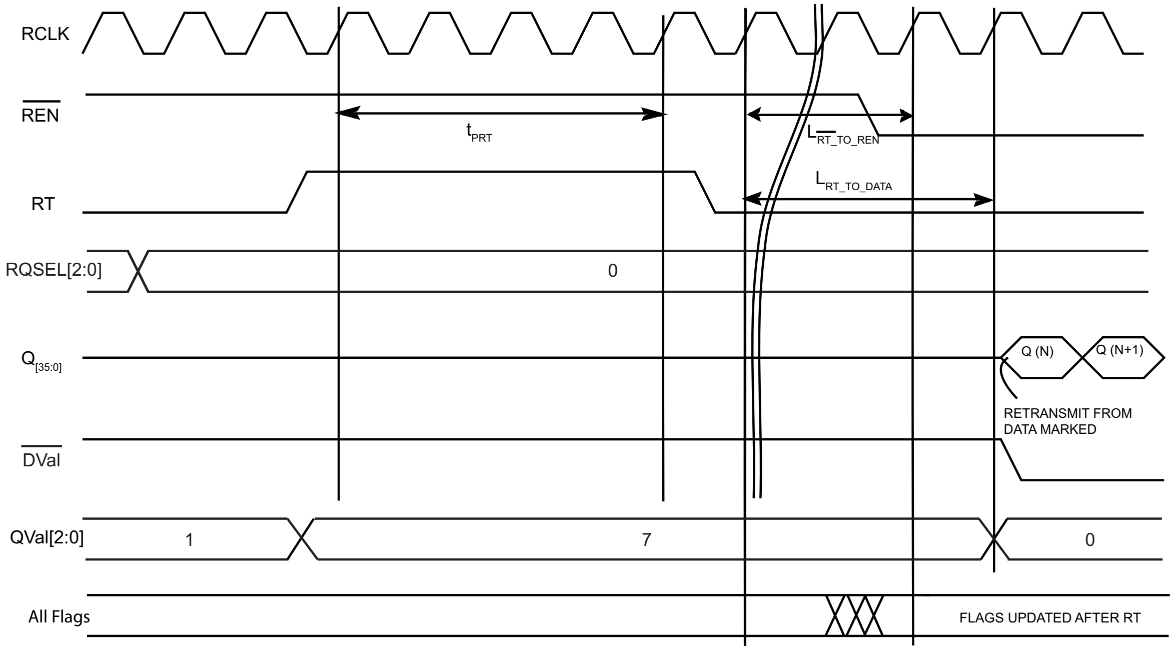


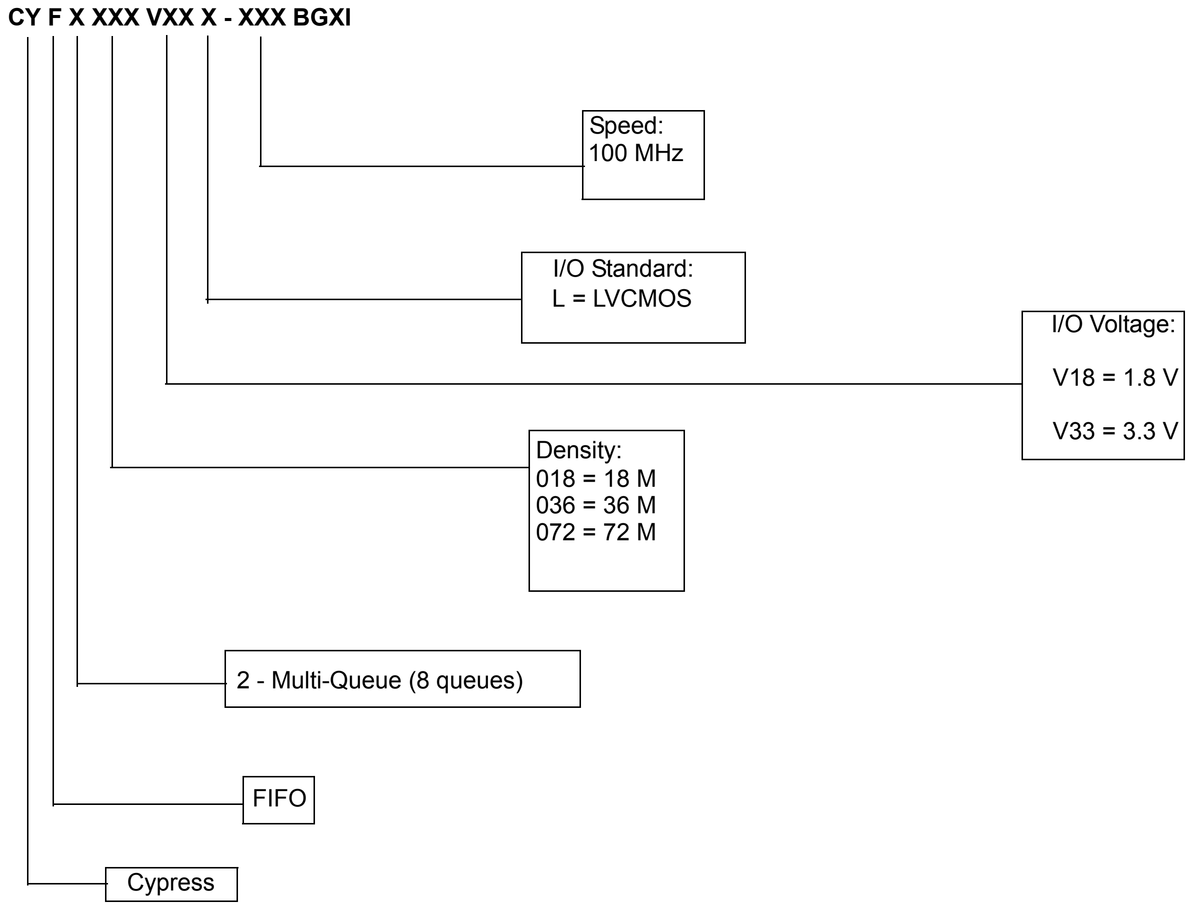
Figure 24. Retransmit



Ordering Information

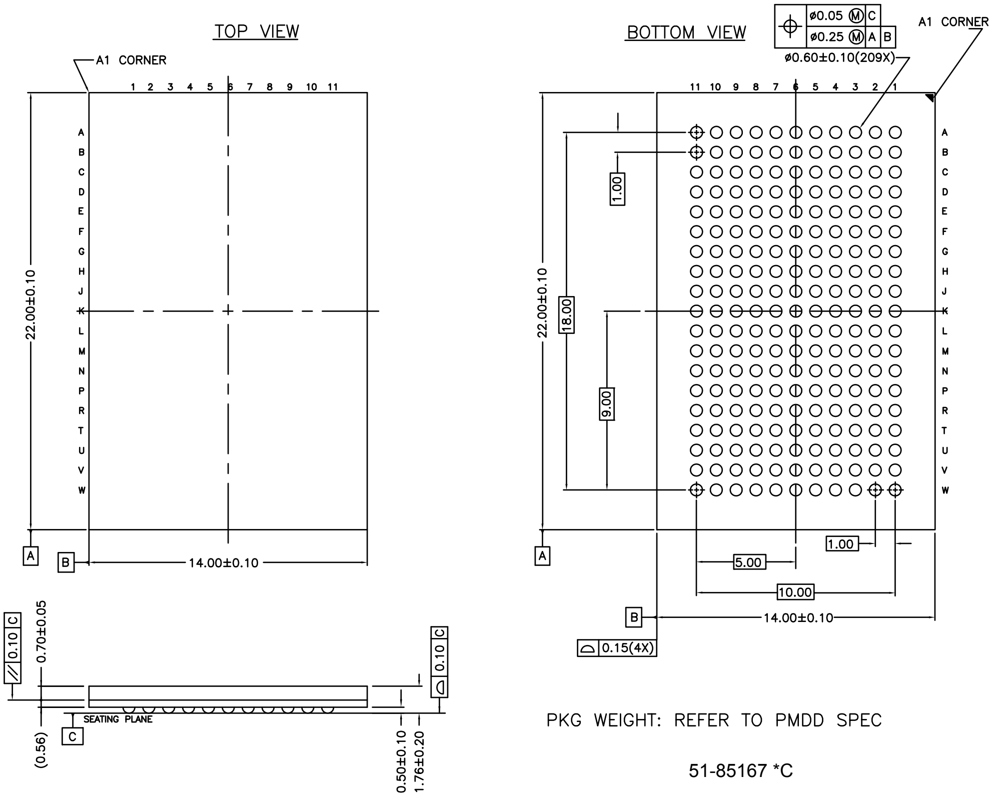
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
100	CYF2072V33L-100BGXI	51-85167	209-ball FBGA (14 × 22 × 1.76 mm)	Industrial

Ordering Code Definitions



Package Diagram

Figure 25. 209-ball FBGA (14 × 22 × 1.76 mm) BB209A Package Outline, 51-85167



Acronyms

Acronym	Description
$\overline{\text{EF}}$	Empty Flag
$\overline{\text{FF}}$	Full Flag
FIFO	First In First Out
$\overline{\text{IE}}$	Input Enable
I/O	Input/Output
FBGA	Fine-Pitch Ball Grid Array
JTAG	Joint Test Action Group
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MB	Mailbox
$\overline{\text{MRS}}$	Master Reset
$\overline{\text{OE}}$	Output Enable
$\overline{\text{REN}}$	Read Enable
RCLK	Read Clock
RQSEL	Read Queue Select
SCLK	Serial Clock
TDI	Test Data In
TDO	Test Data Out
TCK	Test Clock
TMS	Test Mode Select
WCLK	Write Clock
$\overline{\text{WEN}}$	Write Enable
WQSEL	Write Queue Select
QUE-0	Queue Number 0
QUE-1	Queue Number 1

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CYF2018V/CYF2036V/CYF2072V, 18/36/72-Mbit Programmable Multi-Queue FIFOs
Document Number: 001-68336

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3209860	SIVS	03/30/2011	New data sheet.
*A	3353401	AJU	08/26/2011	Updated Package Diagram.
*B	3387127	AJU	09/28/2011	Updated Pin Diagram for CYF2XXXVXXL (Added Note 2 and referred the same note in DNU in ball U6). Updated Multi-Queue Operation (Updated Table 4 (WCLK column in first row)). Updated Recommended DC Operating Conditions (Added Note 4 and referred the same note in Parameter column). Updated Switching Waveforms (Removed the clock cycle numbers in Figure 11, Figure 15, Figure 16, Figure 17, and Figure 21).
*C	3652368	ADMU	08/16/2012	Updated Pin Diagram for CYF2XXXVXXL (Updated Figure 1 (W9 ball marked as DNU)). Updated Figure 6.
*D	3997615	ADMU	05/11/2013	Updated Package Diagram: spec 51-85167 – Changed revision from *B to *C. Added Errata.
*E	4080484	ADMU	07/29/2013	Added Errata footnotes (Note 4, 7, 8, 9). Updated Pin Diagram for CYF2XXXVXXL: Added Note 1 and referred the same note in Figure 1. Updated Functional Description. Updated Logic Block Diagram. Updated Architecture. Updated Retransmit from Mark Operation: Added Note 4 and referred the same note in 3rd paragraph and 5th paragraph. Updated Programming Configuration Registers: Updated Table 2 (Changed value of Register 0x3 from “0x00” to “0x07” in the column “Default”). Updated Latency Table: Added Note 7 and referred the same note in the Latency parameter “$L_{\overline{FF}\_RELEASE}$”. Updated Switching Waveforms: Updated Figure 15, Figure 16, Figure 17, Figure 19, Figure 22, Figure 23, Figure 24. Added Note 6 and referred the same note in “$L_{\overline{FF}\_RELEASE}$” in Figure 17. Added Note 7and referred the same note in “All Flags” and “FLAGS UPDATED AFTER RT” in Figure 24. Updated Ordering Information (Updated part numbers). Updated in new template.
*F	4339515	ADMU	04/10/2014	No technical updates. Completing Sunset Review.
*G	4581652	ADMU	11/25/2014	Added related documentation hyperlink in page 1.
*H	5323855	ADMU	06/28/2016	Updated Logic Block Diagram. Updated Pin Diagram for CYF2XXXVXXL. Updated Pin Definitions. Updated JTAG Operation. Removed Errata section. Updated CY Logo and Sales Disclaimer.
*I	5379263	ADMU	07/29/2016	Updated Pin Diagram for CYF2XXXVXXL: Replaced TRST\ with DNU.
*J	5983421	AESATMP8	12/04/2017	Updated logo and Copyright.

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PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

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