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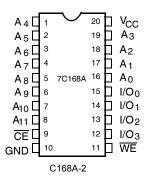
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Pin Configuration

Figure 1. DIP Top View



Selection Guide

| | | 7C168A-20 |
|--------------------------------|------------|-----------|
| Maximum access time (ns) | | 20 |
| Maximum operating current (mA) | Commercial | 90 |
| | Military | 100 |

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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| Output current into outputs (low) | 20 mA |
|--|----------|
| Static discharge voltage(per MIL-STD-883, method 3015) | > 2001 V |
| Latch-up current | > 200 mA |

Operating Range

| Range | Ambient Temperature | V _{cc} |
|------------|------------------------|-----------------|
| Commercial | 0 °C to +70 °C | 5 V \pm 10% |

Electrical Characteristics

Over the Operating Range

| | | | 7C16 | 8A-20 | |
|------------------|---|---|------|-----------------|------|
| Parameter | Description | Test Conditions | Min | Max | Unit |
| V _{OH} | Output HIGH voltage | V _{CC} = Min, I _{OH} = -4.0 mA | 2.4 | _ | V |
| V _{OL} | Output LOW voltage | V _{CC} = Min, I _{OL} = 8.0 mA | - | 0.4 | V |
| V _{IH} | Input HIGH voltage | | 2.2 | V _{CC} | V |
| V _{IL} | Input LOW voltage ^[1] | | -0.5 | 0.8 | V |
| I _{IX} | Input load current | $GND \le V_1 \le V_{CC}$ | -10 | +10 | μA |
| I _{OZ} | Output leakage current | $GND \le V_O \le V_{CC}$, output disabled | -10 | +10 | μA |
| Ios | Output short circuit current ^[2] | V _{CC} = Max, V _{OUT} = GND | - | -350 | mA |
| I _{CC} | V _{CC} operating supply current | V _{CC} = Max, I _{OUT} = 0 mA | - | 90 | mA |
| I _{SB1} | Automatic CE power-down current | Max V _{CC} , CE ≥ V _{IH} | - | 40 | mA |
| I _{SB2} | Automatic CE power-down current | Max V_{CC} , $\overline{CE} \ge V_{CC} - 0.3 \text{ V}$ | - | 20 | mA |

Notes

- 1. $V_{\rm IL}$ min = -3.0 V for pulse durations less than 30 ns.
- 2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

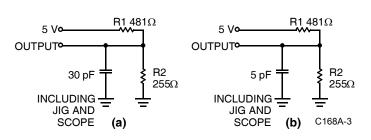
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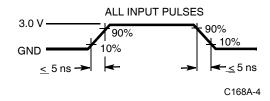


Capacitance^[3]

| Parameter | Description | Test Conditions | Max | Unit |
|------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | $T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = 5.0 \text{V}$ | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

167Ω OUTPUT• • 1.73 V

Note

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^{3.} Tested initially and after any design or process changes that may affect these parameters.

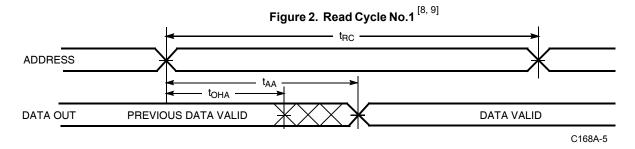


Switching Characteristics

Over the Operating Range^[4]

| Parameter | Description | 7C168 | 7C168A-20 | |
|-------------------|-------------------------------------|-------|-----------|------|
| Parameter | Description | Min. | Max. | Unit |
| READ CYC | LE | | | |
| t _{RC} | Read cycle time | 20 | _ | ns |
| t _{AA} | Address to data valid | _ | 20 | ns |
| t _{OHA} | Output hold from address change | 5 | _ | ns |
| t _{ACE} | CE LOW to data valid | _ | 20 | ns |
| t _{LZCE} | CE LOW to low Z ^[5] | 5 | _ | ns |
| t _{HZCE} | CE HIGH to high Z ^[5, 6] | _ | 8 | ns |
| t _{PU} | CE LOW to power-up | 0 | _ | ns |
| t _{PD} | CE HIGH to power-down | _ | 20 | ns |
| t _{RCS} | Read command set-up | 0 | _ | ns |
| t _{RCH} | Read command hold | 0 | _ | ns |
| WRITE CYC | CLE ^[7] | | | |
| t _{WC} | Write cycle time | 20 | _ | ns |
| t _{SCE} | CE LOW to write end | 15 | _ | ns |
| t _{AW} | Address set-up to write end | 15 | _ | ns |
| t _{HA} | Address hold from write end | 0 | _ | ns |
| t _{SA} | Address set-up to write start | 0 | _ | ns |
| t _{PWE} | WE pulse width | 15 | _ | ns |
| t _{SD} | Data set-up to write end | 10 | _ | ns |
| t _{HD} | Data hold from write end | 0 | _ | ns |
| t _{LZWE} | WE HIGH to low Z ^[5] | 7 | _ | ns |
| t _{HZWE} | WE LOW to high Z ^[5, 6] | 5 | _ | ns |

Switching Waveforms



Notes

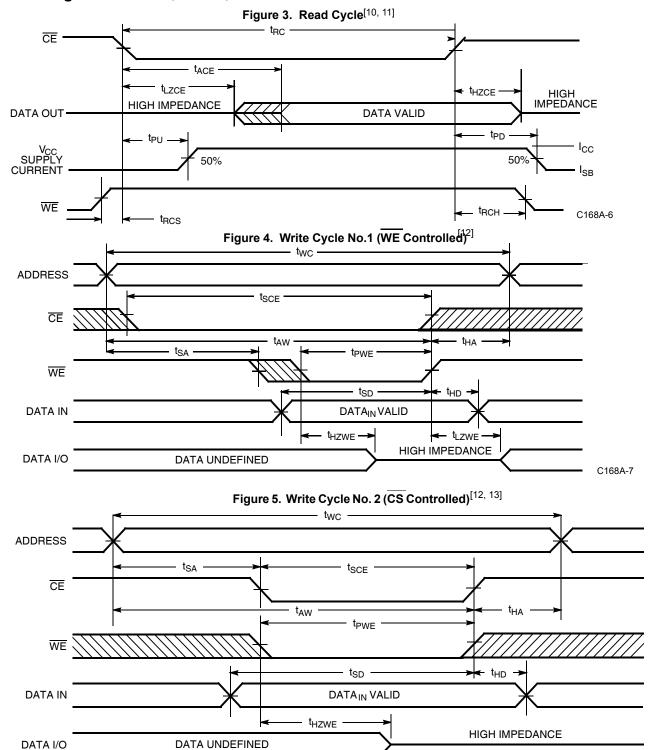
- 4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified log/loH and 30 pF load capacitance.
 5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.

- t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
 The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
 WE is HIGH for read cycle.
 Device is continuously selected, CE = V_{IL}.

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Switching Waveforms (continued)



- Notes

 10. WE is HIGH for read cycle.

 11. Address valid prior to or coincident with CE transition LOW.

 12. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

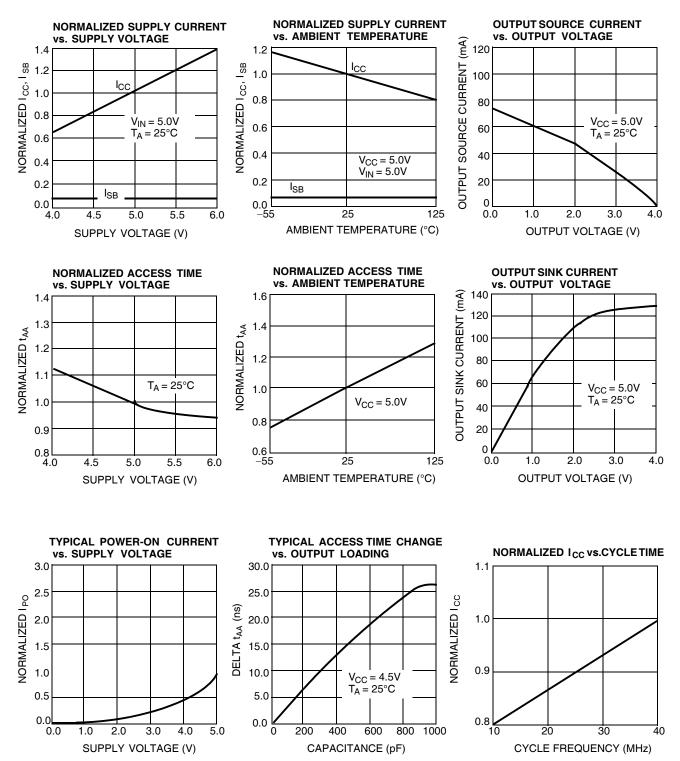
 13. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

[+] Feedback

C168A-8



Typical DC and AC Characteristics



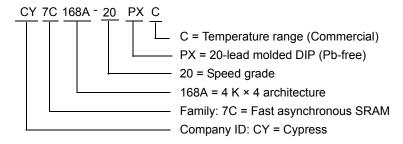
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Ordering Information

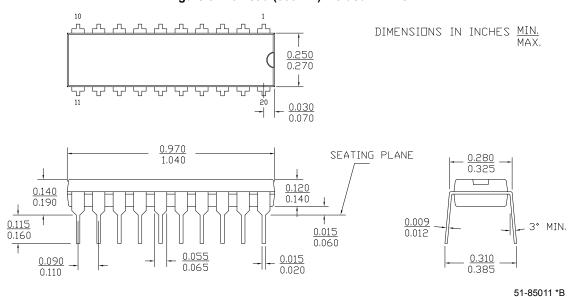
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---------------|----------------|-----------------|--------------------|--------------------|
| 20 | CY7C168A-20PXC | P5 | 20-Lead Molded DIP | Commercial |

Ordering Code Definitions



Package Diagram

Figure 6. 20-Lead (300-Mil) Molded DIP P5



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Acronyms

| Acronym | Description |
|---------|---|
| CMOS | complementary metal oxide semiconductor |
| CE | chip enable |
| DIP | dual inline package |
| I/O | input/output |
| SRAM | static random access memory |
| TTL | transistor-transistor logic |
| WE | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure | |
|--------|-----------------|--|
| ns | nano seconds | |
| V | Volts | |
| μΑ | micro Amperes | |
| mA | milli Amperes | |
| mV | milli Volts | |
| mW | milli Watts | |
| pF | pico Farad | |
| °C | degree Celcius | |
| W | Watts | |
| % | percent | |

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Document History Page

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|------|---------|------------|--------------------|---|
| ** | 106815 | 09/10/01 | SZV | Change from Spec number: 38-00095 to 38-05029 |
| *A | 3008799 | 08/19/2010 | AJU | Updated t _{AA} to 20 ns under High Speed, 495 mW under Low active power in Features section Updated Figure caption to DIP Top View in Pin Configuration section Updated Selection Guide section with only 7C168A-20 values Updated Operating Range section with only Commercial temperature range Updated Electrical Characteristics section with only 7C168A-20 values Updated Switching Characteristics section with only 7C168A-20 values Updated Ordering Information section with only CY7C168A-20PXC Ordering Code Updated Package Diagram with only the latest revision of "20-Lead (300-Mil) Molded DIP P5" (Figure 6 in page 8) Minor edits and updated in new template |
| *B | 3090588 | 11/19/2010 | AJU | Post to external web. |
| *C | 3097955 | 11/30/2010 | PRAS | No technical updates. Sunset review. |

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