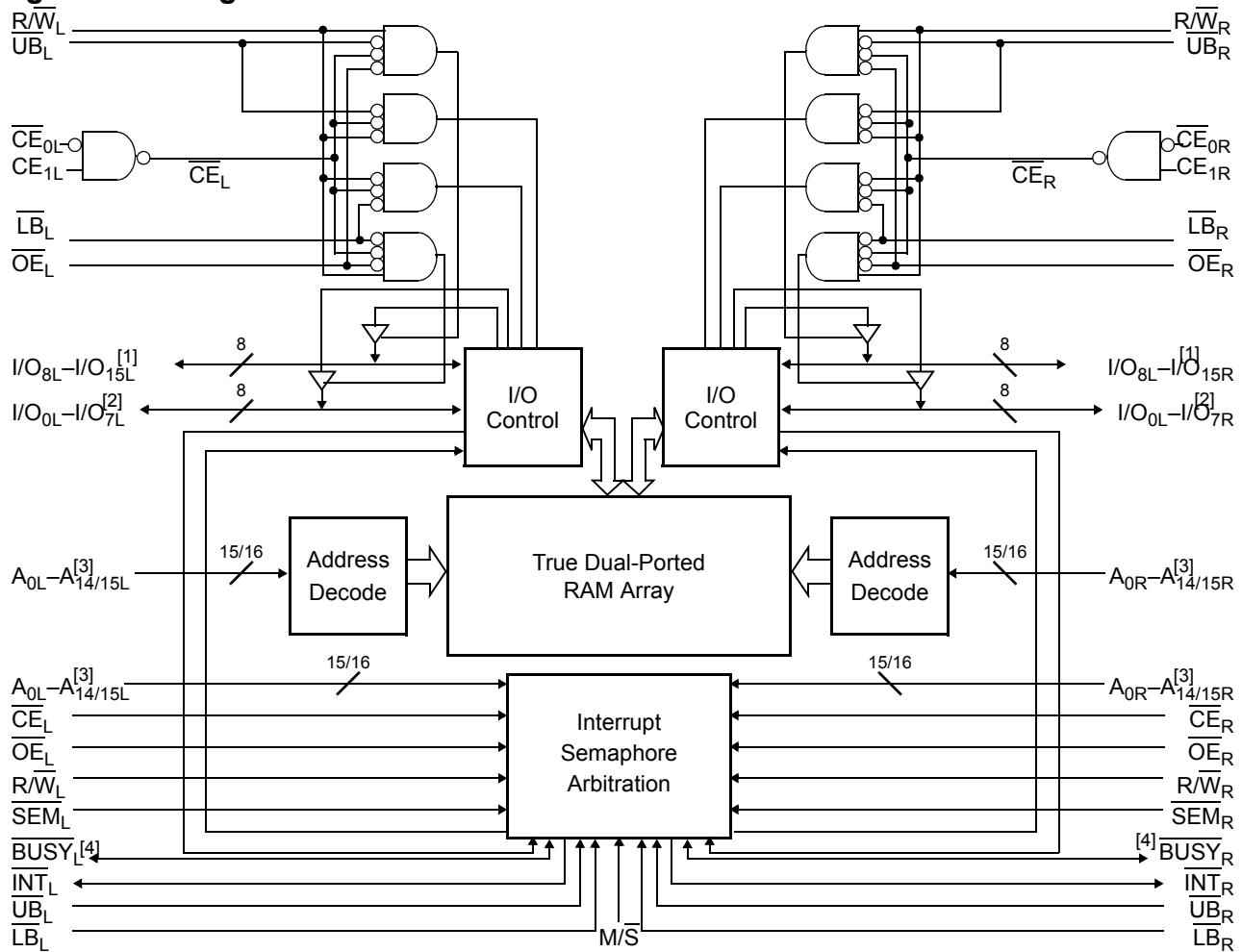


## Logic Block Diagram



### Notes

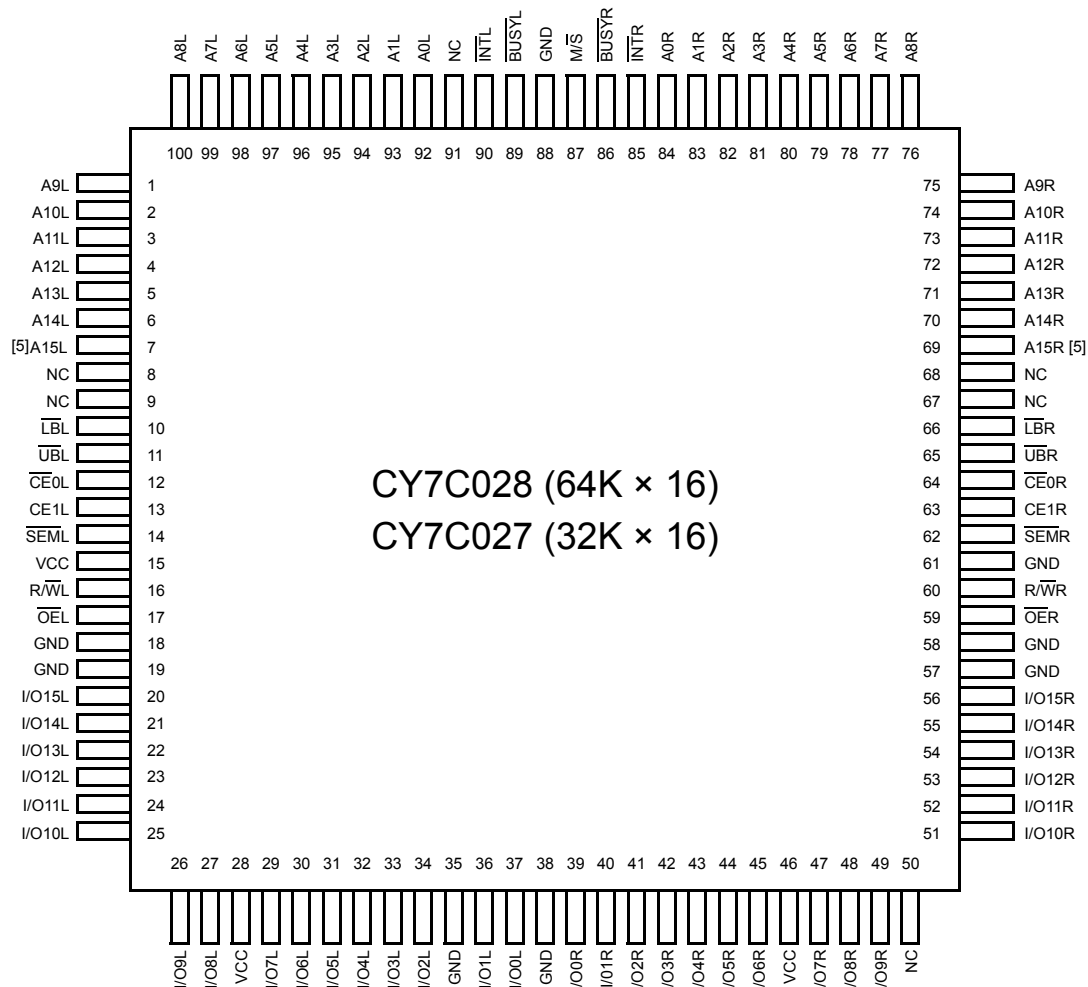
1.  $I/O_8-I/O_{15}$  for × 16 devices
2.  $I/O_0-I/O_7$  for × 16 devices
3.  $A_0-A_{14}$  for 32K;  $A_0-A_{15}$  for 64K devices.
4.  $BUSY$  is an output in master mode and an input in slave mode.

## Contents

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## Pin Configurations

Figure 1. 100-pin TQFP pinout (Top View)



**Note**

5. This pin is NC for CY7C027.

## Pin Definitions

| Left Port                     | Right Port                    | Description                                                                                      |
|-------------------------------|-------------------------------|--------------------------------------------------------------------------------------------------|
| $\overline{CE}_{0L}, CE_{1L}$ | $\overline{CE}_{0R}, CE_{1R}$ | Chip Enable ( $\overline{CE}$ is LOW when $\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$ ) |
| $R/W_L$                       | $R/W_R$                       | Read/Write Enable                                                                                |
| $\overline{OE}_L$             | $\overline{OE}_R$             | Output Enable                                                                                    |
| $A_{0L}-A_{15L}$              | $A_{0R}-A_{15R}$              | Address ( $A_0-A_{14}$ for 32K; $A_0-A_{15}$ for 64K devices)                                    |
| $I/O_{0L}-I/O_{15L}$          | $I/O_{0R}-I/O_{15R}$          | Data Bus Input/Output ( $I/O_0-I/O_{15}$ for $\times 16$ devices)                                |
| $SEM_L$                       | $SEM_R$                       | Semaphore Enable                                                                                 |
| $\overline{UB}_L$             | $\overline{UB}_R$             | Upper Byte Select ( $I/O_8-I/O_{15}$ for $\times 16$ devices)                                    |
| $\overline{LB}_L$             | $\overline{LB}_R$             | Lower Byte Select ( $I/O_0-I/O_7$ for $\times 16$ devices)                                       |
| $\overline{INT}_L$            | $\overline{INT}_R$            | Interrupt Flag                                                                                   |
| $BUSY_L$                      | $BUSY_R$                      | Busy Flag                                                                                        |
| $M/\overline{S}$              |                               | Master or Slave Select                                                                           |
| $V_{CC}$                      |                               | Power                                                                                            |
| GND                           |                               | Ground                                                                                           |
| NC                            |                               | No Connect                                                                                       |

## Maximum Ratings

Exceeding maximum ratings <sup>[6]</sup> may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature  
with Power Applied ..... -55 °C to +125 °C

Supply Voltage to Ground Potential ..... -0.3 V to +7.0 V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5 V to +7.0 V DC

Input Voltage <sup>[7]</sup> ..... -0.5 V to +7.0 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 1100V

Latch-Up Current ..... > 200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0 °C to +70 °C      | 5 V ± 10%       |
| Industrial | -40 °C to +85 °C    | 5 V ± 10%       |

## Electrical Characteristics

Over the Operating Range

| Symbol           | Parameter                                                                                 |            | CY7C027/CY7C028 |      |      |     |     |     | Unit |
|------------------|-------------------------------------------------------------------------------------------|------------|-----------------|------|------|-----|-----|-----|------|
|                  |                                                                                           |            | -15             |      |      | -20 |     |     |      |
|                  |                                                                                           |            | Min             | Typ  | Max  | Min | Typ | Max |      |
| V <sub>OH</sub>  | Output HIGH Voltage (V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA)                    |            | 2.4             | —    | —    | 2.4 | —   | —   | V    |
| V <sub>OL</sub>  | Output LOW Voltage (V <sub>CC</sub> = Min, I <sub>OH</sub> = +4.0 mA)                     |            | —               |      | 0.4  | —   |     | 0.4 | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                                                                        |            | 2.2             |      | —    | 2.2 |     | —   | V    |
| V <sub>IL</sub>  | Input LOW Voltage                                                                         |            | —               |      | 0.8  | —   |     | 0.8 | V    |
| I <sub>OZ</sub>  | Output Leakage Current                                                                    |            | −10             |      | 10   | −10 |     | 10  | μA   |
| I <sub>CC</sub>  | Operating Current<br>(V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA)<br>Outputs Disabled | Commercial | —               | 190  | 280  | —   | 180 | 265 | mA   |
|                  |                                                                                           | Industrial |                 | —    |      |     | 305 | 290 | mA   |
| I <sub>SB1</sub> | Commercial                                                                                | 50         |                 | 70   | 45   |     | 65  | mA  |      |
|                  | Industrial                                                                                | —          |                 | 60   | 80   |     | mA  |     |      |
| I <sub>SB2</sub> | Commercial                                                                                | 120        |                 | 180  | 110  |     | 160 | mA  |      |
|                  | Industrial                                                                                | —          |                 | 125  | 175  |     | mA  |     |      |
| I <sub>SB3</sub> | Commercial                                                                                | 0.05       |                 | 0.5  | 0.05 |     | 0.5 | mA  |      |
|                  | Industrial                                                                                | —          |                 | 0.05 | 0.5  |     | mA  |     |      |
| I <sub>SB4</sub> | Commercial                                                                                | 110        |                 | 160  | 100  |     | 140 | mA  |      |
|                  | Industrial                                                                                | —          |                 | 115  | 155  |     | mA  |     |      |

### Notes

6. The voltage on any input or I/O pin cannot exceed the power pin during power up.

7. Pulse width < 20 ns.

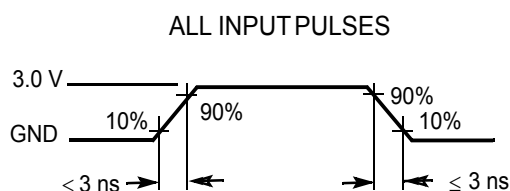
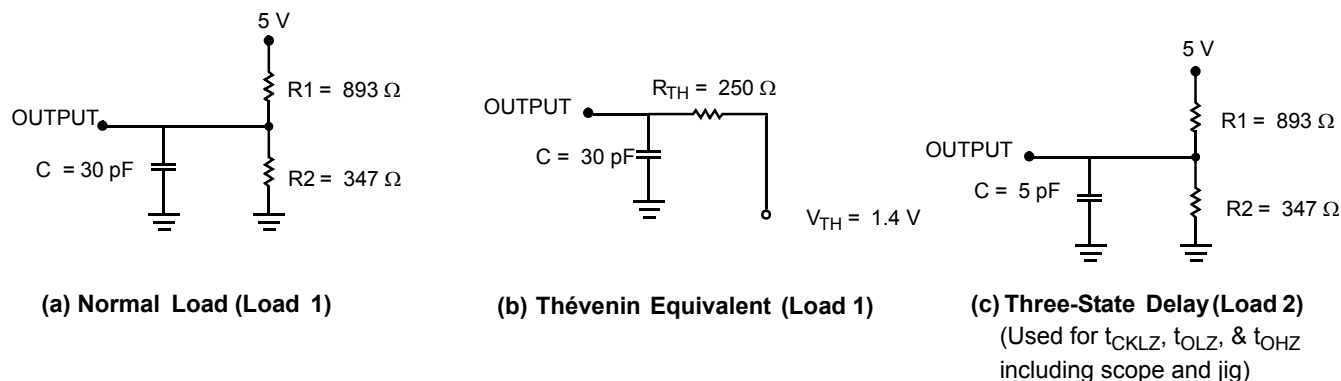
8. f<sub>MAX</sub> = 1/t<sub>RC</sub> = All inputs cycling at f = 1/t<sub>RC</sub> (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I<sub>SB3</sub>.

## Capacitance

| Parameter <sup>[9]</sup> | Description        | Test Conditions                                                         | Max | Unit |
|--------------------------|--------------------|-------------------------------------------------------------------------|-----|------|
| $C_{IN}$                 | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$ | 10  | pF   |
| $C_{OUT}$                | Output Capacitance |                                                                         | 10  | pF   |

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

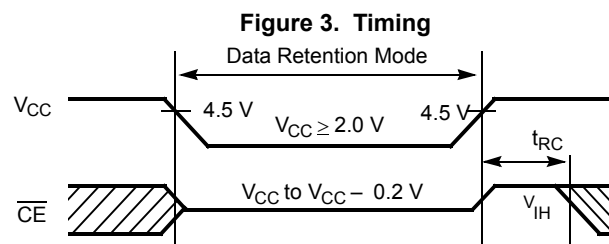


## Data Retention Mode

The CY7C027 and CY7C028 are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip enable ( $\overline{CE}$ ) must be held HIGH during data retention, within  $V_{CC}$  to  $V_{CC} - 0.2\text{ V}$ .
2.  $\overline{CE}$  must be kept between  $V_{CC} - 0.2\text{ V}$  and 70% of  $V_{CC}$  during the power up and power down transitions.
3. The RAM can begin operation  $> t_{RC}$  after  $V_{CC}$  reaches the minimum operating voltage (4.5 V).

## Timing



| Parameter      | Test Conditions <sup>[10]</sup> | Max | Unit |
|----------------|---------------------------------|-----|------|
| $I_{CC_{DR1}}$ | At $V_{CC_{DR}} = 2\text{ V}$   | 1.5 | mA   |

### Notes

9. Tested initially and after any design or process changes that may affect these parameters.
10.  $CE = V_{CC}$ ,  $V_{IN} = \text{GND}$  to  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$ . This parameter is guaranteed but not tested.

## Switching Characteristics

Over the Operating Range

| Parameter <sup>[11]</sup>                 | Description                         | CY7C027/CY7C028 |     |     |     | Unit |
|-------------------------------------------|-------------------------------------|-----------------|-----|-----|-----|------|
|                                           |                                     | -15             |     | -20 |     |      |
|                                           |                                     | Min             | Max | Min | Max |      |
| Read Cycle                                |                                     |                 |     |     |     |      |
| t <sub>RC</sub>                           | Read Cycle Time                     | 15              | –   | 20  | –   | ns   |
| t <sub>AA</sub>                           | Address to Data Valid               | –               | 15  | –   | 20  | ns   |
| t <sub>OHA</sub>                          | Output Hold From Address Change     | 3               | –   | 3   | –   | ns   |
| t <sub>ACE</sub> <sup>[12]</sup>          | $\overline{CE}$ LOW to Data Valid   | –               | 15  | –   | 20  | ns   |
| t <sub>DOE</sub>                          | $\overline{OE}$ LOW to Data Valid   | –               | 10  | –   | 12  | ns   |
| t <sub>LZOE</sub> <sup>[13, 14, 15]</sup> | $\overline{OE}$ LOW to Low Z        | 3               | –   | 3   | –   | ns   |
| t <sub>HZOE</sub> <sup>[13, 14, 15]</sup> | $\overline{OE}$ HIGH to High Z      | –               | 10  | –   | 12  | ns   |
| t <sub>LZCE</sub> <sup>[13, 14, 15]</sup> | $\overline{CE}$ LOW to Low Z        | 3               | –   | 3   | –   | ns   |
| t <sub>HZCE</sub> <sup>[13, 14, 15]</sup> | $\overline{CE}$ HIGH to High Z      | –               | 10  | –   | 12  | ns   |
| t <sub>PU</sub> <sup>[15]</sup>           | $\overline{CE}$ LOW to Power Up     | 0               | –   | 0   | –   | ns   |
| t <sub>PD</sub> <sup>[15]</sup>           | $\overline{CE}$ HIGH to Power Down  | –               | 15  | –   | 20  | ns   |
| t <sub>ABE</sub> <sup>[12]</sup>          | Byte Enable Access Time             | –               | 15  | –   | 20  | ns   |
| Write Cycle                               |                                     |                 |     |     |     |      |
| t <sub>WC</sub>                           | Write Cycle Time                    | 15              | –   | 20  | –   | ns   |
| t <sub>SCE</sub> <sup>[12]</sup>          | $\overline{CE}$ LOW to Write End    | 12              | –   | 15  | –   | ns   |
| t <sub>AW</sub>                           | Address Valid to Write End          | 12              | –   | 15  | –   | ns   |
| t <sub>HA</sub>                           | Address Hold From Write End         | 0               | –   | 0   | –   | ns   |
| t <sub>SA</sub> <sup>[12]</sup>           | Address Setup to Write Start        | 0               | –   | 0   | –   | ns   |
| t <sub>PWE</sub>                          | Write Pulse Width                   | 12              | –   | 15  | –   | ns   |
| t <sub>SD</sub>                           | Data Setup to Write End             | 10              | –   | 15  | –   | ns   |
| t <sub>HD</sub>                           | Data Hold From Write End            | 0               | –   | 0   | –   | ns   |
| t <sub>HZWE</sub> <sup>[14, 15]</sup>     | R/ $\overline{W}$ LOW to High Z     | –               | 10  | –   | 12  | ns   |
| t <sub>LZWE</sub> <sup>[14, 15]</sup>     | R/ $\overline{W}$ HIGH to Low Z     | 3               | –   | 3   | –   | ns   |
| t <sub>WDD</sub> <sup>[16]</sup>          | Write Pulse to Data Delay           | –               | 30  | –   | 45  | ns   |
| t <sub>DDD</sub> <sup>[16]</sup>          | Write Data Valid to Read Data Valid | –               | 25  | –   | 30  | ns   |

### Notes

11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
12. To access RAM,  $\overline{CE} = L$ ,  $\overline{UB} = L$ ,  $\overline{SEM} = H$ . To access semaphore,  $\overline{CE} = H$  and  $\overline{SEM} = L$ . Either condition must be valid for the entire  $t_{SCE}$  time.
13. At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
14. Test conditions used are Load 2.
15. This parameter is guaranteed by design, but it is not production tested.
16. For information on port-to-port delay through RAM cells from writing port to reading port, refer to [Figure 11 on page 13](#).

## Switching Characteristics (continued)

Over the Operating Range

| Parameter <sup>[11]</sup>        | Description                                                   | CY7C027/CY7C028 |     |     |     | Unit |
|----------------------------------|---------------------------------------------------------------|-----------------|-----|-----|-----|------|
|                                  |                                                               | -15             |     | -20 |     |      |
|                                  |                                                               | Min             | Max | Min | Max |      |
| Busy Timing <sup>[17]</sup>      |                                                               |                 |     |     |     |      |
| t <sub>BLA</sub>                 | BUSY LOW from Address Match                                   | –               | 15  | –   | 20  | ns   |
| t <sub>BHA</sub>                 | BUSY HIGH from Address Mismatch                               | –               | 15  | –   | 20  | ns   |
| t <sub>BLC</sub>                 | BUSY LOW from $\overline{CE}$ LOW                             | –               | 15  | –   | 20  | ns   |
| t <sub>BHC</sub>                 | BUSY HIGH from $\overline{CE}$ HIGH                           | –               | 15  | –   | 17  | ns   |
| t <sub>PS</sub>                  | Port Setup for Priority                                       | 5               | –   | 5   | –   | ns   |
| t <sub>WB</sub>                  | R/ $\overline{W}$ HIGH after BUSY (Slave)                     | 0               | –   | 0   | –   | ns   |
| t <sub>WH</sub>                  | R/ $\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)   | 13              | –   | 15  | –   | ns   |
| t <sub>BDD</sub> <sup>[18]</sup> | BUSY HIGH to Data Valid                                       | –               | 15  | –   | 20  | ns   |
| Interrupt Timing <sup>[17]</sup> |                                                               |                 |     |     |     |      |
| t <sub>INS</sub>                 | $\overline{INT}$ Set Time                                     | –               | 15  | –   | 20  | ns   |
| t <sub>INR</sub>                 | $\overline{INT}$ Reset Time                                   | –               | 15  | –   | 20  | ns   |
| Semaphore Timing                 |                                                               |                 |     |     |     |      |
| t <sub>SOP</sub>                 | SEM Flag Update Pulse ( $\overline{OE}$ or $\overline{SEM}$ ) | 10              | –   | 10  | –   | ns   |
| t <sub>SWRD</sub>                | SEM Flag Write to Read Time                                   | 5               | –   | 5   | –   | ns   |
| t <sub>SPS</sub>                 | SEM Flag Contention Window                                    | 5               | –   | 5   | –   | ns   |
| t <sub>SAA</sub>                 | SEM Address Access Time                                       | –               | 15  | –   | 20  | ns   |

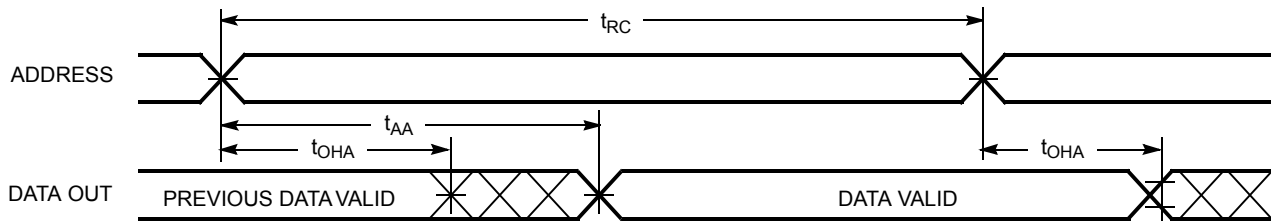
### Notes

17. Test conditions used are Load 1.

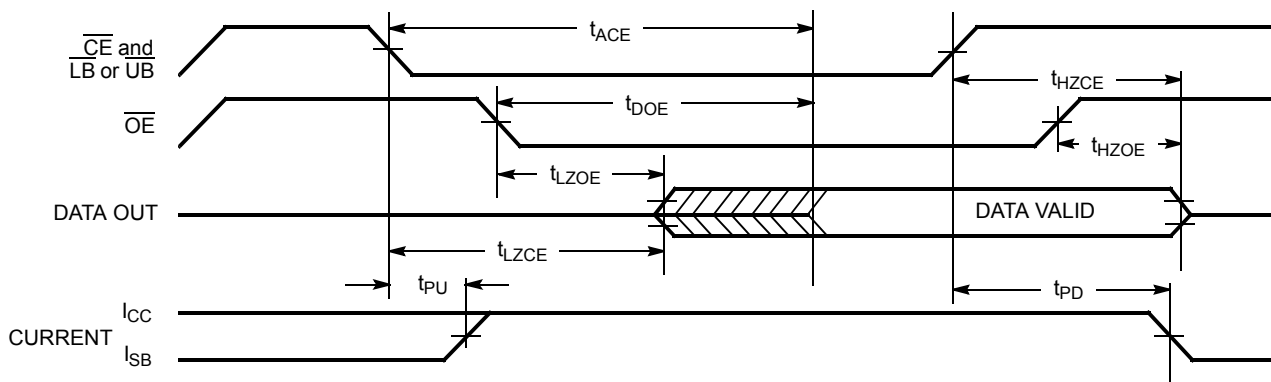
18. t<sub>BDD</sub> is a calculated parameter and is the greater of t<sub>WDD</sub>–t<sub>PWE</sub> (actual) or t<sub>DD</sub>–t<sub>SD</sub> (actual).

## Switching Waveforms

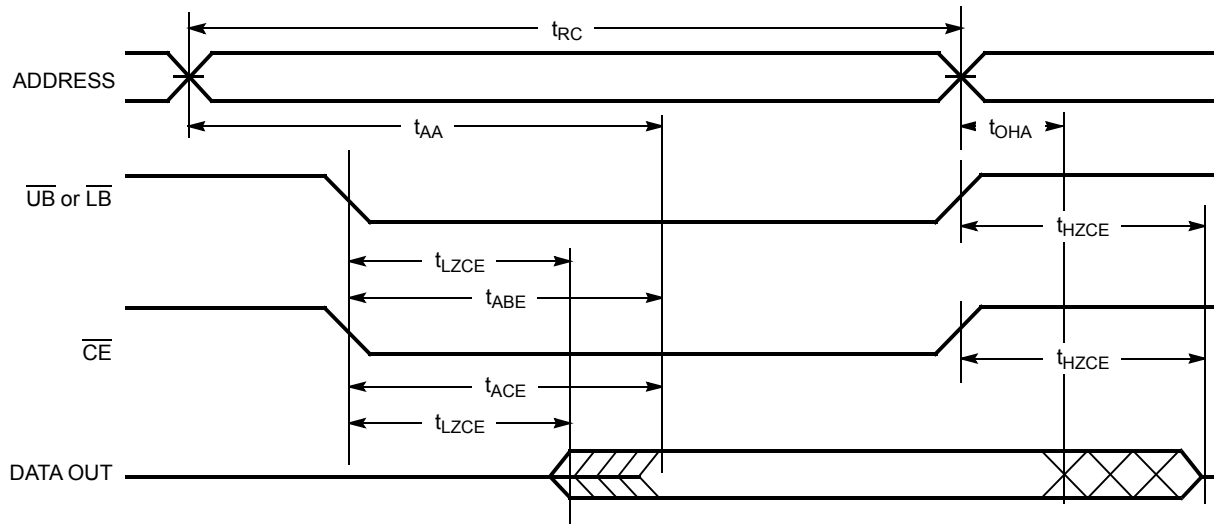
**Figure 4. Read Cycle No. 1 (Either Port Address Access)** [19, 20, 21]



**Figure 5. Read Cycle No. 2 (Either Port  $\overline{\text{CE}}/\overline{\text{OE}}$  Access)** [19, 22, 23]



**Figure 6. Read Cycle No. 3 (Either Port)** [19, 21, 22, 23]

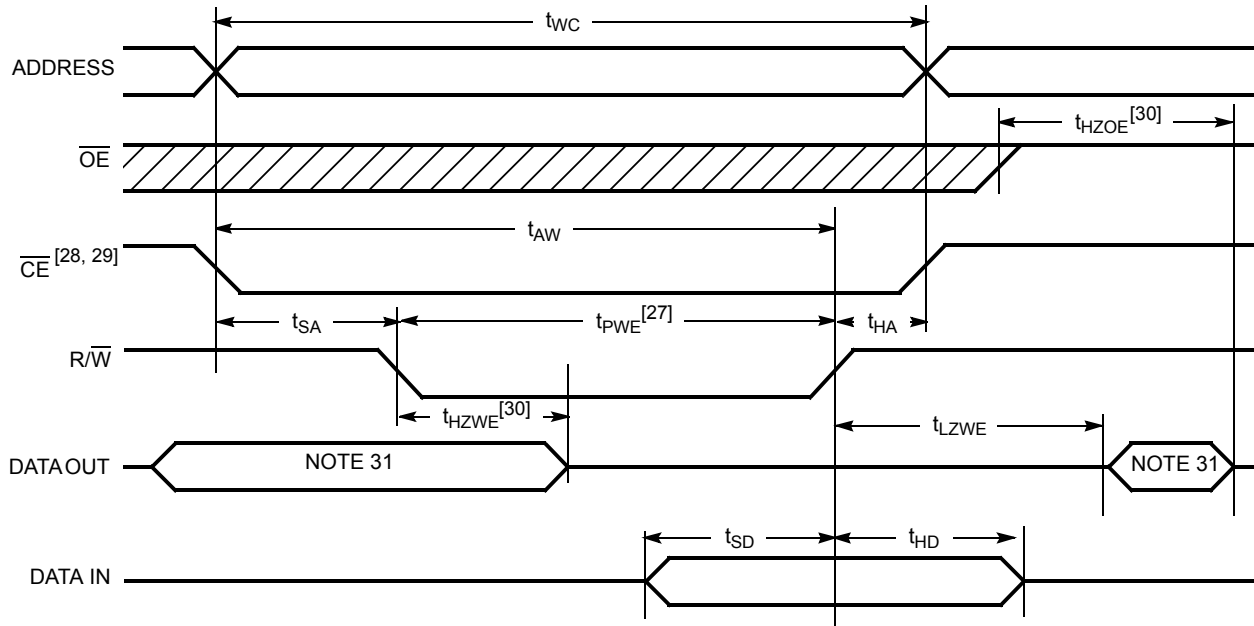


### Notes

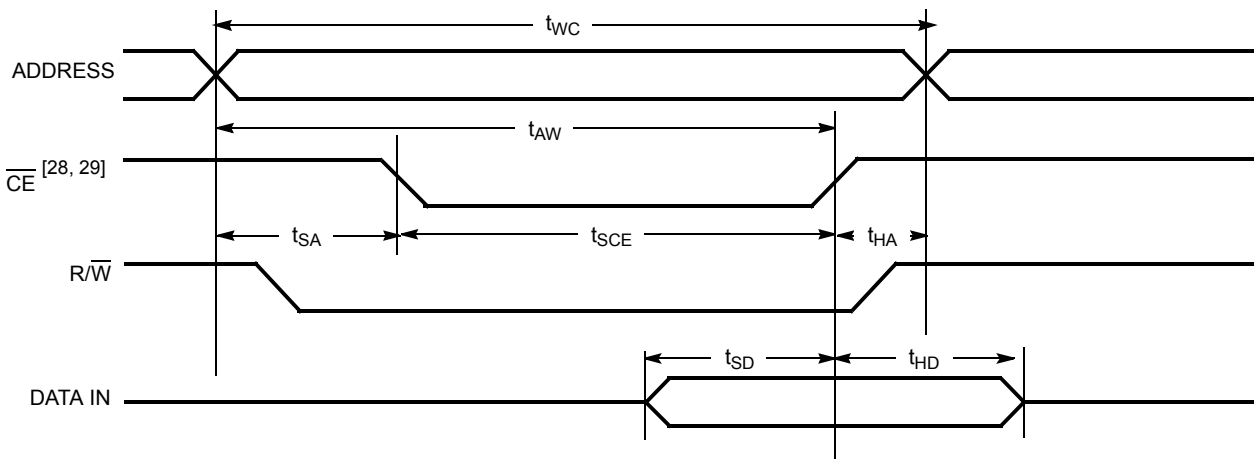
19.  $\overline{\text{R}}/\overline{\text{W}}$  is HIGH for read cycles.
20. Device is continuously selected  $\overline{\text{CE}} = \text{V}_{\text{IL}}$  and  $\overline{\text{UB}}$  or  $\overline{\text{LB}} = \text{V}_{\text{IL}}$ . This waveform cannot be used for semaphore reads.
21.  $\overline{\text{OE}} = \text{V}_{\text{IL}}$ .
22. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
23. To access RAM,  $\overline{\text{CE}} = \text{V}_{\text{IL}}$ ,  $\overline{\text{UB}}$  or  $\overline{\text{LB}} = \text{V}_{\text{IL}}$ ,  $\overline{\text{SEM}} = \text{V}_{\text{IH}}$ . To access semaphore,  $\overline{\text{CE}} = \text{V}_{\text{IH}}$ ,  $\overline{\text{SEM}} = \text{V}_{\text{IL}}$ .

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 (R/W Controlled Timing)** [24, 25, 26, 27]



**Figure 8. Write Cycle No. 2 (CE Controlled Timing)** [24, 25, 26, 31, 32]

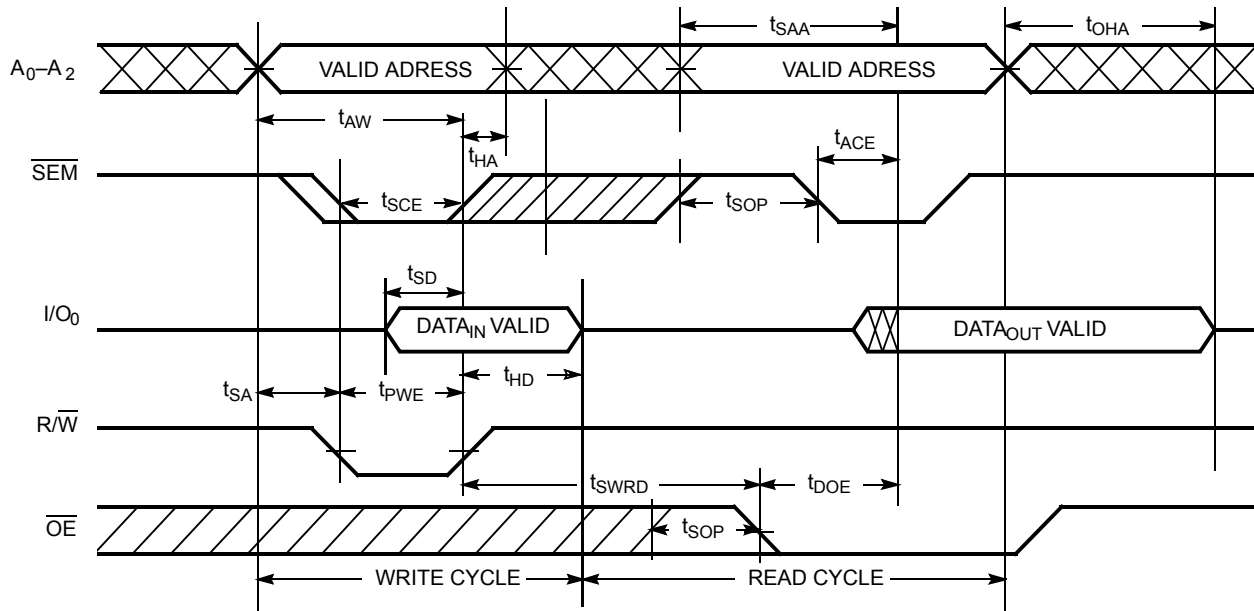


### Notes

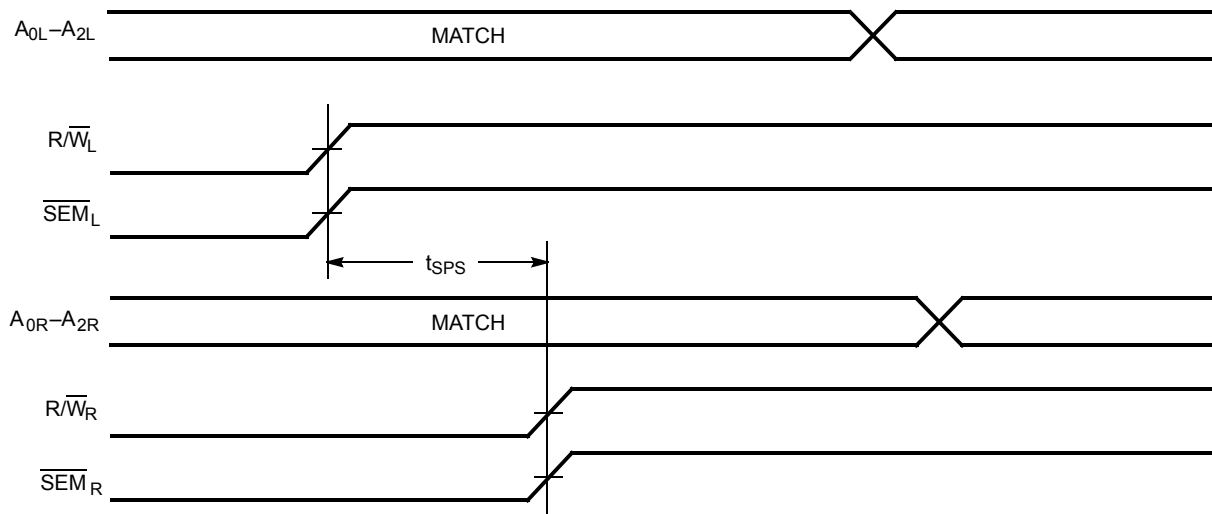
24. R/W must be HIGH during all address transitions.
25. A write occurs during the overlap ( $t_{SCE}$  or  $t_{PWE}$ ) of a LOW  $\overline{CE}$  or  $\overline{SEM}$  and a LOW  $\overline{UB}$  or  $\overline{LB}$ .
26.  $t_{HA}$  is measured from the earlier of CE or R/W or ( $\overline{SEM}$  or R/W) going HIGH at the end of write cycle.
27. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or ( $t_{HZWE} + t_{SD}$ ) to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{SD}$ . If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{PWE}$ .
28. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .
29. To access upper byte,  $\overline{CE} = V_{IL}$ ,  $\overline{UB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .  
To access lower byte,  $\overline{CE} = V_{IL}$ ,  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IH}$ .
30. Transition is measured  $\pm 500$  mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
31. During this period, the I/O pins are in the output state, and input signals must not be applied.
32. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high impedance state.

## Switching Waveforms (continued)

**Figure 9. Semaphore Read After Write Timing, Either Side** [33]



**Figure 10. Timing Diagram of Semaphore Contention** [34, 35, 36]



### Notes

33.  $\overline{CE}$  = HIGH for the duration of the above timing (both write and read cycle).

34.  $I/O_{0R} = I/O_{0L} = \text{LOW}$  (request semaphore);  $\overline{CE}_R = \overline{CE}_L = \text{HIGH}$ .

35. Semaphores are reset (available to both ports) at cycle start.

36. If  $t_{SPS}$  is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

## Switching Waveforms (continued)

Figure 11. Timing Diagram of Read with  $\overline{\text{BUSY}}$  ( $\overline{\text{M}}/\overline{\text{S}} = \text{HIGH}$ ) <sup>[37]</sup>

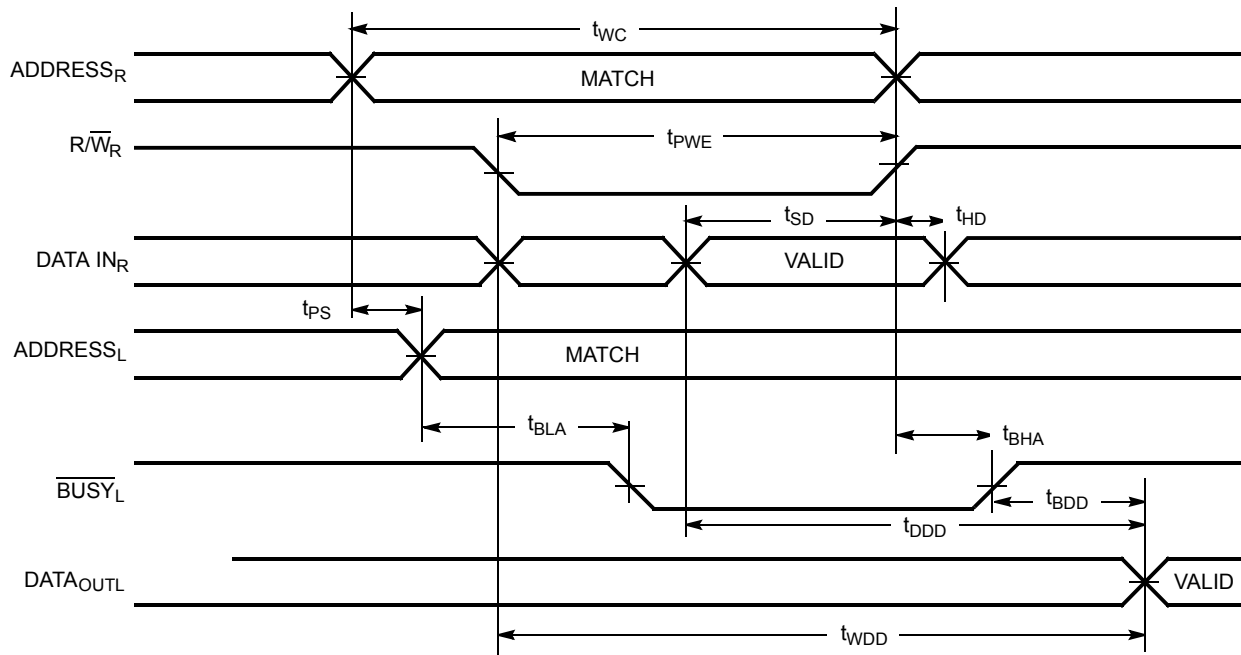
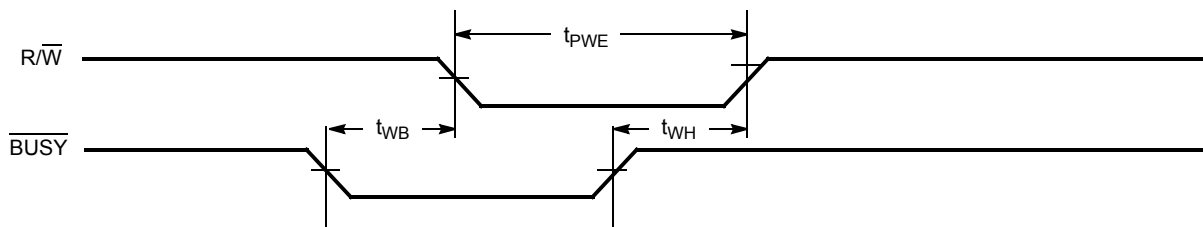


Figure 12. Write Timing with Busy Input ( $\overline{\text{M}}/\overline{\text{S}} = \text{LOW}$ )

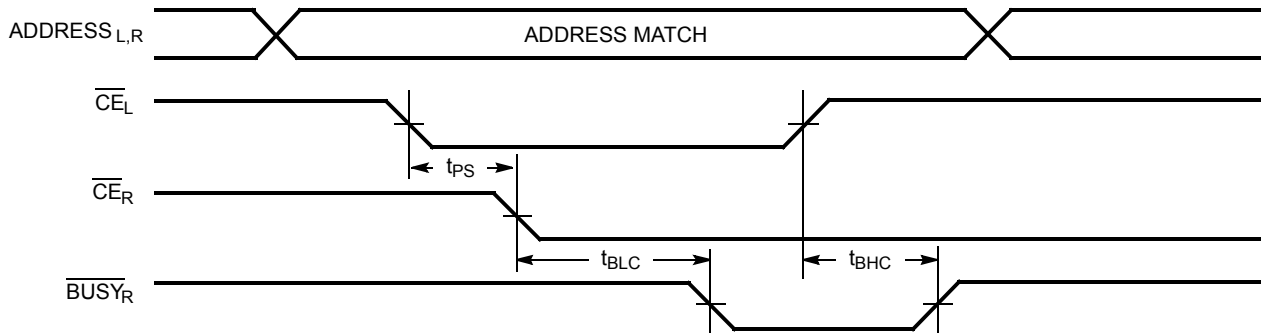


**Note**  
 37.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$ .

## Switching Waveforms (continued)

Figure 13. Busy Timing Diagram No.1 ( $\overline{\text{CE}}$  Arbitration) [38]

$\overline{\text{CE}}_{\text{L}}$  Valid First:



$\overline{\text{CE}}_{\text{R}}$  Valid First:

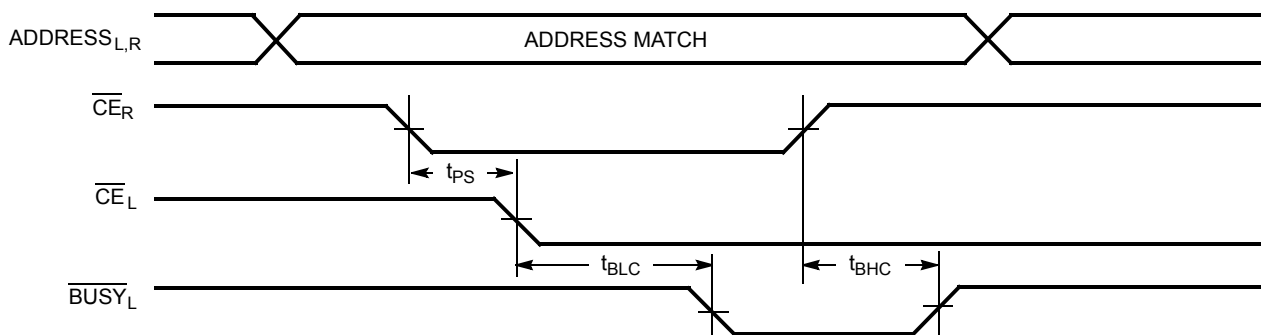
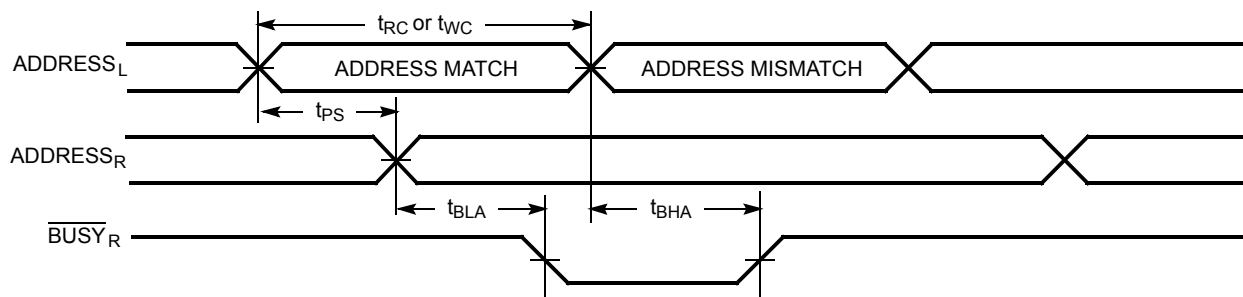
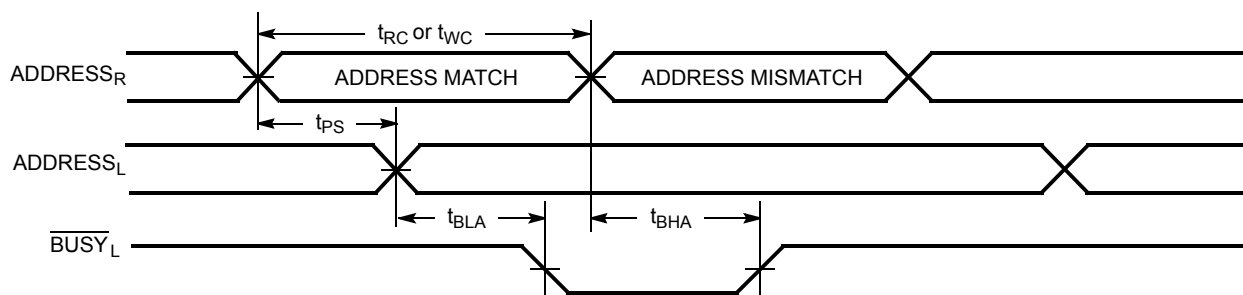


Figure 14. Busy Timing Diagram No. 2 (Address Arbitration) [38]

Left Address Valid First:



Right Address Valid First:

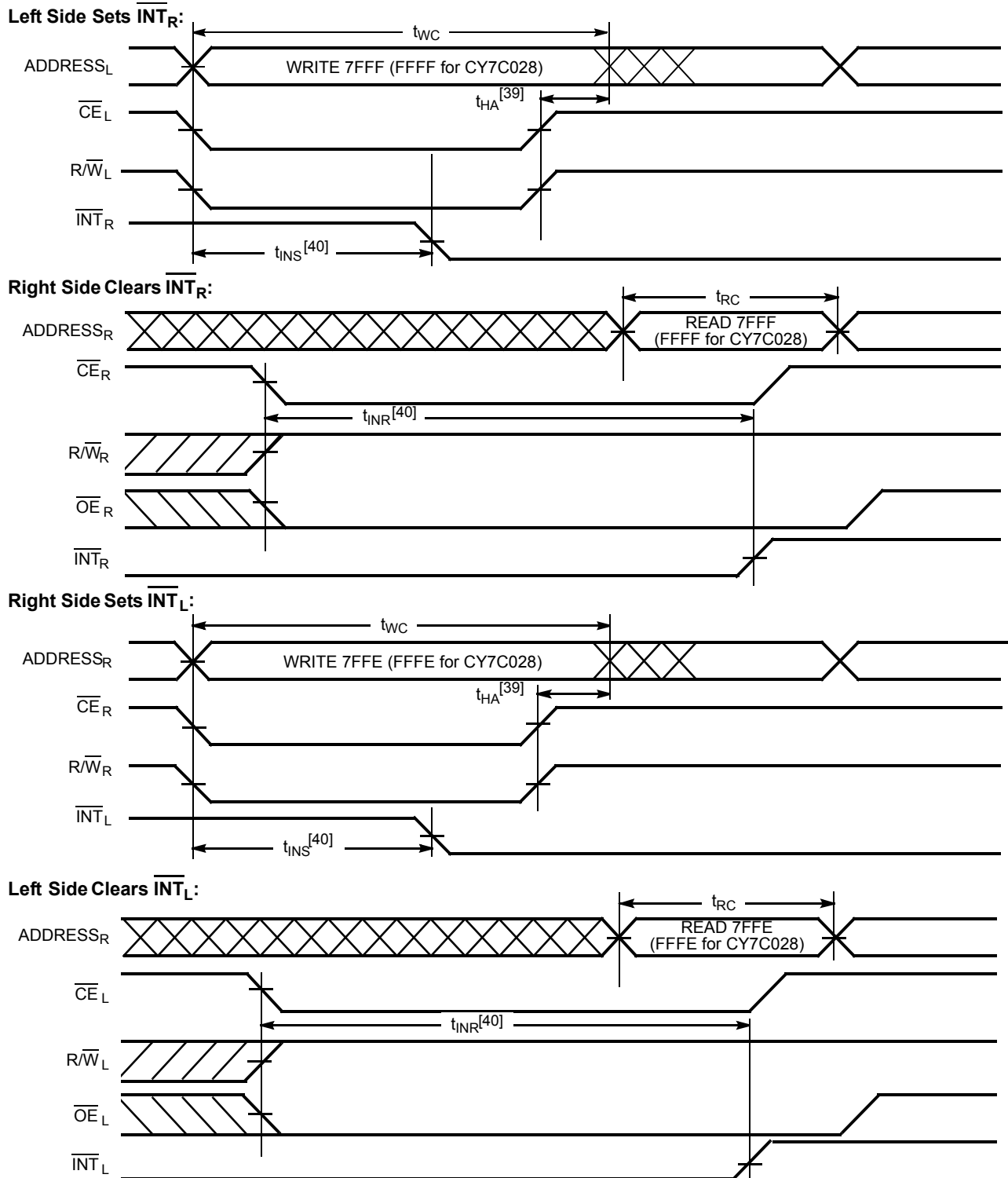


### Note

38. If  $t_{PS}$  is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side  $\overline{\text{BUSY}}$  is asserted.

## Switching Waveforms (continued)

Figure 15. Interrupt Timing Diagrams



### Notes

39.  $t_{HA}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is deasserted first.  
 40.  $t_{INS}$  or  $t_{INR}$  depends on which enable pin ( $\overline{\text{CE}}_L$  or  $\overline{\text{R}}/\overline{\text{W}}_L$ ) is asserted last.

## Architecture

The CY7C027 and CY7C028 consist of an array of 32K and 64K words of 16 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be used for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power down feature controlled by CE. Each port is provided with its own output enable control (OE), which allows data to be read from the device.

**Table 1. Non-Contending Read/Write**

| Inputs |                                                                                     |    |    |    |     | Outputs                             |                                    | Operation                                  |
|--------|-------------------------------------------------------------------------------------|----|----|----|-----|-------------------------------------|------------------------------------|--------------------------------------------|
| CE     | R/W                                                                                 | OE | UB | LB | SEM | I/O <sub>8</sub> –I/O <sub>15</sub> | I/O <sub>0</sub> –I/O <sub>7</sub> |                                            |
| H      | X                                                                                   | X  | X  | X  | H   | High Z                              | High Z                             | Deselected: Power Down                     |
| X      | X                                                                                   | X  | H  | H  | H   | High Z                              | High Z                             | Deselected: Power Down                     |
| L      | L                                                                                   | X  | L  | H  | H   | Data In                             | High Z                             | Write to Upper Byte Only                   |
| L      | L                                                                                   | X  | H  | L  | H   | High Z                              | Data In                            | Write to Lower Byte Only                   |
| L      | L                                                                                   | X  | L  | L  | H   | Data In                             | Data In                            | Write to Both Bytes                        |
| L      | H                                                                                   | L  | L  | H  | H   | Data Out                            | High Z                             | Read Upper Byte Only                       |
| L      | H                                                                                   | L  | H  | L  | H   | High Z                              | Data Out                           | Read Lower Byte Only                       |
| L      | H                                                                                   | L  | L  | L  | H   | Data Out                            | Data Out                           | Read Both Bytes                            |
| X      | X                                                                                   | H  | X  | X  | X   | High Z                              | High Z                             | Outputs Disabled                           |
| H      | H                                                                                   | L  | X  | X  | L   | Data Out                            | Data Out                           | Read Data in Semaphore Flag                |
| X      | H                                                                                   | L  | H  | H  | L   | Data Out                            | Data Out                           | Read Data in Semaphore Flag                |
| H      |  | X  | X  | X  | L   | Data In                             | Data In                            | Write D <sub>IN0</sub> into Semaphore Flag |
| X      |  | X  | H  | H  | L   | Data In                             | Data In                            | Write D <sub>IN0</sub> into Semaphore Flag |
| L      | X                                                                                   | X  | L  | X  | L   |                                     |                                    | Not Allowed                                |
| L      | X                                                                                   | X  | X  | L  | L   |                                     |                                    | Not Allowed                                |

## Read Operation

When reading the device, the user must assert both the  $\overline{\text{OE}}$  and CE pins. Data is available  $t_{\text{ACE}}$  after CE or  $t_{\text{DOE}}$  after OE is

## Functional Overview

### Write Operation

Data must be set up for a duration of  $t_{\text{SD}}$  before the rising edge of R/W to guarantee a valid write. A write operation is controlled by either the R/W pin (see Figure 7 on page 11) or the CE pin (see Figure 8 on page 11). Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port  $t_{\text{DD}}$  after the data is presented on the other port.

asserted. If the user wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin, and OE must also be asserted.

## Interrupts

The upper two memory locations may be used for message passing. The highest memory location (7FFF for the CY7C027, FFFF for the CY7C028) is the mailbox for the right port and the second-highest memory location (7FFE for the CY7C027, FFFE for the CY7C028) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy is summarized in [Table 2](#).

**Table 2. Interrupt Operation Example (assumes  $\overline{\text{BUSY}}_L = \overline{\text{BUSY}}_R = \text{HIGH}$ )** <sup>[41]</sup>

| Function                                   | Left Port        |                 |                 |                     |                   | Right Port       |                 |                 |                     |                   |
|--------------------------------------------|------------------|-----------------|-----------------|---------------------|-------------------|------------------|-----------------|-----------------|---------------------|-------------------|
|                                            | R/W <sub>L</sub> | CE <sub>L</sub> | OE <sub>L</sub> | A <sub>0L-14L</sub> | INT <sub>L</sub>  | R/W <sub>R</sub> | CE <sub>R</sub> | OE <sub>R</sub> | A <sub>0R-14R</sub> | INT <sub>R</sub>  |
| Set Right $\overline{\text{INT}}_R$ Flag   | L                | L               | X               | 7FFF                | X                 | X                | X               | X               | X                   | L <sup>[42]</sup> |
| Reset Right $\overline{\text{INT}}_R$ Flag | X                | X               | X               | X                   | X                 | X                | L               | L               | 7FFF                | H <sup>[43]</sup> |
| Set Left $\overline{\text{INT}}_L$ Flag    | X                | X               | X               | X                   | L <sup>[43]</sup> | L                | L               | X               | 7FFE                | X                 |
| Reset Left $\overline{\text{INT}}_L$ Flag  | X                | L               | L               | 7FFE                | H <sup>[42]</sup> | X                | X               | X               | X                   | X                 |

## Busy

The CY7C027 and CY7C028 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' CE<sub>s</sub> are asserted and an address match occurs within t<sub>PS</sub> of each other, the busy logic determines which port has access. If t<sub>PS</sub> is violated, one port definitely gains permission to the location, but it is not predictable which port gets that permission. BUSY is asserted t<sub>BLA</sub> after an address match or t<sub>BLC</sub> after CE is taken LOW.

## Master/Slave

A M/ $\overline{\text{S}}$  pin is provided to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled (t<sub>BLC</sub> or t<sub>BLA</sub>), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/ $\overline{\text{S}}$  pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

## Semaphore Operation

The CY7C027 and CY7C028 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t<sub>SOP</sub> before attempting to read the semaphore. The semaphore value is available t<sub>SWRD</sub> + t<sub>DOE</sub> after the rising

edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting  $\overline{\text{SEM}}$  LOW. The  $\overline{\text{SEM}}$  pin functions as a chip select for the semaphore latches (CE must remain HIGH during  $\overline{\text{SEM}}$  LOW). A<sub>0-2</sub> represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O<sub>0</sub> is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. [Table 3](#) shows sample semaphore operations.

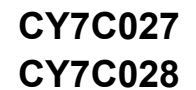
When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t<sub>SPS</sub> of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

### Notes

41. A<sub>0L-15L</sub> and A<sub>0R-15R</sub>: FFFF/FFFE for the CY7C028.
42. If  $\overline{\text{BUSY}}_L = \text{L}$ , then no change.
43. If  $\overline{\text{BUSY}}_R = \text{L}$ , then no change.

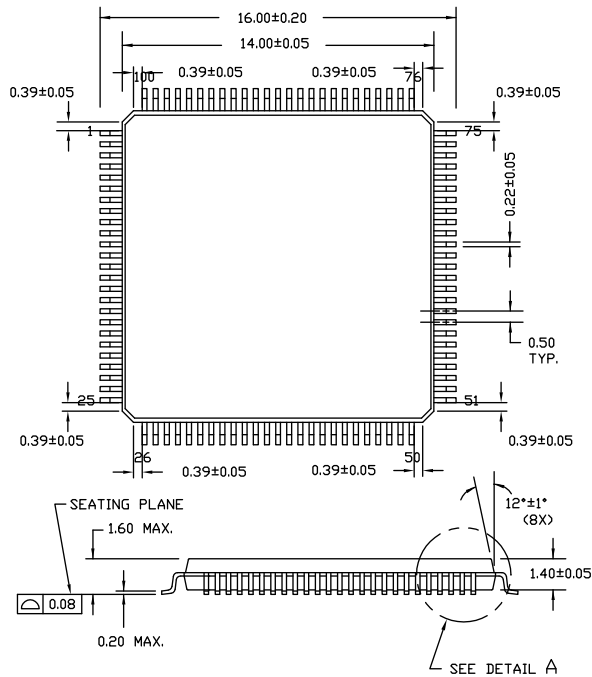
**Table 3. Semaphore Operation Example**

| Function                         | I/O <sub>0</sub> –I/O <sub>15</sub> Left | I/O <sub>0</sub> –I/O <sub>15</sub> Right | Status                                                 |
|----------------------------------|------------------------------------------|-------------------------------------------|--------------------------------------------------------|
| No action                        | 1                                        | 1                                         | Semaphore free                                         |
| Left port writes 0 to semaphore  | 0                                        | 1                                         | Left port has semaphore token                          |
| Right port writes 0 to semaphore | 0                                        | 1                                         | No change. Right side has no write access to semaphore |
| Left port writes 1 to semaphore  | 1                                        | 0                                         | Right port obtains semaphore token                     |
| Left port writes 0 to semaphore  | 1                                        | 0                                         | No change. Left port has no write access to semaphore  |
| Right port writes 1 to semaphore | 0                                        | 1                                         | Left port obtains semaphore token                      |
| Left port writes 1 to semaphore  | 1                                        | 1                                         | Semaphore free                                         |
| Right port writes 0 to semaphore | 1                                        | 0                                         | Right port has semaphore token                         |
| Right port writes 1 to semaphore | 1                                        | 1                                         | Semaphore free                                         |
| Left port writes 0 to semaphore  | 0                                        | 1                                         | Left port has semaphore token                          |
| Left port writes 1 to semaphore  | 1                                        | 1                                         | Semaphore free                                         |



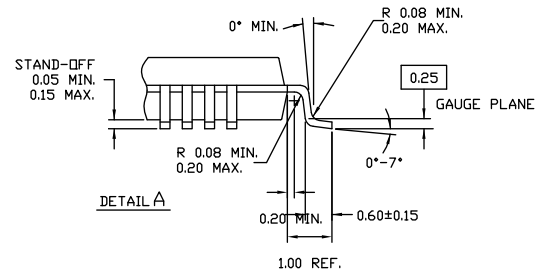
## Package Diagram

**Figure 16. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048**

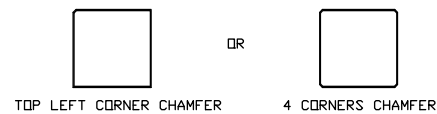


**NOTE:**

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE  
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



**NOTE:** PKG. CAN HAVE



51-85048 \*J

## Acronyms

| Acronym                | Description                             |
|------------------------|-----------------------------------------|
| $\overline{\text{CE}}$ | Chip Enable                             |
| CMOS                   | Complementary Metal Oxide Semiconductor |
| I/O                    | Input/Output                            |
| $\overline{\text{OE}}$ | Output Enable                           |
| SRAM                   | Static Random Access Memory             |
| TQFP                   | Thin Quad Flat Pack                     |
| TTL                    | Transistor-Transistor Logic             |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| mm     | millimeter      |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |

## Document History Page

| Document Title: CY7C027/CY7C028, 32K/64K × 16 Dual-Port Static RAM<br>Document Number: 38-06042 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                            | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| **                                                                                              | 110190  | SZV             | 09/29/2001      | Change from Spec number: 38-00666 to 38-06042                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *A                                                                                              | 122292  | RBI             | 12/27/2002      | Updated <a href="#">Maximum Ratings</a> :<br>Added Note 6 and referred the same note in “maximum ratings”.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *B                                                                                              | 236765  | YDT             | 6/23/2004       | Updated <a href="#">Features</a> (Removed cross information from this section).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| *C                                                                                              | 377454  | PCX             | 06/13/2005      | Updated <a href="#">Ordering Information</a> (Added Pb-free Logo, added Pb-free parts to ordering information namely CY7C027-20AXC, CY7C028-12AXC, CY7C028-15AXC, CY7C028-15AI, CY7C028-15AXI).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| *D                                                                                              | 2623540 | VKN / PYRS      | 12/17/2008      | Updated <a href="#">Ordering Information</a> (Added CY7C027-15AXI in the Ordering information table).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| *E                                                                                              | 2897217 | RAME            | 03/22/2010      | Updated <a href="#">Ordering Information</a> (Updated part numbers).<br>Updated <a href="#">Package Diagram</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *F                                                                                              | 3111417 | ADMU            | 12/15/2010      | Added <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *G                                                                                              | 3352028 | ADMU            | 08/23/2011      | Updated <a href="#">Features</a> (Removed CY7C037/CY7C038 related information and also removed -12 speed bin related information).<br>Updated <a href="#">Functional Description</a> (Removed CY7C037/CY7C038 related information).<br>Updated <a href="#">Pin Configurations</a> (Removed CY7C037/CY7C038 related information).<br>Updated <a href="#">Selection Guide</a> (Removed CY7C037/CY7C038 related information and also removed -12 speed bin related information).<br>Updated <a href="#">Electrical Characteristics</a> (Removed CY7C037/CY7C038 related information and also removed -12 speed bin related information).<br>Updated <a href="#">AC Test Loads and Waveforms</a> (Removed -12 speed bin related information).<br>Updated <a href="#">Switching Characteristics</a> (Removed CY7C037/CY7C038 related information and also removed -12 speed bin related information).<br>Updated <a href="#">Package Diagram</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated to new template. |
| *H                                                                                              | 3721632 | ADMU            | 08/23/2012      | Updated <a href="#">Operating Range</a> (Removed the Note “Industrial parts are available in CY7C028 only.” and its reference).<br>Updated <a href="#">Electrical Characteristics</a> (Removed the Note “Industrial parts are available in CY7C028 only.” and its reference).<br>Updated <a href="#">Ordering Information</a> (Updated part numbers).<br>Updated <a href="#">Package Diagram</a> (spec 51-85048 (Changed revision from *E to *G)).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| *I                                                                                              | 3846315 | SMCH            | 12/19/2012      | Updated <a href="#">Ordering Information</a> (Updated part numbers).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| *J                                                                                              | 4106180 | SMCH            | 08/28/2013      | Updated <a href="#">Pin Configurations</a> :<br>Updated <a href="#">Figure 1</a> (Removed overline on “R” in “CE1R” in pin 63).<br>Updated <a href="#">Package Diagram</a> :<br>spec 51-85048 – Changed revision from *G to *H.<br>Updated to new template.<br>Completing Sunset Review.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| *K                                                                                              | 4580622 | SMCH            | 11/26/2014      | Updated <a href="#">Functional Description</a> :<br>Added “For a complete list of related documentation, <a href="#">click here</a> .” at the end.<br>Updated <a href="#">Package Diagram</a> :<br>spec 51-85048 – Changed revision from *H to *I.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| *L                                                                                              | 5436673 | NILE            | 09/14/2016      | Updated <a href="#">Package Diagram</a> :<br>spec 51-85048 – Changed revision from *I to *J.<br>Updated to new template.<br>Completing Sunset Review.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Document History Page (continued)**

| Document Title: CY7C027/CY7C028, 32K/64K × 16 Dual-Port Static RAM<br>Document Number: 38-06042 |         |                 |                 |                                                       |
|-------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-------------------------------------------------------|
| Rev.                                                                                            | ECN No. | Orig. of Change | Submission Date | Description of Change                                 |
| *M                                                                                              | 5840744 | NILE            | 08/01/2017      | Updated to new template.<br>Completing Sunset Review. |

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