Contents

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1MHz		f = f_{max}			
		Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62137FV30LL	Industrial	2.2 V	3.0 V	3.6 V	45	1.6	2.5	13	18	1	5

Pin Configuration

Figure 1. 48-ball VFBGA pinout [2, 3]

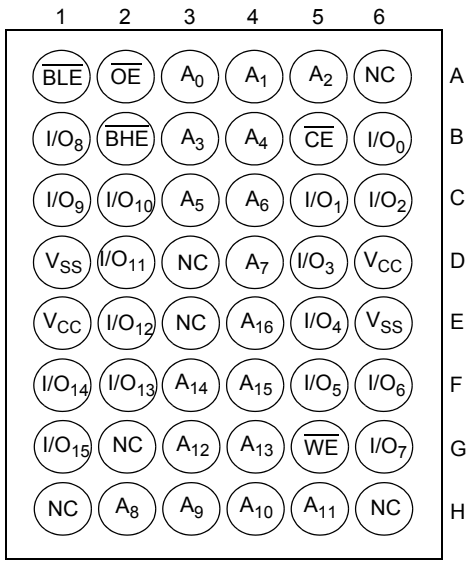
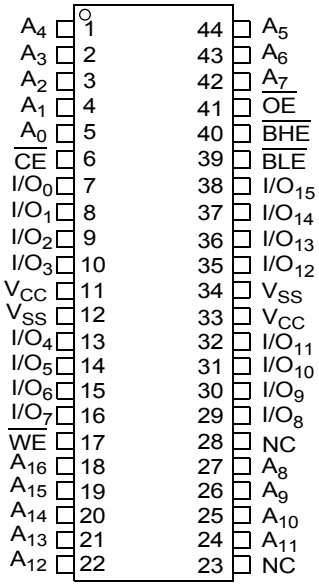


Figure 2. 44-pin TSOP II pinout [2]



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.3 V to 3.9 V

DC voltage applied to outputs in High Z state [4, 5] .....–0.3 V to 3.9 V

DC input voltage [5] .....–0.3 V to 3.9 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (MIL–STD–883, method 3015)

Latch up current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62137FV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial)			Unit
				Min	Typ [7]	Max	
V_{OH}	Output high voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	V
V_{OL}	Output low voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	V
V_{IH}	Input high voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	V
I_{IX}	Input leakage current	$GND \le V_I \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	13	18	mA
		f = 1 MHz		–	1.6	2.5	
I_{SB1}[8]	Automatic power-down current – CMOS inputs	$\overline{CE} \ge V_{CC} - 0.2$ V, or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC} - 0.2$ V, $V_{IN} \le 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	1	5	µA
I_{SB2} [8]	Automatic power-down current – CMOS inputs	$\overline{CE} \ge V_{CC} - 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		–	1	5	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$=V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Capacitance

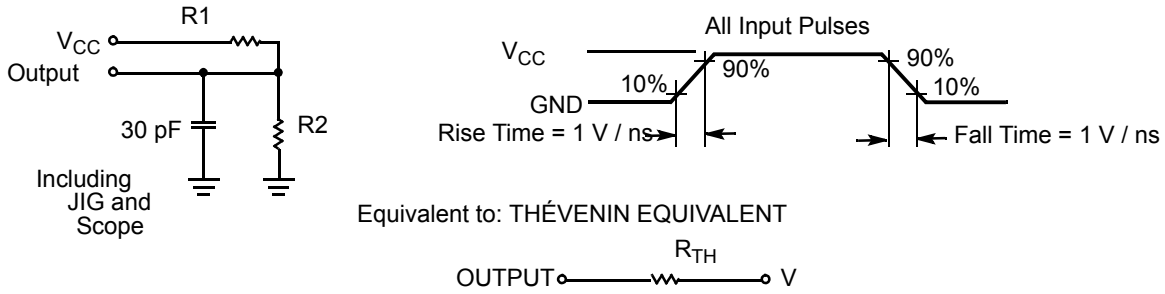
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal resistance (junction to case)		10	13	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Notes
9. Tested initially and after any design or process changes that may affect these parameters.

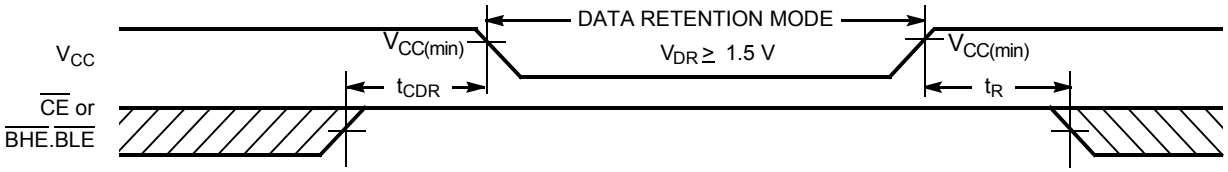
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial	–	–	4	µA
t_{CDR} [12]	Chip deselect to data retention time			0	–	–	ns
t_R [13]	Operation recovery time		CY62137FV30LL-45	45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [14]



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
14. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter [15, 16]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [17]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [17, 18]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [17]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [17, 18]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to low Z [17, 19]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to high Z [17, 18]	–	18	ns
Write Cycle [20]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [17, 18]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [17]	10	–	ns

Notes

15. Test conditions for all parameters, other than tristate parameters, assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads and Waveforms on page 5.
16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. If both byte enables are toggled together, this value is 10 ns.
20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 5. Read Cycle 1: Address Transition Controlled [21, 22]

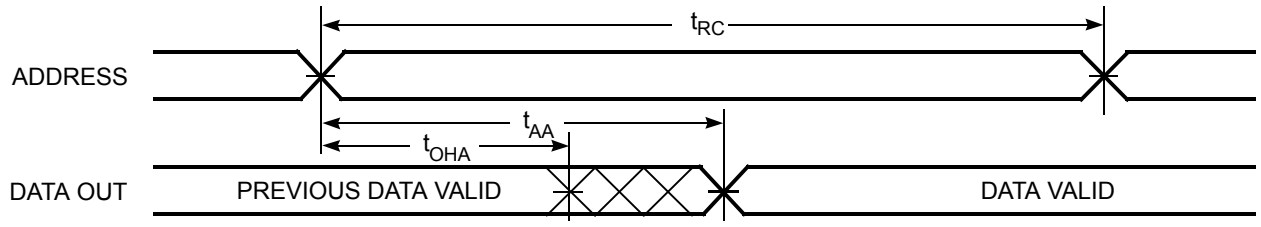
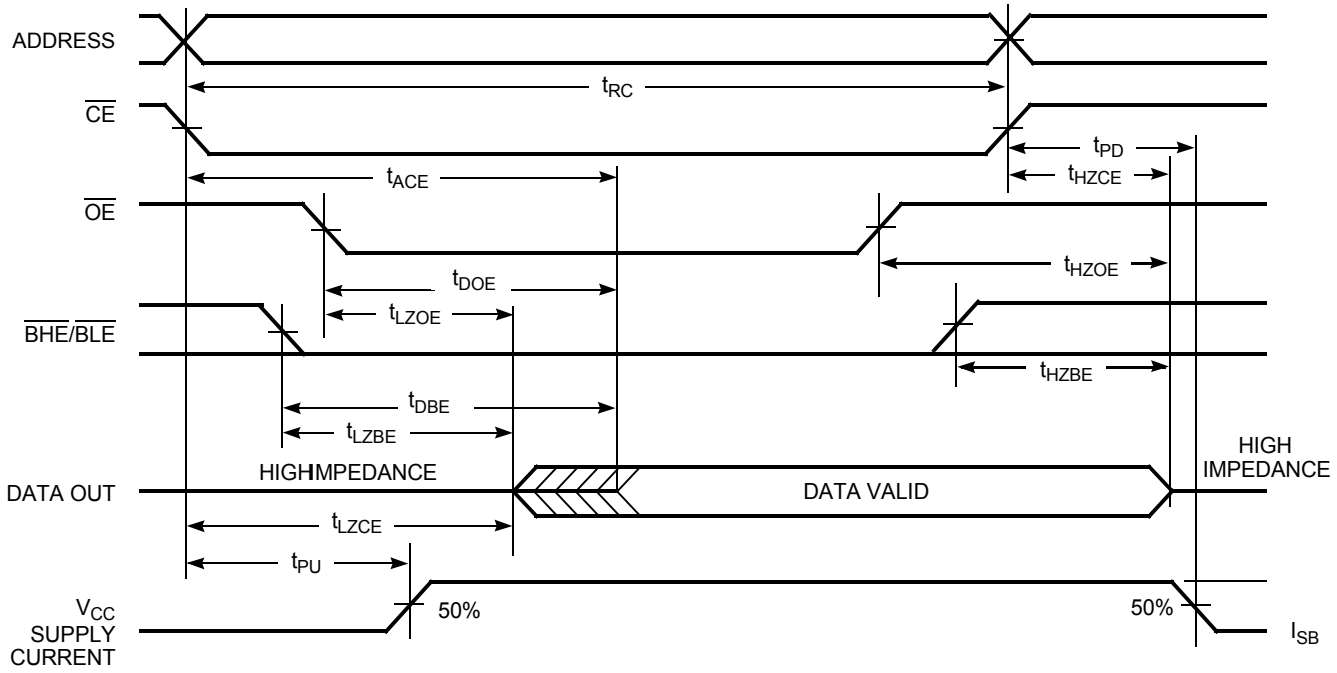


Figure 6. Read Cycle 2: $\overline{OE}$ Controlled [22, 23]



Notes
21. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle 1: $\overline{WE}$ Controlled [24, 25, 26]

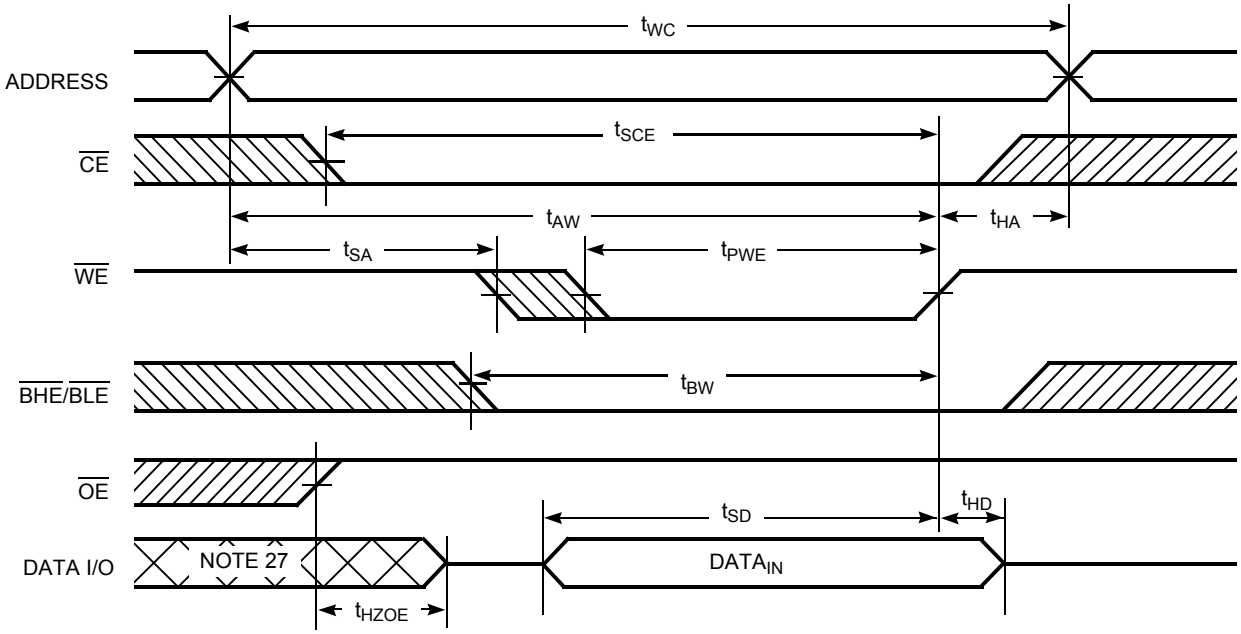
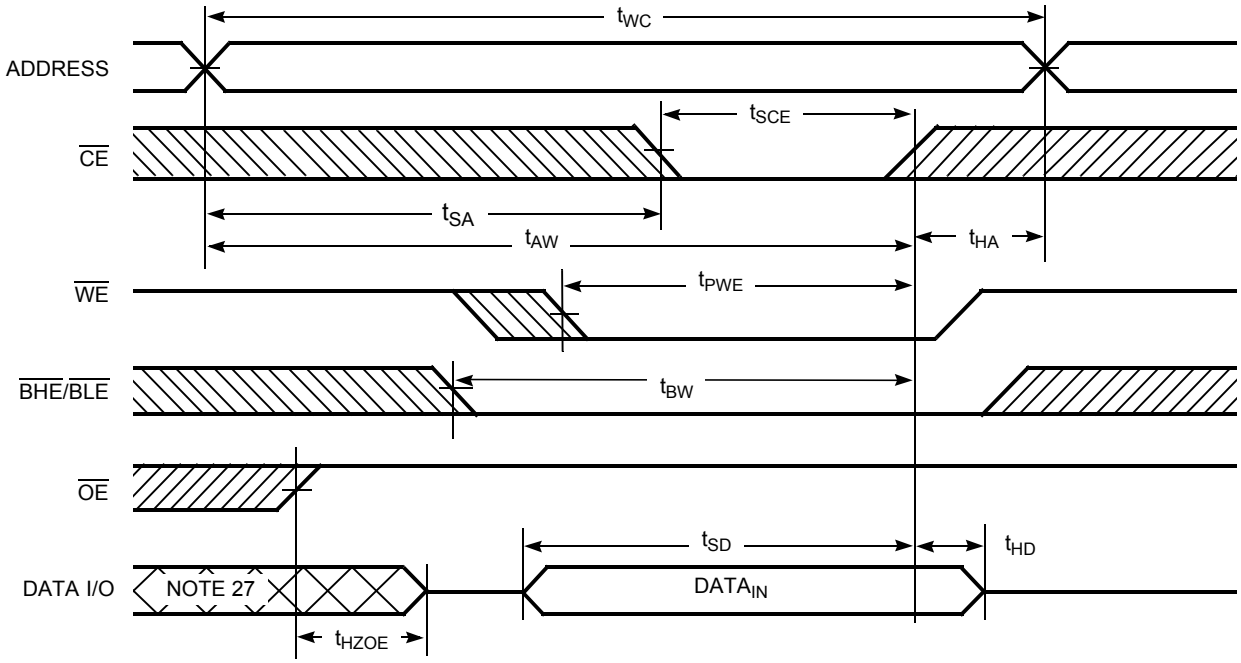


Figure 8. Write Cycle 2: $\overline{CE}$ Controlled [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [28]

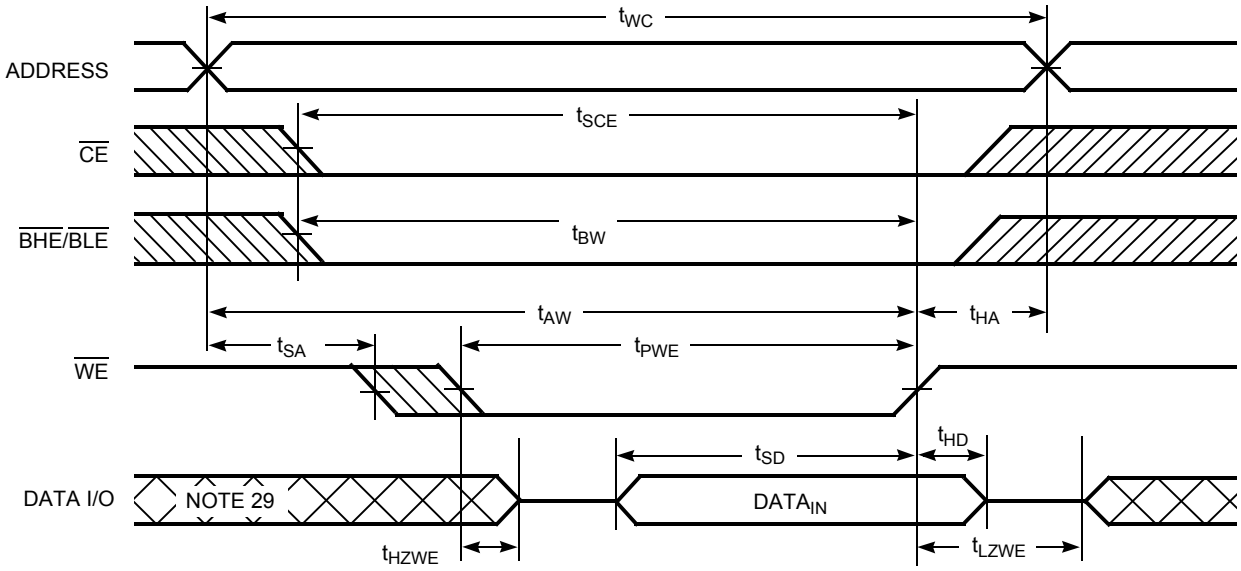
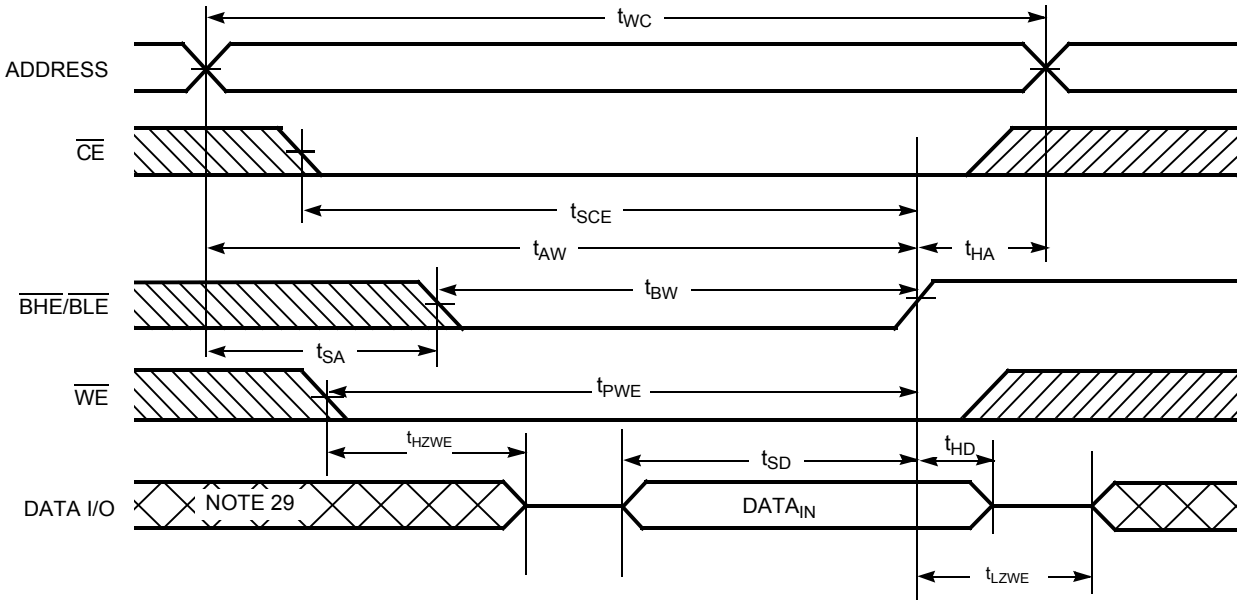


Figure 10. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [28]



Notes
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
29. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs or Outputs	Mode	Power
H	X	X	X [30]	X [30]	High Z	Deselect or power-down	Standby (I_{SB})
X [30]	X	X	H	H	High Z	Deselect or power-down	Standby (I_{SB})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

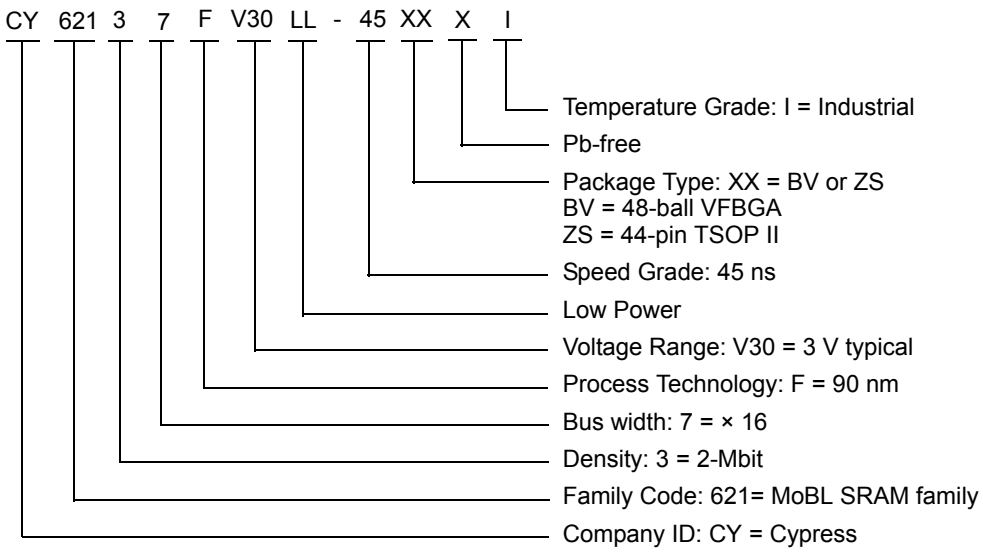
Note
30. The 'X' (Don't care) state for the Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ and $\overline{BLE}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62137FV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62137FV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

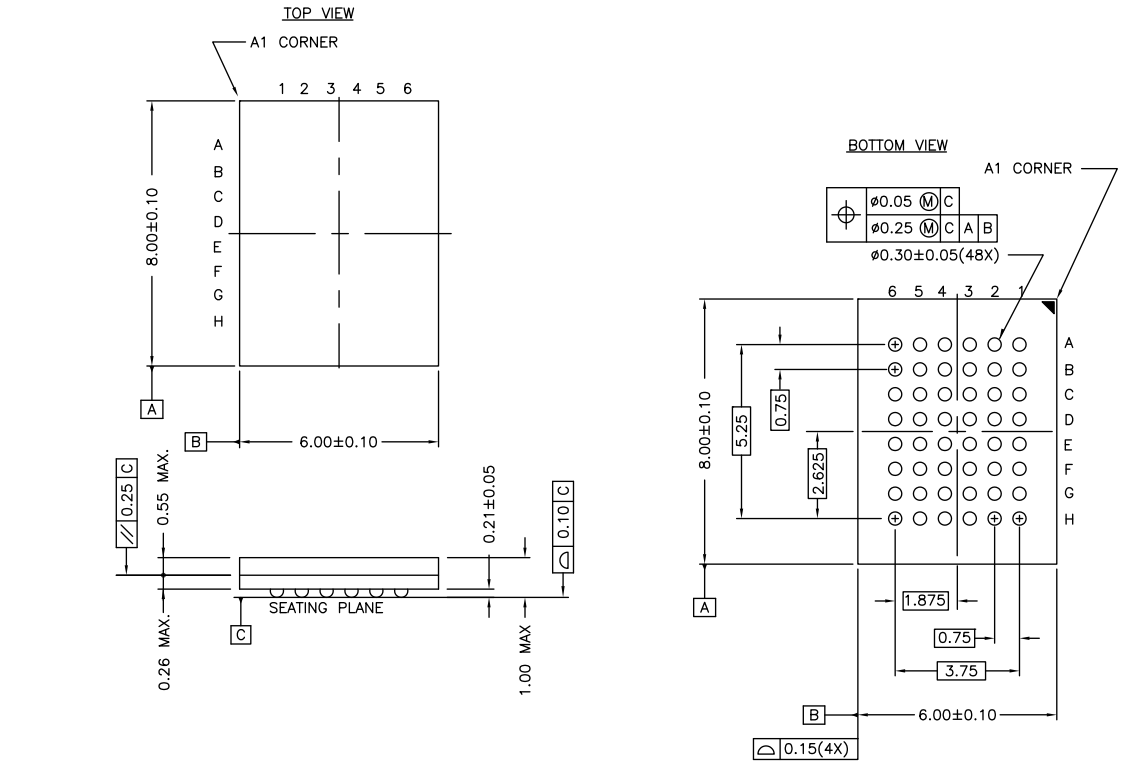
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

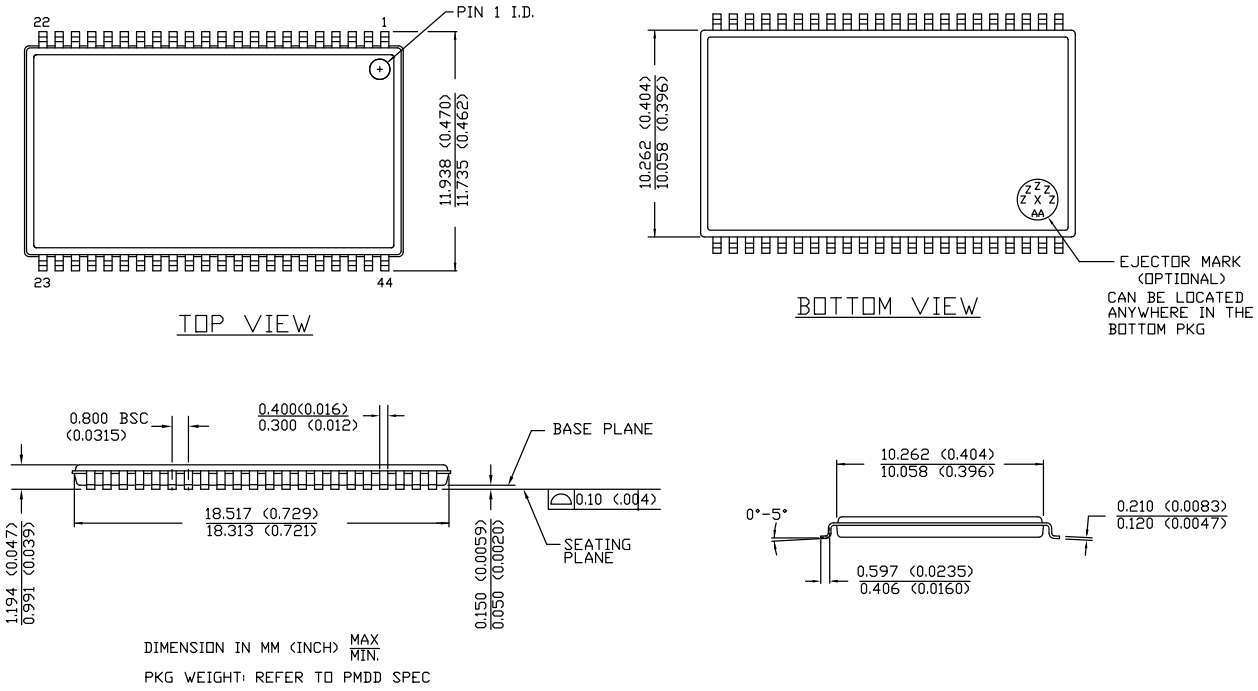


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{BLE}$	Byte Low Enable
$\overline{BHE}$	Byte High Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62137FV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-07141				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	449438	See ECN	NXR	New data sheet.
*A	464509	See ECN	NXR	Changed the $I_{SB2(typ)}$ value from 1.0 µA to 0.5 µA Changed the $I_{SB2(max)}$ value from 4 µA to 2.5 µA Changed the $I_{CC(typ)}$ value from 2 mA to 1.6 mA and $I_{CC(max)}$ value from 2.5 mA to 2.25 mA for f = 1 MHz test condition Changed the $I_{CC(typ)}$ value from 15 mA to 13 mA and $I_{CC(max)}$ value from 20 mA to 18 mA for f = 1 MHz test condition Changed the $I_{CCDR(typ)}$ value from 0.7 µA to 0.5 µA and $I_{CCDR(max)}$ value from 3 µA to 2.5 µA
*B	566724	See ECN	NXR	Changed status from preliminary to final Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition f = 1 MHz Changed the $I_{SB2(typ)}$ value from 0.5 µA to 1 µA Changed the $I_{SB2(max)}$ value from 2.5 µA to 5 µA Changed the $I_{CCDR(typ)}$ value from 0.5 µA to 1 µA and $I_{CCDR(max)}$ value from 2.5 µA to 4 µA
*C	869500	See ECN	VKN	Added Automotive-A and Automotive-E information Updated Ordering Information Table Added footnote 13 related to t_{ACE}
*D	901800	See ECN	VKN	Added footnote 9 related to I_{SB2} and I_{CCDR} Made footnote 14 applicable to AC parameters from t_{ACE}
*E	1371124	See ECN	VKN / AESA	Converted Automotive information from preliminary to final Changed I_{IX} min spec from –1 µA to –4 µA and I_{IX} max spec from +1 µA to +4 µA Changed I_{OZ} min spec from –1 µA to –4 µA and I_{OZ} max spec from +1 µA to +4 µA
*F	1875374	See ECN	VKN / AESA	Added -45BVI part in the Ordering Information table
*G	2943752	06/03/2010	VKN	Added Contents Added footnote related to Chip enable and Byte enables in Truth Table Updated Package Diagrams Updated links in Sales, Solutions, and Legal Information
*H	3055031	10/12/10	RAME	Converted all table notes into footnotes. Updated Electrical Characteristics. Changed $I_{SB1}/I_{SB2}/I_{CCDR}$ test conditions to reflect byte power down feature Updated Data Retention Characteristics. Updated Switching Characteristics. Updated Package Diagrams from 51-85150 *E to *F Added Acronyms and Units of Measure Table.
*I	3123998	01/03/2011	RAME	Separated Automotive and Industrial parts from datasheet Removed Automotive info
*J	3285093	06/16/2011	RAME	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated in new template.
*K	3841412	12/14/2012	YHB / TAVA	Updated Ordering Information (Updated part numbers). Updated Package Diagrams (spec 51-85150 (Changed revision from *F to *H), spec 51-85087 (Changed revision from *C to *E)).
*L	4102022	08/22/2013	VINI	Updated Switching Characteristics: Updated Note 16. Updated in new template.

Document History Page (continued)

Document Title: CY62137FV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-07141				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*M	4268388	01/31/2014	VINI	No technical updates. Completing Sunset Review.

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