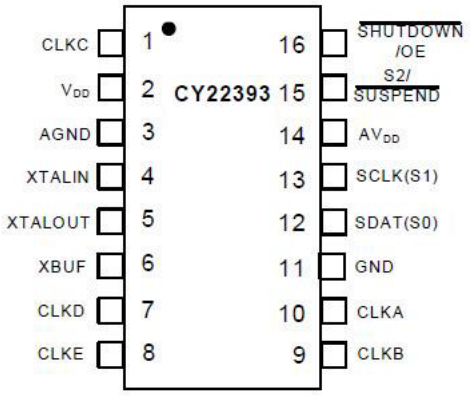
Contents

Pin Configuration

Figure 1. Pin Diagram - 16-Pin TSSOP CY22393



Pin Definitions

Name	Pin Number	Description
CLKC	1	Configurable clock output C
V_{DD}	2	Power supply
AGND	3	Analog ground
XTALIN	4	Reference crystal input or external reference clock input
XTALOUT	5	Reference crystal feedback
XBUF	6	Buffered reference clock output
CLKD	7	Configurable clock output D
CLKE	8	Configurable clock output E
CLKB	9	Configurable clock output B
CLKA	10	Configurable clock output A
GND	11	Ground
SDAT (S0)	12	Serial port data. S0 value latched during start-up
SCLK (S1)	13	Serial port clock. S1 value latched during start-up
AV_{DD}	14	Analog power supply
S2/ SUSPEND	15	General-purpose input for frequency control; bit 2. Optionally, Suspend mode control input
SHUTDOWN/ OE	16	Places outputs in tristate condition and shuts down chip when LOW. Optionally, only places outputs in tristate condition and does not shut down chip when LOW

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to the cross point switch. The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed using serial programming or by external CMOS inputs, S0, S1, and S2. See General-Purpose Inputs on page 4 for more detail.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the cross point switch. The frequency of PLL2 is changed using serial programming.

PLL3 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the cross point switch. The frequency of PLL3 is changed using serial programming.

General-Purpose Inputs

S2 is a general-purpose input that is programmed to enable two frequency settings. The options that switch with this general-purpose input are as follows: the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA.

The two frequency settings are contained within an eight-row frequency table. The values of SCLK (S1) and SDAT (S0) pins are latched during start-up and used as the other two indices into this array.

CLKA and CLKB have seven-bit dividers that point to one of the two programmable settings (register 0 or register 1). Both clocks share a single register control and both must be set to register 0, or both must be set to register 1.

For example, the part may be programmed to use S0, S1, and S2 (0, 0, 0 to 1, 1, 1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch-free.

Crystal Input

The input crystal oscillator is an important feature of CY24293 because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This enables maximum compatibility with crystals from various manufacturers. Parallel resonant, fundamental mode crystals should be used.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when nonlinear load capacitance interacts with load, bias, supply, and temperature changes. Nonlinear (FET gate) crystal load capacitors must not be used for MPEG, communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF. Typical crystals have a C_L specification in the range of 12 pF to 18 pF.

For driven clock inputs, the input load capacitors can be bypassed. This allows the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, leave XTALOUT floating.

Crystal Drive Level and Power

Crystals are specified to accept a maximum drive level. Generally, larger crystals can accept more power. For a specific voltage swing, power dissipation in the crystal is proportional to ESR and proportional to the square of the crystal frequency. (Note that the actual ESR is sometimes much less than the value specified by the crystal manufacturer.) Power is also almost proportional to the square of C_L.

Power can be reduced to less than the DL specified in Recommended Crystal Specifications on page 11 by selecting a reduced frequency crystal with low C_L and low R_1 (ESR).

Digital VCXO

The serial programming interface is used to dynamically change the capacitor load value on the crystal. A change in crystal load capacitance corresponds with a change in the reference frequency.

For special pullable crystals specified by Cypress, the capacitance pull range is +150 ppm to –150 ppm from midrange.

Be aware that adjusting the frequency of the reference affects all frequencies on all PLLs in a similar manner because all frequencies are derived from the single reference.

Output Configuration

Under normal operation there are four internal frequency sources that are routed through a programmable cross point switch to any of the four programmable 7-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. The following is a description of each output.

- CLKA's output originates from the cross point switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of the two programmable registers. See the section General-Purpose Inputs for more information.
- CLKB's output originates from the cross point switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of the two programmable registers. See the section General-Purpose Inputs for more information.
- CLKC's output originates from the cross point switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.
- CLKD's output originates from the cross point switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.
- CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4.
- XBUF is the buffered reference.

The clock outputs are designed to drive a single-point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination, it is generally not recommended.

Power-Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input tristates the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, reference oscillator, and all other active components. The resulting current on the V_{DD} pins is less than 5 mA (typical). Relock the PLLs after leaving the shutdown mode.

The S2/$\overline{\text{SUSPEND}}$ input is configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs are shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a tristate condition.

With the serial interface, each PLL and/or output is individually disabled. This provides total control over the power savings.

Improving Jitter

Jitter Optimization Control is useful for mitigating problems related to similar clocks switching at the same moment, causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning and allows superior jitter performance.

Power Supply Sequencing

There are no power supply sequencing requirements. The part is not fully operational until all V_{DD} pins are brought up to the voltages specified in the Operating Conditions on page 11.

All grounds must be connected to the same ground plane.

CyClocksRT Software

CyClocksRT is our second-generation software application that allows users to configure this device. The easy-to-use interface offers complete control of the many features of this device including, but not limited to, input frequency, PLL and output frequencies, and different functional options. It checks the data sheet frequency range limitations and automatically applies performance tuning. CyClocksRT also has a power estimation feature that allows you to see the power consumption of a specific configuration. You can download a free copy of CyberClocks that includes CyClocksRT on Cypress's web site, www.cypress.com.

CyClocksRT is used to generate P, Q, and divider values used in serial programming. There are many internal frequency rules that are not documented in this datasheet, but are required for proper operation of the device. Check these rules by using the latest version of CyClocksRT.

Device Programming

Part numbers starting with CY22392F are 'field programmable' devices. Field programmable devices are shipped unprogrammed and must be programmed prior to installation on a PCB. After a programming file (.jed) is created using the CyberClocks software, devices can be programmed in small quantities using the CY3672 programmer and CY3698[1] adapter. Programming of the clock device should be done at temperatures < 75 °C. Volume programming is available through Cypress Semiconductor's value-added distribution partners or by using third-party programmers from BP Microsystems, HiLo Systems, and others. For sufficiently large volumes, Cypress can supply pre-programmed devices with a part number extension that is configuration-specific.

Junction Temperature Limitations

It is possible to program this family such that the maximum junction temperature rating is exceeded. The package θ_{JA} is 115 °C/W. Use the CyClocksRT power estimation feature to verify that the programmed configuration meets the junction temperature and package power dissipation maximum ratings.

Note
1. CY3698 only supports programming of only the 16-pin TSSOP package.

Dynamic Updates

The output divider registers are not synchronized with the output clocks. Changing the divider value of an active output is likely cause a glitch on that output.

PLL P and Q data is spread between three bytes. Each byte becomes active on the acknowledge for that byte, so changing P and Q data for an active PLL can cause the PLL to try to lock an out-of-bounds condition. Therefore, you must turn off the PLL being programmed during the update. Do this by setting the PLL*_En bit LOW.

PLL1, CLKA, and CLKB each have multiple registers supplying data. To program these resources safely, always program an inactive register, and then transition to that register. This allows these resources to stay active during programming.

The serial interface is active even with the $\overline{\text{SHUTDOWN}}$/OE pin LOW as the serial interface logic uses static components and is completely self-timed. The part does not meet the I_{DDS} current limit with transitioning inputs.

Memory Bitmap Definitions

Clk{A–D}_Div[6:0]

Each of the four main output clocks (CLKA–CLKD) features a 7-bit linear output divider. Any divider setting between 1 and 127 may be used by programming the value of the desired divider into this register. Odd divide values are automatically duty-cycle corrected. Setting a divide value of zero powers down the divider and forces the output to a tristate condition.

CLKA and CLKB have two divider registers, selected by the DivSel bit (which, in turn, is selected by S2, S1, and S0). This allows the output divider value to change dynamically.

ClkE_Div[1:0]

CLKE has a simpler divider (see Table 1).

Table 1. ClkE Divider

ClkE_Div[1:0]	ClkE Output
00	Off
01	PLL1 0 ° Phase/4
10	PLL1 0 ° Phase/2
11	PLL1 0 ° Phase/3

Clk*_FS[2:0]

Each of the four main output clocks (CLKA–CLKD) has a three-bit code that determines the clock sources for the output divider. The available clock sources are: Reference, PLL1, PLL2, and PLL3. Each PLL provides both positive and negative phased outputs, for a total of seven clock sources (see Table 2). Note that the phase is a relative measure of the PLL output phases. No absolute phase relation exists at the outputs.

Table 2. Clock Source

Clk*_FS[2:0]	Clock Source
000	Reference Clock
001	Reserved
010	PLL1 0 ° Phase
011	PLL1 180 ° Phase
100	PLL2 0 ° Phase
101	PLL2 180 ° Phase
110	PLL3 0 ° Phase
111	PLL3 180 ° Phase

Xbuf_OE

This bit enables the XBUF output when HIGH.

PdnEn

This bit selects the function of the $\overline{\text{SHUTDOWN}}$/OE pin. When this bit is HIGH, the pin is an active LOW shutdown control. When this bit is LOW, this pin is an active HIGH output enable control.

Clk*_ACAdj[1:0]

These bits modify the output predrivers, changing the duty cycle through the pads. These are nominally set to 01, with a higher value shifting the duty cycle higher. The performance of the nominal setting is guaranteed.

Clk*_DCAdj[1:0]

These bits modify the DC drive of the outputs. The performance of the nominal setting is guaranteed.

Table 3. Output Drive Strength

Clk*_DCAdj[1:0]	Output Drive Strength
00	–30% of nominal
01	Nominal
10	+15% of nominal
11	+50% of nominal

PLL*_Q[7:0]

PLL*_P[9:0]

PLL*_P0

These are the 8-bit Q value and 11-bit P values that determine the PLL frequency. The formula is:

$$F_{PLL} = F_{REF} \times \left(\frac{P_T}{Q_T}\right)$$

$$P_T = (2 \times (P + 3)) + PO \qquad \text{Equation 1}$$

$$Q_T = Q + 2$$

PLL*_LF[2:0]

These bits adjust the loop filter to optimize the stability of the PLL. Table 4 can be used to guarantee stability. However, CyClocksRT uses a more complicated algorithm to set the loop filter for enhanced jitter performance. Use the **Print Preview** function in CyClocksRT to determine the charge pump settings for optimal jitter performance.

Table 4. Loop Filter Settings

PLL*_LF[2:0]	P_T Min	P_T Max
000	16	231
001	232	626
010	627	834
011	835	1043
100	1044	1600

PLL*_En

This bit enables the PLL when HIGH. If PLL2 or PLL3 are not enabled, then any output selecting the disabled PLL must have a divider setting of zero (off). Because the PLL1_En bit is dynamic, internal logic automatically turns off dependent outputs when PLL1_En goes LOW.

DivSel

This bit controls which register is used for the CLKA and CLKB dividers.

OscCap[5:0]

This controls the internal capacitive load of the oscillator. The approximate effective crystal load capacitance is:

$$C_{LOAD} = 6pF + (OscCap \times 0.375pF) \qquad \text{Equation 2}$$

Set to zero for external reference clock.

OscDrv[1:0]

These bits control the crystal oscillator gain setting. These must always be set according to Table 5. The parameters are the Crystal Frequency, Internal Crystal Parasitic Resistance (equivalent series resistance), and the OscCap setting during crystal start-up, which occurs when power is applied, or after shutdown is released. If in doubt, use the next higher setting.

Table 5. Crystal Oscillator Gain Settings

OscCap	00H–20H		20H–30H		30H–40H	
Crystal Freq\ R	30 Ω	60 Ω	30 Ω	60 Ω	30 Ω	60 Ω
8–15 MHz	00	01	01	10	01	10
15–20 MHz	01	10	01	10	10	10
20–25 MHz	01	10	10	10	10	11
25–30 MHz	10	10	10	11	11	NA

For external reference, the use Table 6.

Table 6. Osc Drv for External Reference

External Freq (MHz)	1–25	25–50	50–90	90–166
OscDrv[1:0]	00	01	10	11

Reserved

These bits must be programmed LOW for proper operation of the device.

Serial Programming Bitmaps – Summary Tables

Addr	DivSel	b7	b6	b5	b4	b3	b2	b1	b0
08H	0	ClkA_FS[0]	ClkA_Div[6:0]						
09H	1	ClkA_FS[0]	ClkA_Div[6:0]						
0AH	0	ClkB_FS[0]	ClkB_Div[6:0]						
0BH	1	ClkB_FS[0]	ClkB_Div[6:0]						
0CH	–	ClkC_FS[0]	ClkC_Div[6:0]						
0DH	–	ClkD_FS[0]	ClkD_Div[6:0]						
0EH	–	ClkD_FS[2:1]		ClkC_FS[2:1]		ClkB_FS[2:1]		ClkA_FS[2:1]	
0FH	–	Clk{C,X}_ACAdj[1:0]		Clk{A,B,D,E}_ACAdj[1:0]		PdnEn	Xbuf_OE	ClkE_Div[1:0]	
10H	–	ClkX_DCAdj[1]		Clk{D,E}_DCAdj[1]		ClkC_DCAdj[1]		Clk{A,B}_DCAdj[1]	
11H	–	PLL2_Q[7:0]							
12H	–	PLL2_P[7:0]							
13H	–	Reserved	PLL2_En	PLL2_LF[2:0]			PLL2_PO	PLL2_P[9:8]	
14H	–	PLL3_Q[7:0]							
15H	–	PLL3_P[7:0]							
16H	–	Reserved	PLL3_En	PLL3_LF[2:0]			PLL3_PO	PLL3_P[9:8]	
17H	–	Osc_Cap[5:0]						Osc_Drv[1:0]	

Addr	S2 (1,0)	b7	b6	b5	b4	b3	b2	b1	b0
40H	000	PLL1_Q[7:0]							
41H		PLL1_P[7:0]							
42H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
43H	001	PLL1_Q[7:0]							
44H		PLL1_P[7:0]							
45H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
46H	010	PLL1_Q[7:0]							
47H		PLL1_P[7:0]							
48H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
49H	011	PLL1_Q[7:0]							
4AH		PLL1_P[7:0]							
4BH		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
4CH	100	PLL1_Q[7:0]							
4DH		PLL1_P[7:0]							
4EH		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
4FH	101	PLL1_Q[7:0]							
50H		PLL1_P[7:0]							
51H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
52H	110	PLL1_Q[7:0]							
53H		PLL1_P[7:0]							
54H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
55H	111	PLL1_Q[7:0]							
56H		PLL1_P[7:0]							
57H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	

Serial Bus Programming Protocol and Timing

The CY22393 has a 2-wire serial interface for in-system programming. They use the SDAT and SCLK pins, and operate up to 400 kbit/s in Read or Write mode. Except for the data hold time, it is compliant with the I^2C bus standard. The basic Write serial format is as follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit.

The basic serial format is illustrated in Figure 3 on page 9.

Default Startup Condition for the CY22393

The default (programmed) condition of CY24293 is set by the distributor, who programs the device using a customer-specified JEDEC file produced by CyClocksRT, Cypress's proprietary development software. Parts shipped by the factory are blank and unprogrammed. In this condition, all bits are set to 0, all outputs are tristated, and the crystal oscillator circuit is active.

While users can develop their own subroutine to program any or all of the individual registers as described in the following pages, it may be easier to simply use CyClocksRT to produce the required register setting file.

Device Address

The device address is a 7-bit value that is configured during Field Programming. By programming different device addresses, two or more parts are connected to the serial interface and can be independently controlled. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

The default serial interface address is 69H, but there must not be a conflict with any other devices in your system. This can also be changed using CyClocksRT.

Data Valid

Data is valid when the clock is HIGH, and can only be transitioned when the clock is LOW as illustrated in Figure 4 on page 9.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 5 on page 10.

Start Sequence - Start Frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by the register address (eight bits) and register data (eight bits).

Stop Sequence - Stop Frame is indicated by SDAT going HIGH when SCLK is HIGH. A Stop Frame frees the bus for writing to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During Write Mode, the CY22393 responds with an Acknowledge pulse after every eight bits. To do this, it pulls the SDAT line LOW during the N*9th clock cycle, as illustrated in Figure 6 on page 10. (N = the number of bytes transmitted). During Read Mode, the master generates the acknowledge pulse after the data packet is read.

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (ack = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (ack = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write multiple bytes at a time, the master must not end the write sequence with a STOP condition. Instead, the master sends multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, the same as after the first byte, and accepts data until the STOP condition responds to the acknowledge bit. When receiving multiple bytes, the CY22393 internally increment the register address.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to '1' (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY22393 have an onboard address counter that retains "1" more than the address of the last word access. If the last word written or read was word 'n', then a current address read operation returns the value stored in location 'n+1'. When the CY22393 receives the slave address with the R/W bit set to a '1', it issues an acknowledge and transmit the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition, which causes the CY22393 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first set the word address. Do this by sending the address to the CY22393 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before setting the internal address pointer. Next, the master reissues the control byte with the R/W byte set to '1'. The CY22393, then, issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition which causes CY22393 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmitting the first 8-bit data word. This action increments the internal address pointer, and subsequently outputs the next 8-bit data word. By continuing to issue

acknowledges instead of STOP conditions, the master serially reads the entire contents of the slave device memory. Note that register addresses outside of 08H to 1BH and 40H to 57H can be read from but are not real registers and do not contain configuration information. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

Figure 2. Data Transfer Sequence on the Serial Bus

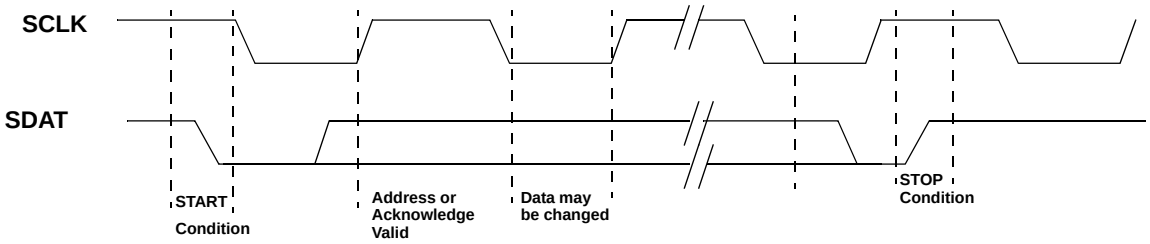


Figure 3. Data Frame Architecture

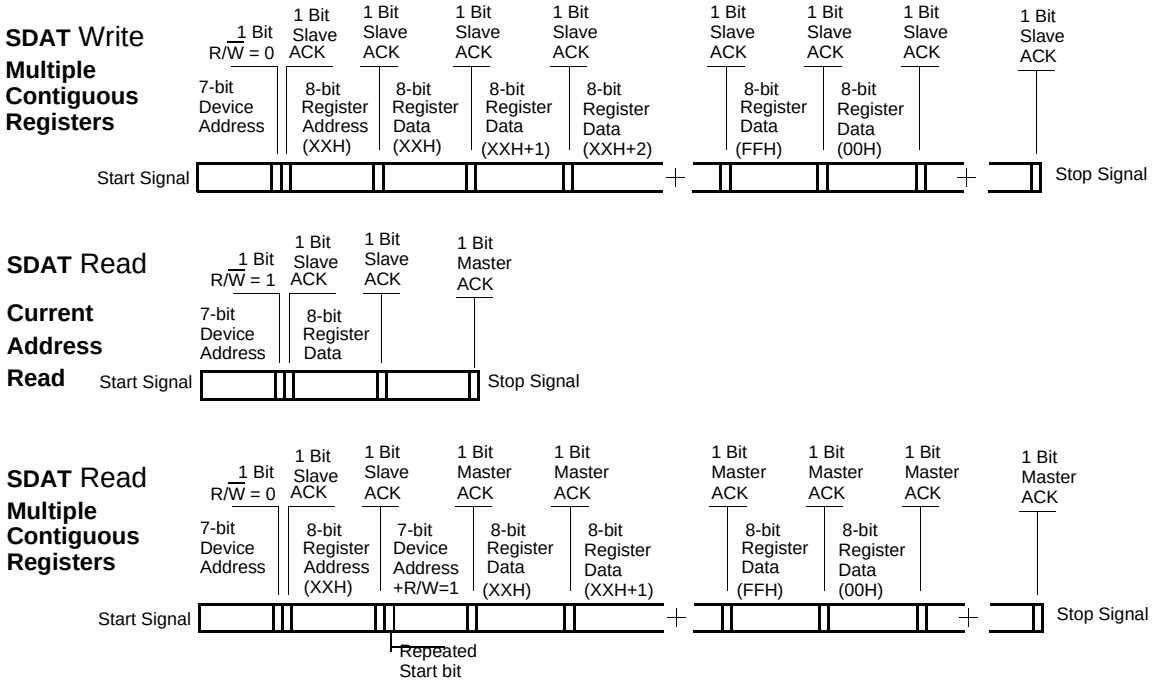
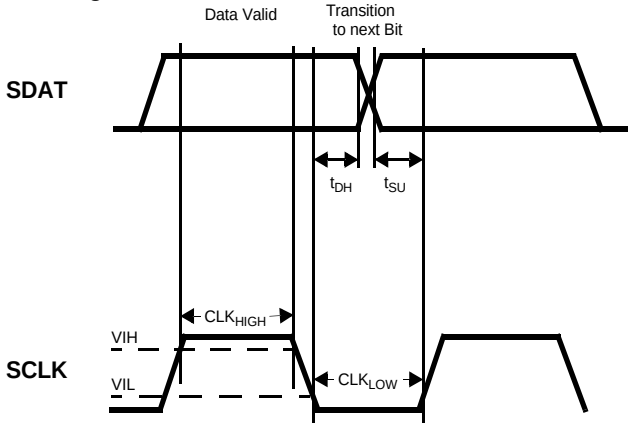


Figure 4. Data Valid and Data Transition Periods



Serial Programming Interface Timing

Figure 5. Start and Stop Frame

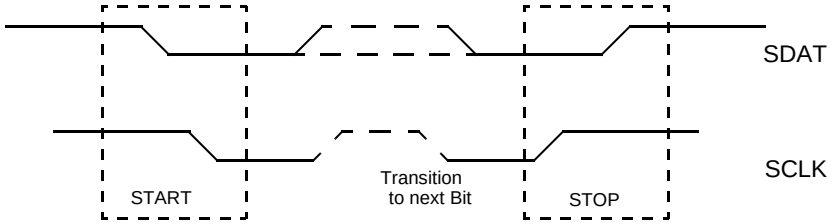
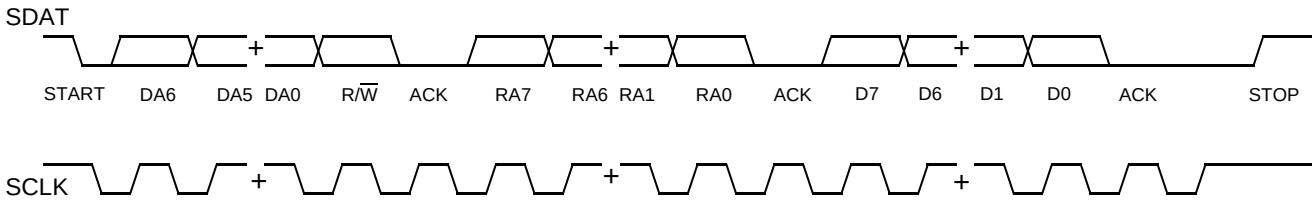


Figure 6. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Serial Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	400	kHz
	Start mode time from SDA LOW to SCL LOW	0.6	–	µs
CLK_{LOW}	SCLK LOW period	1.3	–	µs
CLK_{HIGH}	SCLK HIGH period	0.6	–	µs
t_{SU}	Data transition to SCLK HIGH	100	–	ns
t_{DH}	Data hold (SCLK LOW to data transition)	100	–	ns
	Rise time of SCLK and SDAT	–	300	ns
	Fall time of SCLK and SDAT	–	300	ns
	Stop mode time from SCLK HIGH to SDAT HIGH	0.6	–	µs
	Stop mode to Start mode	1.3	–	µs

Electrical Specifications

Absolute Maximum Conditions

Supply voltage .....–0.5 V to +7.0 V

DC input voltage ..... –0.5 V to + (AV_{DD} + 0.5 V)

Storage temperature ..... –65 °C to +125 °C

Junction temperature

A Grade..... 125 °C

E Grade.....150 °C

Data retention at T_J = 125 °C .....> 10 years

Data retention at T_J = 150 °C .....> 2 years

Maximum programming cycles 100

Package power dissipation (A-Grade) ..... 350 mW

Package power dissipation (E-Grade) ..... 217 mW

Static discharge voltage
(per MIL-STD-883, Method 3015) ..... ≥ 2000 V

Latch-up (per JEDEC 17) ..... ≥ ±200 mA

Stresses exceeding absolute maximum conditions may cause permanent damage to the device. These conditions are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this datasheet is not implied. Extended exposure to absolute maximum conditions may affect reliability.

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}/AV_{DD}	Supply voltage	3.135	3.3	3.465	V
T_A	Automotive A-Grade operating temperature, Ambient	–40	–	85	°C
T_A	Automotive E-Grade operating temperature, Ambient	-40		125	°C
C_{LOAD_OUT}	Maximum load capacitance	–	–	15	pF
f_{REF}	External reference crystal	8	–	30	MHz
	External reference clock[2], Automotive	1	–	150	MHz

Recommended Crystal Specifications

Parameter	Description	Description	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode	8	–	30	MHz
C_{LNOM}	Nominal load capacitance		8	–	20	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	50	Ω
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW

3.3 V Electrical Characteristics

Parameter	Description	Conditions[3]	Min	Typ	Max	Unit
I_{OH}	Output high current [4, 5]	$V_{OH} = V_{DD} – 0.5$ V, V_{DD} = 3.3 V	12	24	–	mA
I_{OL}	Output low current [4, 5]	V_{OL} = 0.5 V, V_{DD} = 3.3 V	12	24	–	mA
C_{XTAL_MIN}	Crystal load capacitance [4]	Capload at minimum setting	–	6	–	pF
C_{XTAL_MAX}	Crystal load capacitance[3]	Capload at maximum setting	–	30	–	pF
C_{IN}	Input pin capacitance [4]	Except crystal pins	–	7	–	pF
V_{IH}	High-level input voltage	CMOS levels,% of AV_{DD}	70%	–	–	AV_{DD}
V_{IL}	Low-level input voltage	CMOS levels,% of AV_{DD}	–		30%	AV_{DD}
I_{IH}	Input high current	$V_{IN} = AV_{DD} – 0.3$ V	–	<1	10	µA
I_{IL}	Input low current	V_{IN} = +0.3 V	–	<1	10	µA
I_{OZ}	Output leakage current	Three-state outputs (OE = Low)	–		10	µA

Notes
2. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
3. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
4. Guaranteed by design, not 100% tested.
5. Profile configuration through CyberClocks (JEDEC file) should be so generated such that Drive strength should be at ‘Mid Low’ or above.

3.3 V Electrical Characteristics (continued)

Parameter	Description	Conditions[3]	Min	Typ	Max	Unit
I_{DD}	Total power supply current	3.3-V power supply; 2 outputs at 20 MHz; 4 outputs at 40 MHz [6,7]	–	50	–	mA
		3.3-V power supply; 2 outputs at 166 MHz; 4 outputs at 83 MHz[6,7]	–	100	–	mA
I_{DDS}	Total power supply current in shutdown mode	Shutdown active	–	5	20	µA

3.3 V Switching Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$1/t_1$	Output frequency [8, 9]	Clock output limit, CMOS, Automotive	–	–	166	MHz
t_2	Output duty cycle [8, 10]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout < 100 MHz, divider ≥ 2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout > 100 MHz or divider = 1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising edge slew rate [8]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4	–	V/ns
t_4	Falling edge slew rate [8]	Output clock fall time, 20% to 80% of V_{DD}	0.75	1.4	–	V/ns
t_5	Output three-state timing [8]	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches	–	150	300	ns
t_6	Clock jitter [8, 9]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$	–	400	–	ps
t_7	Lock time [8]	PLL lock time from power-up	–	1.0	3	ms

Notes
6. Profile configuration through CyberClocks (JEDEC file) should be so generated such that for E-Grade, I_{DD} max < 56 mA (considering T_A max = 125 °C).
7. Profile configuration through CyberClocks (JEDEC file) should be so generated such that for A - Grade, I_{DD} max < 90 mA (considering T_A max = 85 °C).
8. Guaranteed to meet 20%–80% output thresholds, duty cycle, and crossing point specifications.
9. Reference output duty cycle depends on XTALIN duty cycle.
10. Jitter varies significantly with configuration. Reference output jitter depends on XTALIN jitter and edge rate.

Switching Waveforms

Figure 7. All Outputs, Duty Cycle and Rise and Fall Time

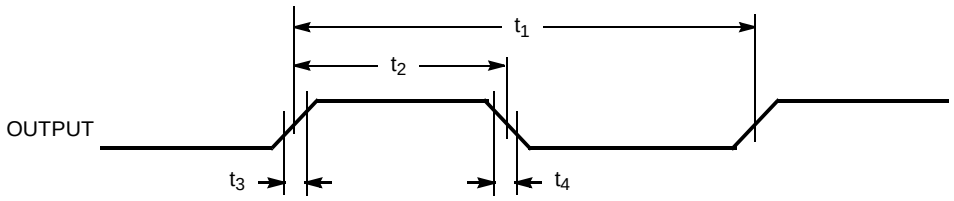


Figure 8. Output Tristate Timing

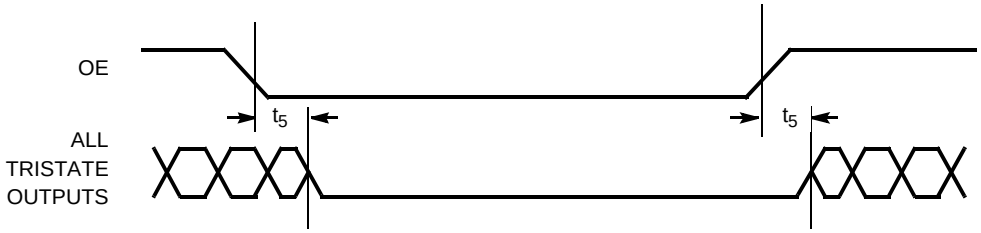


Figure 9. CLK Output Jitter

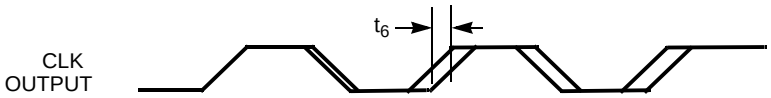
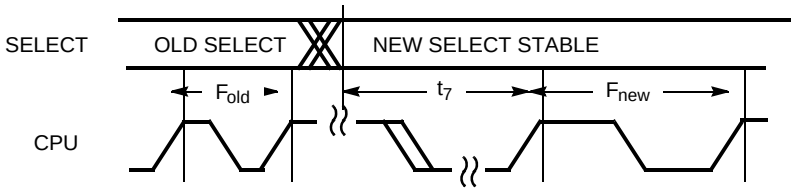
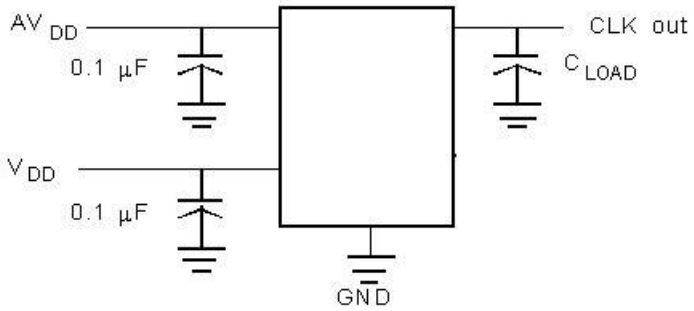


Figure 10. CPU Frequency Change



Test Circuit

Figure 11. Test Circuit



Ordering Information

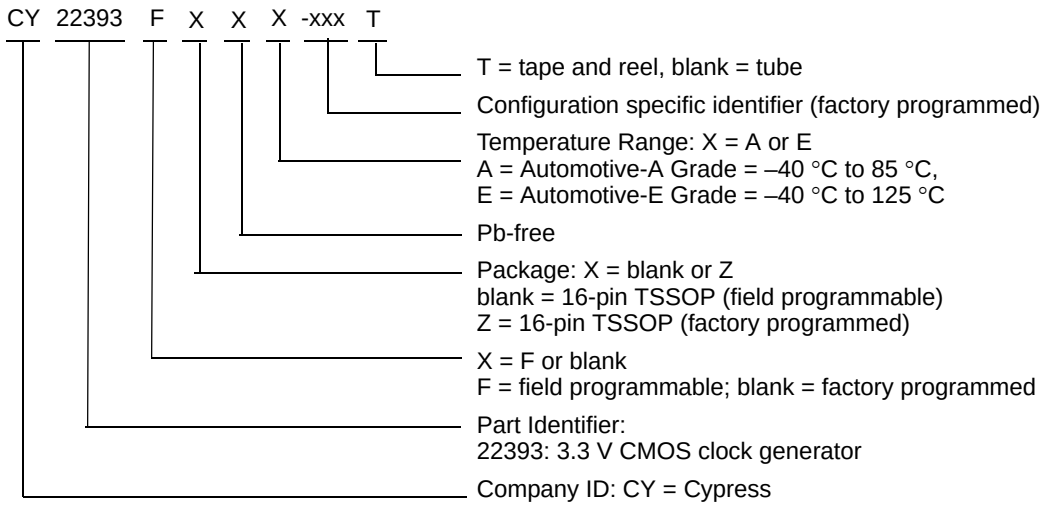
Ordering Code	Package Type	Product Flow
Pb-free		
CY22393FXA	16-pin TSSOP	Automotive A-Grade, –40 °C to 85 °C
CY22393FXAT	16-pin TSSOP - Tape and Reel	Automotive A-Grade, –40 °C to 85 °C
CY22393FXE	16-pin TSSOP	Automotive E-Grade, –40 °C to 125 °C
CY22393FXET	16-pin TSSOP - Tape and Reel	Automotive E-Grade, –40 °C to 125 °C
Programmer		
CY3672-USB	Programmer	
CY3698	CY22393F Adapter for CY3672-USB	

Possible Configurations

Some product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information

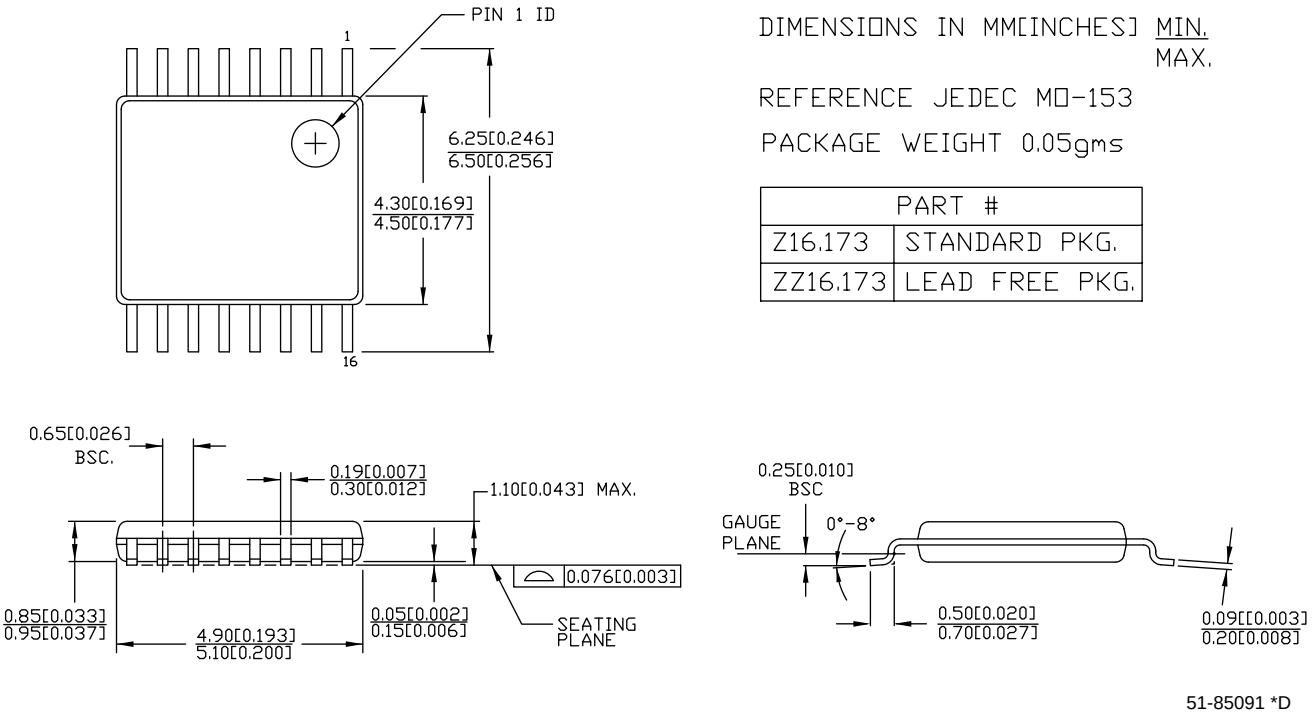
Ordering Code	Package Type	Product Flow
Pb-Free		
CY22393ZXA-xxx	16-pin TSSOP	Automotive A-Grade, –40 °C to 85 °C
CY22393ZXA-xxxT	16-pin TSSOP - Tape and Reel	Automotive A-Grade, –40 °C to 85 °C
CY22393ZXE-xxx	16-pin TSSOP	Automotive E-Grade, –40 °C to 125 °C
CY22393ZXE-xxxT	16-pin TSSOP - Tape and Reel	Automotive E-Grade, –40 °C to 125 °C

Ordering Code Definitions



Package Diagram

Figure 12. 16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Table 7. Acronyms Used in this Document

Acronym	Description
CMOS	complementary metal oxide semiconductor
ESR	equivalent series resistance
FAE	field application engineer
FET	field effect transistor
JEDEC	joint electron devices engineering council
LSB	least significant bit
LVTTL	low voltage transistor-transistor logic
MPEG	motion picture experts group
OE	output enable
PLL	phase-locked loop
TSSOP	thin shrink small outline package
VCXO	voltage-controlled crystal oscillator

Document Conventions

Units of Measure

Table 8. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

Document History Page

Document Title: CY22393, Automotive Three-PLL Serial-Programmable Flash-Programmable Clock Generator Document Number: 001-73555				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3416122	PURU	11/14/2011	New data sheet
*A	3693908	PURU	07/26/2012	Added CY22393 Automotive E-Grade Device
*B	4337034	CINM	04/23/2014	Added A and E grade compatibility in Features Added Device Programming section Added footnotes 1, 5, 6, and 7. Added junction temperature for A and E grade. Added data retention at T_J = 150 °C and updated package power dissipation for A and E grade. Changed datasheet status to Final

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