The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

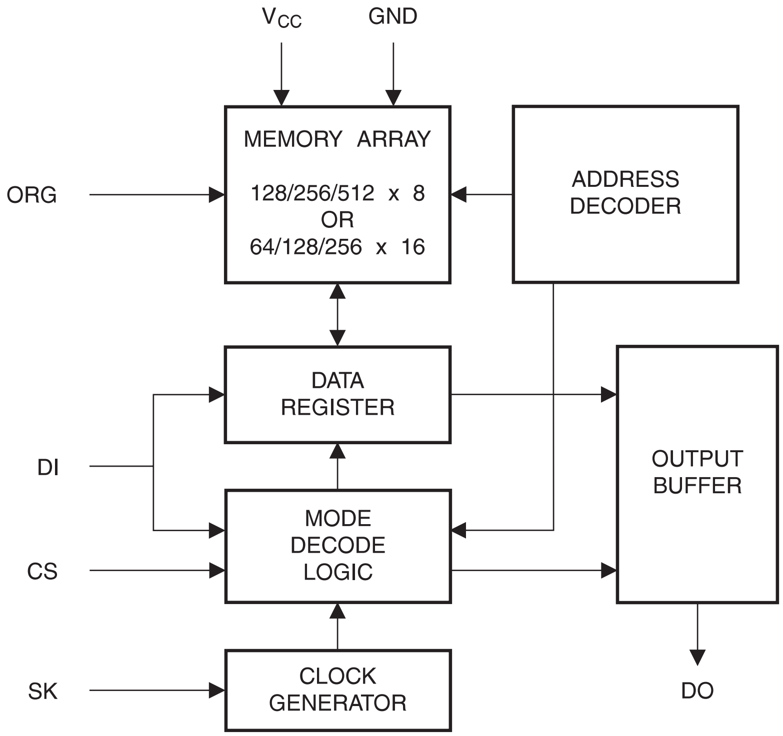
The AT93C46 is available in 4.5V to 5.5V, 2.7V to 5.5V, 2.5V to 5.5V, and 1.8V to 5.5V versions. The AT93C56/57/66 is available in 4.5V to 5.5V, 2.7V to 5.5V, and 2.5V to 5.5V versions.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Block Diagram



Note: 1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device (of approximately 1 MΩ) will select the x 16 organization. This feature is not available on 1.8V devices.

Pin Capacitance(1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0V	CS = 0V		17	30	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1} (1) V_{IH1}(1)	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2} (1) V_{IH2}(1)	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		-0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
			I_{OH} = -0.4 mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
			I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0 0		2 1 0.5 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{PD1}	Output Delay to ‘1’	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{PD0}	Output Delay to ‘0’	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 100 200 400	ns
t_{WP}	Write Cycle Time			0.1		10	ms
			$4.5V \le V_{CC} \le 5.5V$		1		ms
Endurance[1]	5.0V, 25°C, Page Mode			1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Instruction Set for the AT93C46

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6 - A_0	A_5 - A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXX	01XXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C57

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_7 - A_0	A_6 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX	11XXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_7 - A_0	A_6 - A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_7 - A_0	A_6 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXX	10XXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXX	01XXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXXX	00XXXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8 - A_0	A_7 - A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Functional Description

The AT93C46/56/57/66 is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic ‘1’) followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic ‘0’) precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical ‘1’ state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic ‘1’ at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic ‘0’ at DO indicates that programming is still in progress. A logic ‘1’ indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. **A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.**

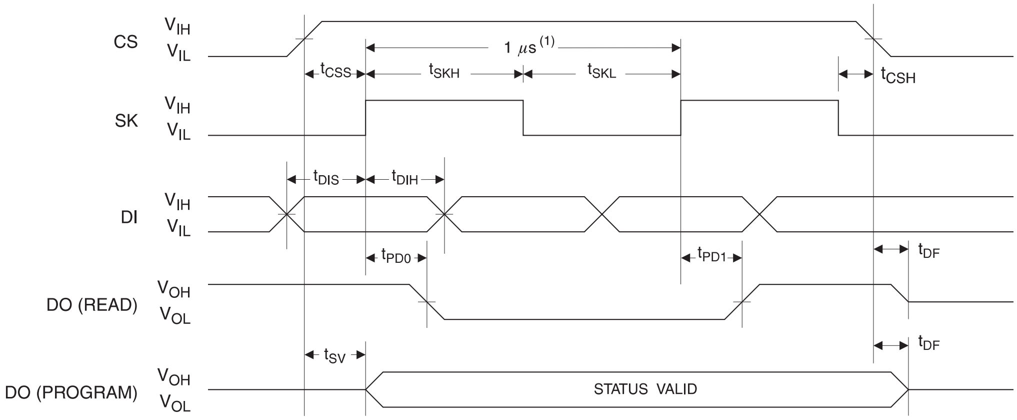
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic ‘1’ state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



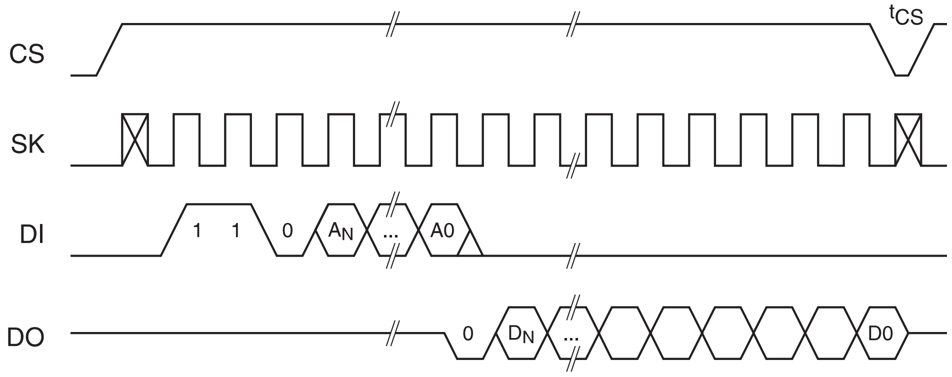
Note: 1. This is the minimum SK period.

Organization Key for Timing Diagrams

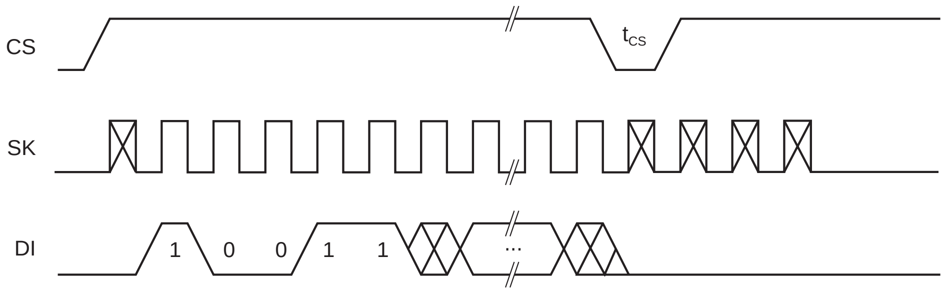
I/O	AT93C46 (1K)		AT93C56 (2K)		AT93C57 (2K)		AT93C66 (4K)	
	x 8	x 16	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_8(1)	A_7	A_7	A_6	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

Note: 1. A_8 is a DON'T CARE value, but the extra clock is required.

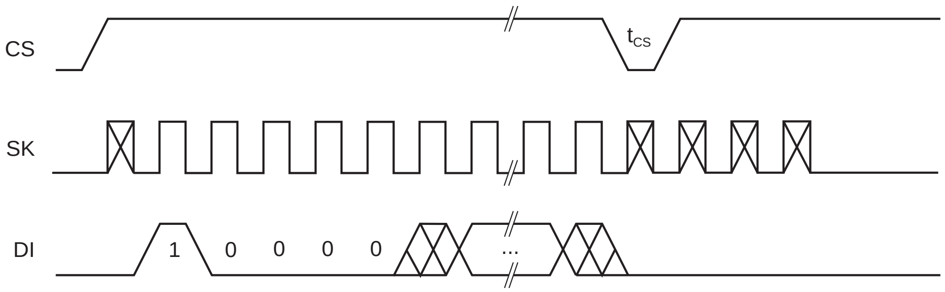
READ Timing



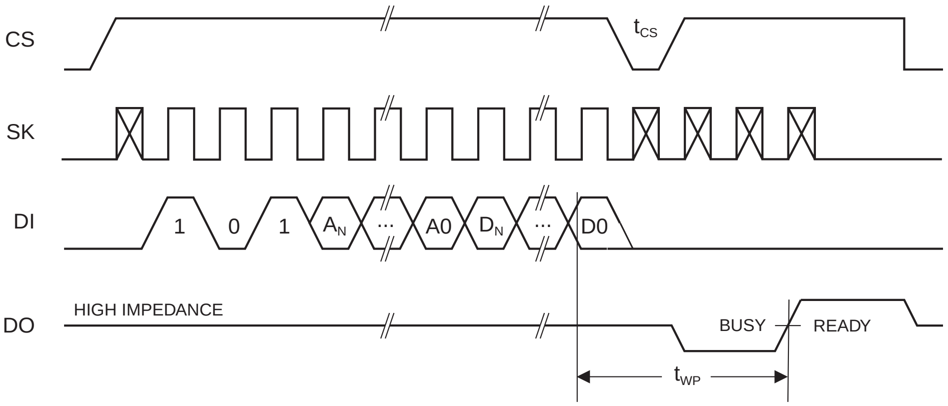
EWEN Timing



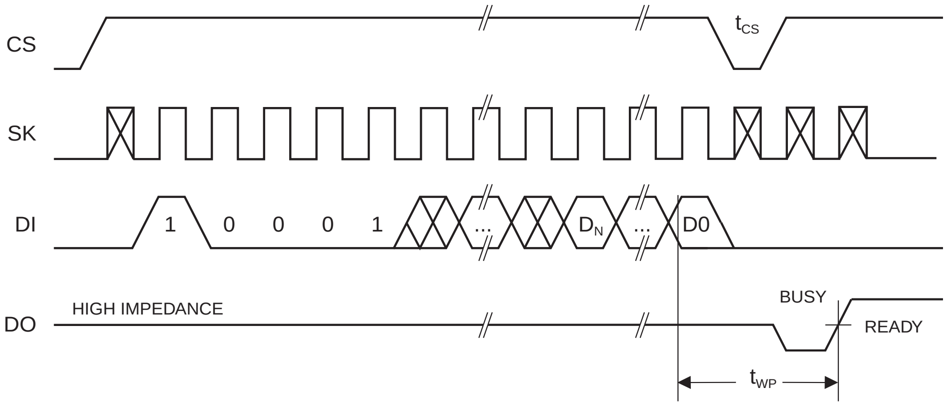
EWDS Timing



WRITE Timing

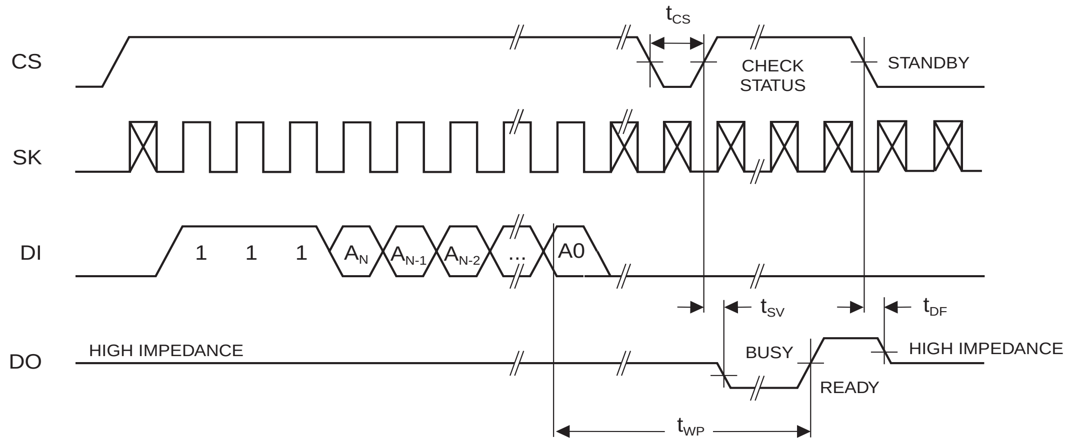


WRAL Timing(1)

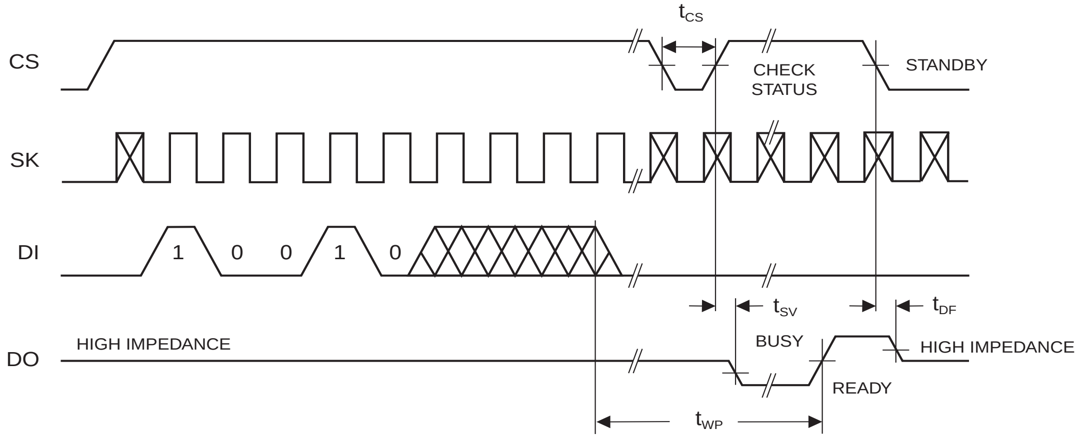


Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

ERASE Timing



TERAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

AT93C46 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C46-10PC	8P3	Commercial (0°C to 70°C)
				AT93C46-10SC	8S1	
				AT93C46R-10SC	8S1	
				AT93C46W-10SC	8S2	
				AT93C46-10TC	8T	
		30.0	2000	AT93C46-10PI	8P3	Industrial (-40°C to 85°C)
				AT93C46-10SI	8S1	
				AT93C46R-10SI	8S1	
				AT93C46W-10SI	8S2	
				AT93C46-10TI	8T	
10	800	10.0	1000	AT93C46-10PC-2.7	8P3	Commercial (0°C to 70°C)
				AT93C46-10SC-2.7	8S1	
				AT93C46R-10SC-2.7	8S1	
				AT93C46W-10SC-2.7	8S2	
				AT93C46-10TC-2.7	8T	
		10.0	1000	AT93C46-10PI-2.7	8P3	Industrial (-40°C to 85°C)
				AT93C46-10SI-2.7	8S1	
				AT93C46R-10SI-2.7	8S1	
				AT93C46W-10SI-2.7	8S2	
				AT93C46-10TI-2.7	8T	

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200” Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170” Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C46 Ordering Information (Continued)

t_{WP} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	600	10.0	500	AT93C46-10PC-2.5 AT93C46-10SC-2.5 AT93C46R-10SC-2.5 AT93C46W-10SC-2.5 AT93C46-10TC-2.5	8P3 8S1 8S1 8S2 8T	Commercial (0°C to 70°C)
		10.0	500	AT93C46-10PI-2.5 AT93C46-10SI-2.5 AT93C46R-10SI-2.5 AT93C46W-10SI-2.5 AT93C46-10TI-2.5	8P3 8S1 8S1 8S2 8T	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C46-10PC-1.8 AT93C46-10SC-1.8 AT93C46R-10SC-1.8 AT93C46W-10SC-1.8 AT93C46-10TC-1.8	8P3 8S1 8S1 8S2 8T	Commercial (0°C to 70°C)
		0.1	250	AT93C46-10PI-1.8 AT93C46-10SI-1.8 AT93C46R-10SI-1.8 AT93C46W-10SI-1.8 AT93C46-10TI-1.8	8P3 8S1 8S1 8S2 8T	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200” Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8T	8-Lead, 0.170” Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C56 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C56-10PC AT93C56-10SC AT93C56W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
		30.0	2000	AT93C56-10PI AT93C56-10SI AT93C56W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C56-10PC-2.7 AT93C56-10SC-2.7 AT93C56W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT93C56-10PI-2.7 AT93C56-10SI-2.7 AT93C56W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C56-10PC-2.5 AT93C56-10SC-2.5 AT93C56W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	500	AT93C56-10PI-2.5 AT93C56-10SI-2.5 AT93C56W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200” Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C57 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C57-10PC AT93C57-10SC AT93C57W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
		30.0	2000	AT93C57-10PI AT93C57-10SI AT93C57W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C57-10PC-2.7 AT93C57-10SC-2.7 AT93C57W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT93C57-10PI-2.7 AT93C57-10SI-2.7 AT93C57W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200” Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

AT93C66 Ordering Information

t_{WP} (max) (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C66-10PC AT93C66-10SC AT93C66W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
		30.0	2000	AT93C66-10PI AT93C66-10SI AT93C66W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C66-10PC-2.7 AT93C66-10SC-2.7 AT93C66W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT93C66-10PI-2.7 AT93C66-10SI-2.7 AT93C66W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C66-10PC-2.5 AT93C66-10SC-2.5 AT93C66W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
		10.0	500	AT93C66-10PI-2.5 AT93C66-10SI-2.5 AT93C66W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)

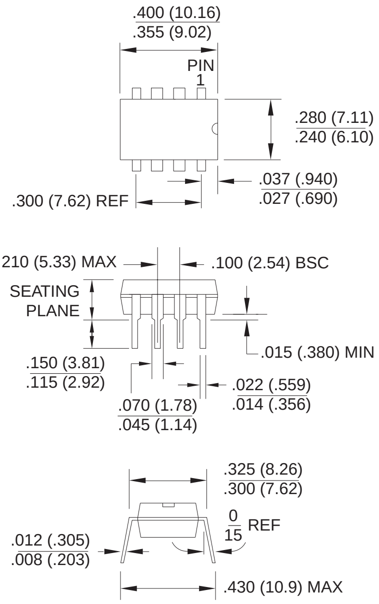
Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-Lead, 0.200” Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low Voltage (2.7V to 5.5V)
-2.5	Low Voltage (2.5V to 5.5V)
R	Rotated Pinout

Packaging Information

8P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

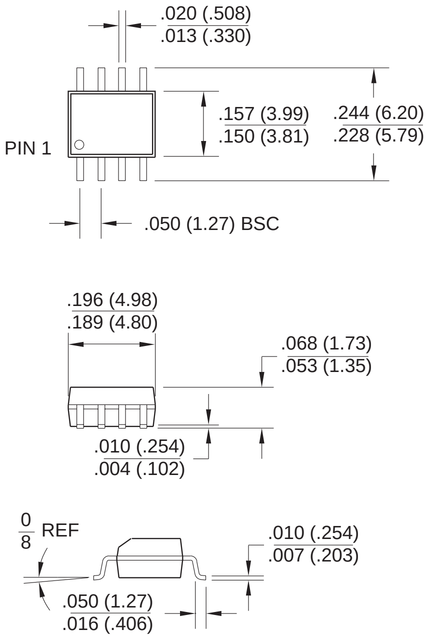
Dimensions in Inches and (Millimeters)

JEDEC STANDARD MS-001 BA



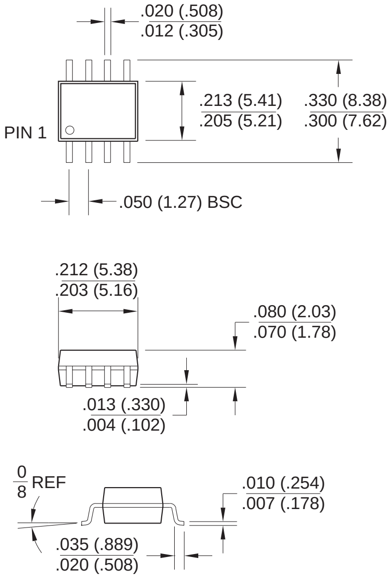
8S1, 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Dimensions in Inches and (Millimeters)



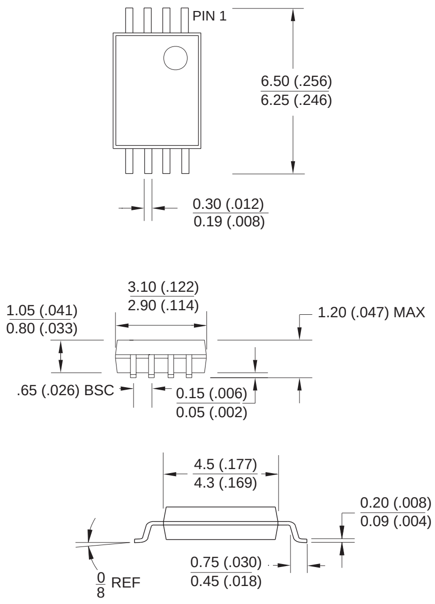
8S2, 8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)

Dimensions in Inches and (Millimeters)



8T, 8-Lead, 0.170" Wide Thin Shrink Small Outline Package (TSSOP)

Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters