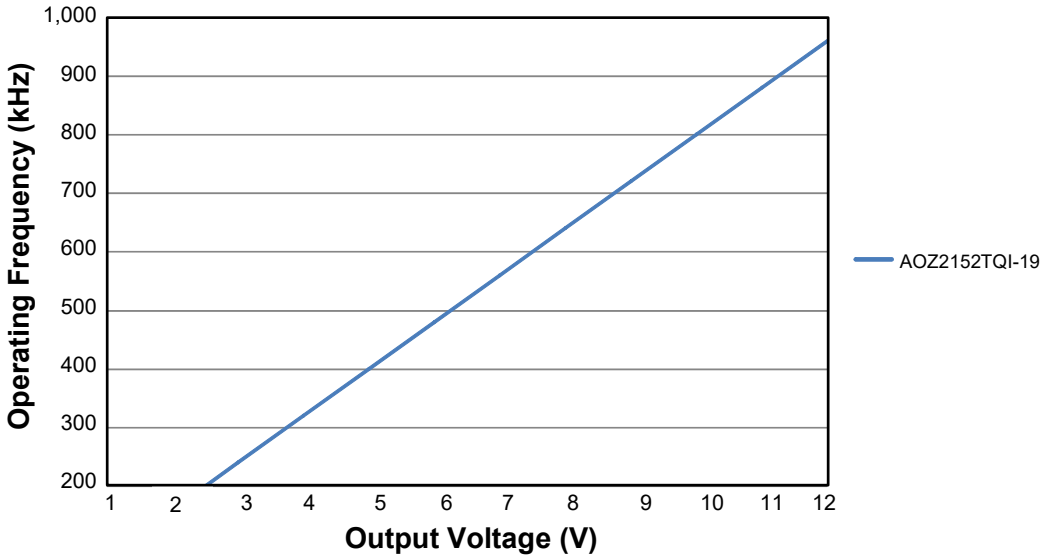
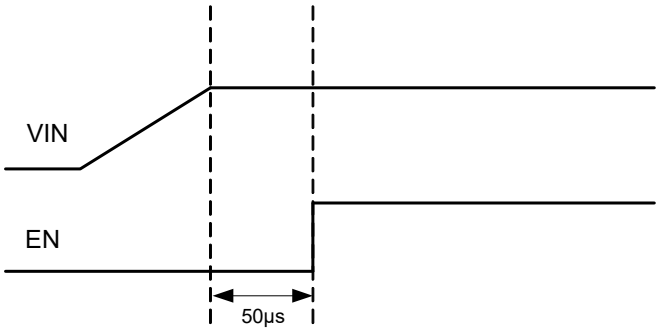
Output Voltage vs. Operating Frequency



Recommended Start-up Sequence

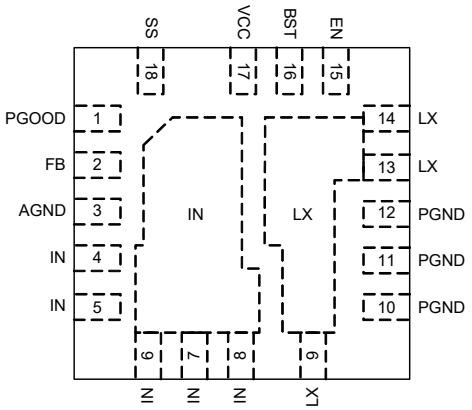


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ2151TQI-19	-40°C to +85°C	18-Pin 3mm x 3mm QFN	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



18-Pin 3mm x 3mm QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.
2	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
3	AGND	Analog Ground.
4, 5, 6, 7, 8	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
9, 13, 14	LX	Switching Node.
10, 11, 12	PGND	Power Ground.
15	EN	Enable Input. The AOZ2151TQI-19 is enabled when EN is pulled high. The device shuts down when EN is pulled low.

Pin Number	Pin Name	Pin Function
16	BST	Bootstrap Capacitor Connection. The AOZ2151TQI-19 includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in the Typical Application diagram.
17	VCC	Supply Input for analog functions. Bypass VCC to AGND with a 4.7µF~10µF ceramic capacitor. Place the capacitor close to VCC pin.
18	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
IN to AGND	-0.3V to 30V
LX to AGND(1)	-0.3V to 30V
BST to AGND	-0.3V to 36V
SS, PGOOD, FB, EN, VCC to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(2)	2kV

Notes:

1. LX to PGND Transient (t<20ns) ------- -7V to V_{IN}+7V.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating ratings.

Parameter	Rating
Supply Voltage (V_{IN})	6.5V to 28V
Output Voltage Range	0.8V to 0.85*V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance θ_{JA} θ_{JC}	 40°C/W 6°C/W

Electrical Characteristics

T_A = 25°C, V_{IN}=12V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

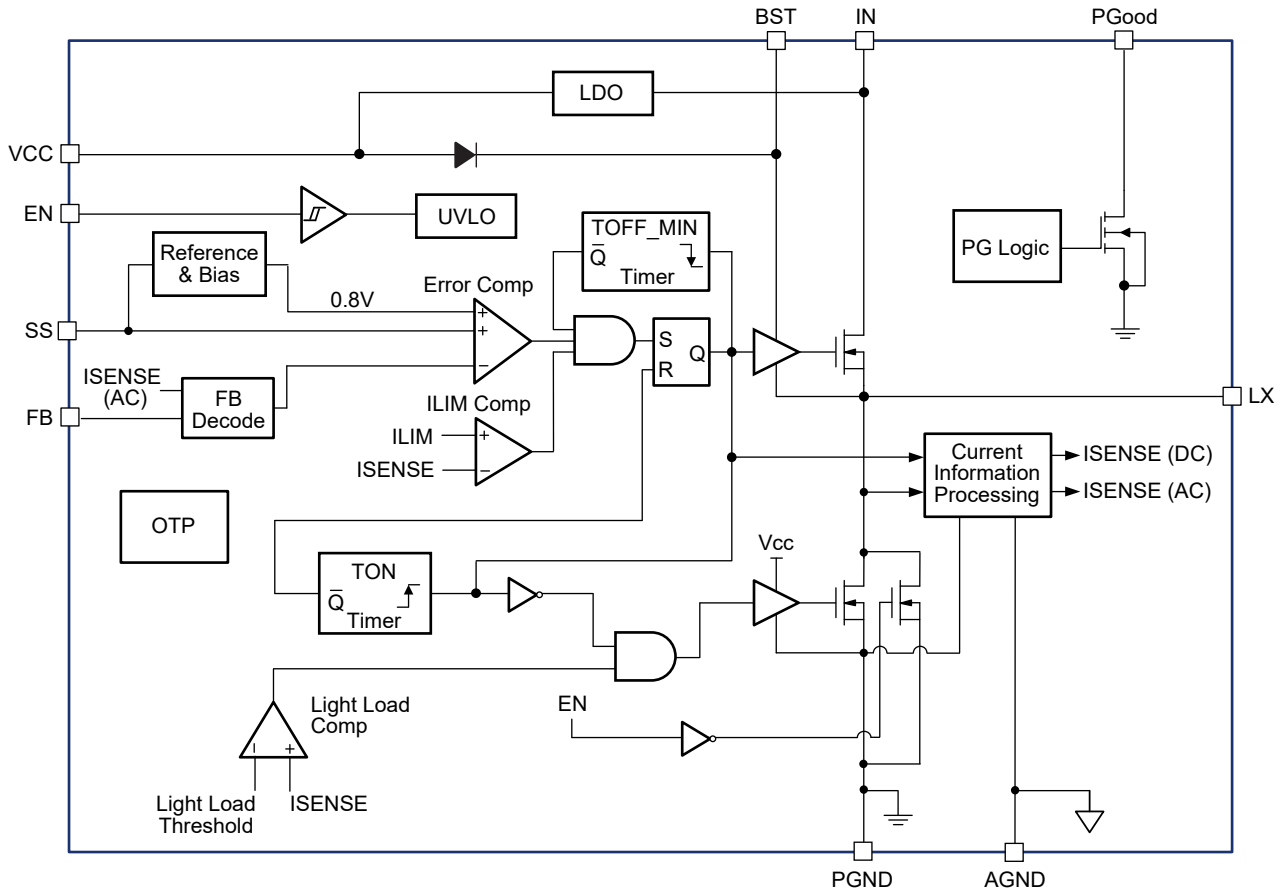
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	IN Supply Voltage		6.5		28	V
V_{UVLO}	Under-Voltage Lockout Threshold of V_{IN}	V_{IN} rising V_{IN} falling	 3.2	4.0 3.7	4.4	V
I_q	Quiescent Supply Current of V_{IN}	I_{OUT} = 0, V_{EN} > 2V, PFM		0.16		mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		15		µA
V_{FB}	Feedback Voltage	T_A = 25°C T_A = 0°C to 85°C	0.792 0.788	0.800 0.800	0.808 0.812	V
	Load Regulation			0.5		%
	Line Regulation			1		%
I_{FB}	FB Input Bias Current				200	nA
Enable						
V_{EN}	EN Input Threshold	Off threshold On threshold	 1.4		0.5	V
V_{EN_HYS}	EN Input Hysteresis			100		mV
Modulator						
T_{ON_MIN}	Minimum On Time			60		ns
T_{OFF_MIN}	Minimum Off Time			300		ns
Soft-Start						
I_{SS_OUT}	SS Source Current	V_{SS} = 0 C_{SS} = 0.001µF to 0.1µF	7	11	15	µA

Electrical Characteristics

T_A = 25°C, V_{IN}=12V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			0.5	V
	PGOOD Leakage Current				±1	µA
V_{PGH}	PGOOD Threshold (Low Level to High Level)	FB rising		90		%
V_{PGL}	PGOOD Threshold (High Level to Low Level)	FB rising FB falling		120 85		%
	PGOOD Threshold Hysteresis			5		%
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	FB falling		70		%
T_{PL}	Under Voltage Delay Time			32		µs
V_{PH}	Over Voltage Threshold	FB rising		120		%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	V_{IN} = 12V		28		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 12V		28		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Over-current and Thermal Protection						
I_{LIM}	Current Limit		6			A
	Thermal Shutdown Threshold	T_J rising T_J falling		150 100		°C

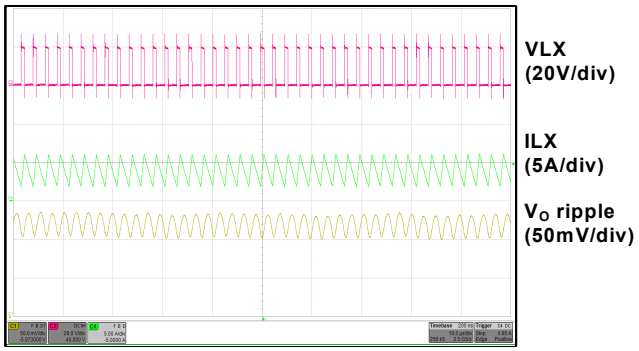
Functional Block Diagram



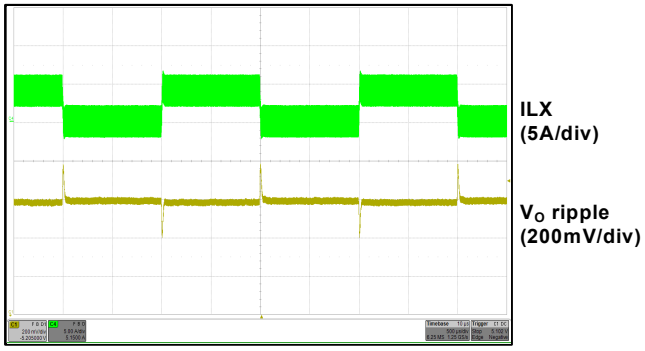
Typical Performance Characteristics

Circuit of Typical Application. T_A = 25°C, V_{IN} = 19V, V_{OUT} = 5V, unless otherwise specified.

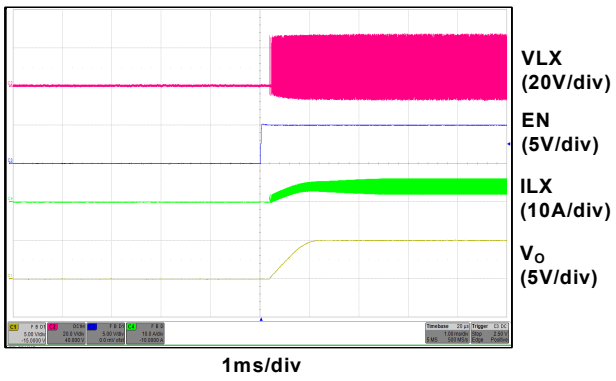
Normal Operation



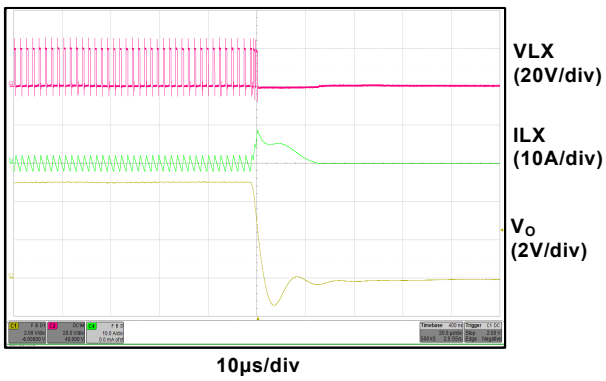
Load Transient 0A to 4A



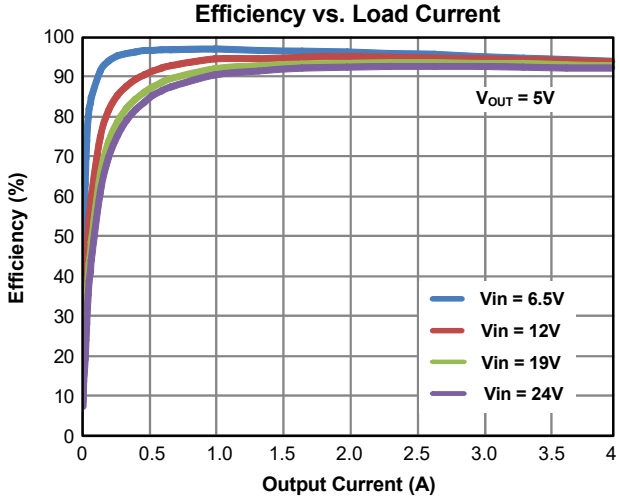
Full Load Start-up



Short Circuit Protection



Efficiency vs. Load Current



Detailed Description

The AOZ2151TQI-19 is a high-efficiency, easy-to-use, synchronous buck regulator optimized for notebook computers. The regulator is capable of supplying 4A of continuous output current with an output voltage adjustable down to 0.8V.

The input voltage of AOZ2151TQI-19 can be as low as 6.5V. The highest input voltage of AOZ2151TQI-19 can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with ceramics output capacitor. Protection features include V_{CC} under-voltage lockout, current limit, output over voltage and under voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2151TQI-19 is available in 18-pin 3mmx3mm QFN package.

Input Power Architecture

The AOZ2151TQI-19 integrates an internal linear regulator to generate 5.3V (±5%) V_{CC} from input. If input voltage is lower than 5.3V, the linear regulator operates at low drop-output mode; the V_{CC} voltage is equal to input voltage minus the drop-output voltage of internal linear regulator.

Soft Start

The AOZ2151TQI-19 has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when V_{CC} rises to 4.5V and voltage on EN pin is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of soft-start pin (V_{SS}) when it is lower than 0.8V. When V_{SS} is higher than 0.8V, the FB voltage is regulated by internal precise band-gap voltage (0.8V). When V_{SS} is higher than 3.3V, the PGOOD signal is high. The soft-start time for PGOOD can be calculated by the following formula:

$T_{SS}(\mu s) = 330 \times C_{SS}(nF)$

If C_{SS} is 1nF, the soft-start time will be 330µ second; if C_{SS} is 10nF, the soft-start time will be 3.3m second.

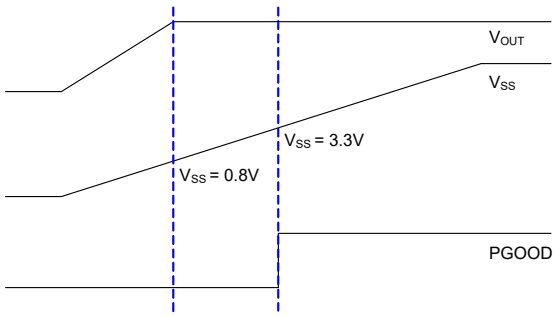


Figure 1. Soft Start Sequence

Enable

The AOZ2151TQI-19 has an embedded discharge path, including a 100kΩ resistor and an M1 NMOS device. This discharge path is activated when V_{IN}(Input Voltage) is high and V_{EN}(Enable Voltage) is low. The internal circuit of EN pin is shown in Figure 2.

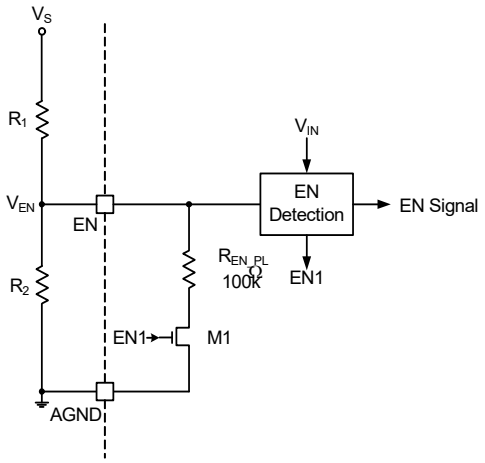


Figure 2. Enable Internal Circuit

There are two different enable control methods:

1. Connection to EN pin by an external resistor divider.
2. Direct connection to EN pin by an external power source, Vs.

In the first condition, we must consider the internal pull down resistance by using a divider circuit with an external power source V_s and get V_{EN}, the V_{EN} can be calculated by the following formula:

$$V_{en} = \frac{R_2 // R_{EN\_PL}}{R_1 + (R_2 // R_{EN+PL})} \cdot V_s$$

When the V_{IN} is high and V_{EN} is high, the EN internal M1 is turned off, and then the pull down resistance is removed for V_{EN}, the V_{EN} can be re-calculated by:

$$V_{en} = \frac{R_2}{R_1 + R_2} \cdot V_S$$

In the second condition, the AOZ2151TQI-19 will be turned on when the V_{EN} is higher than 1.4V, and will be turned off when the V_{EN} is lower than 0.5V. The simplified schematic and timing sequence are shown in Figure 3.

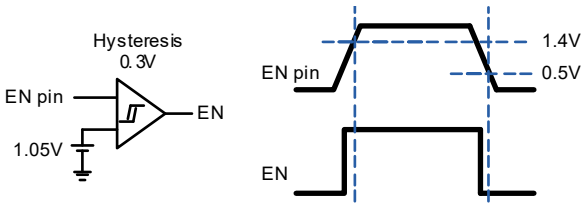


Figure 3. Enable Threshold Schematic and Timing Sequence

Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of AOZ2151TQI-19 is constant-on-time PWM control with input feed-forward. The simplified control schematic is shown in Figure 4. The high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage (IN). The one-shot is triggered when the internal 0.8V is higher than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed lower-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on time control schemes.

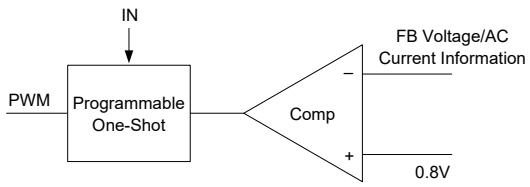


Figure 4. Simplified Control Schematic

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The AOZ2151TQI-19 senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus, the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Current-Limit Protection

The AOZ2151TQI-19 has the current-limit protection by using $R_{DS(ON)}$ of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off (300ns typical) is implemented after a constant-on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 8 switching cycles, the AOZ2151TQI-19 considers this is a true failed condition and thus turns-off both high-side and low-side MOSFETs and shuts down. The AOZ2151TQI-19 enters hiccup mode to periodically restart the part. When the current limit protection is removed, the AOZ2151TQI-19 exits hiccup mode.

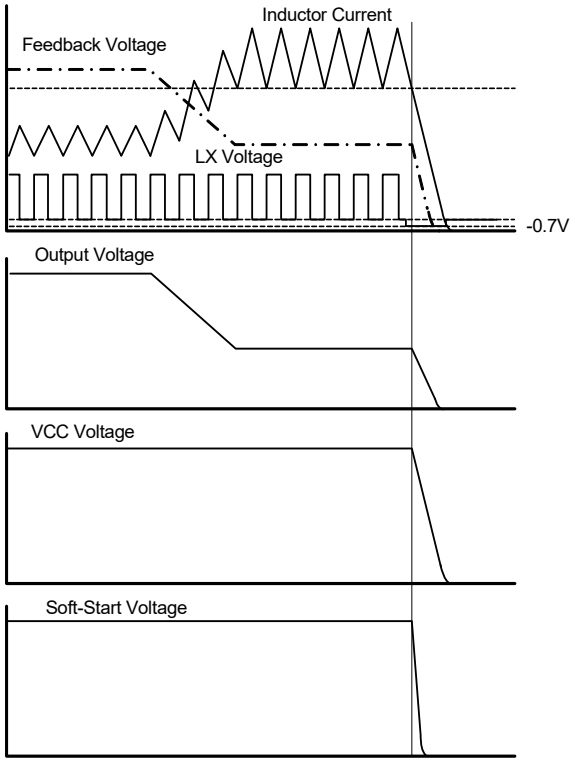


Figure 5. OCP Timing Chart

Output Voltage Under-voltage Protection

If the output voltage is lower than 70% by over-current or short circuit, AOZ2151TQI-19 will wait for 32µs (typical) and turns-off both high-side and low-side MOSFETs shuts down. The AOZ2151TQI-19 enters hiccup mode to periodically restart the part. When the current limit protection is removed, the AOZ2151TQI-19 exits hiccup mode.

Output Voltage Over-voltage Protection

The threshold of OVP is set 20% higher than 800mV. When the VFB voltage exceeds the OVP threshold, high-side MOSFET is turned off and low-side MOSFET is turned on until VFB voltage is lower than 800mV.

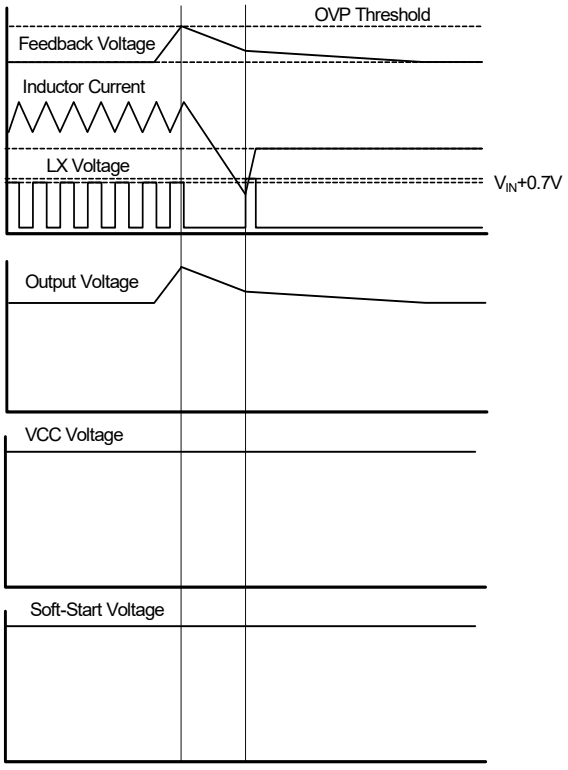


Figure 6. OVP Timing Chart

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 15% below than the nominal regulation voltage for, the PGOOD is pulled low. When the output voltage is 20% higher than the nominal regulation voltage, the PGOOD is also pull low.

When combined with the under-voltage-protection circuit, this current-limit method is effective in almost every circumstance.

Application Information

The basic AOZ2151TQI-19 application circuit is shown in the Typical Application section. The component selection is explained below.

Input capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ2151TQI-19 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7µF, should be connected to the V_{CC} pin and AGND pin for stable operation of the AOZ2151TQI-19. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 7. It can be seen that when V_O is half of V_{IN}, C_{IN} it is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

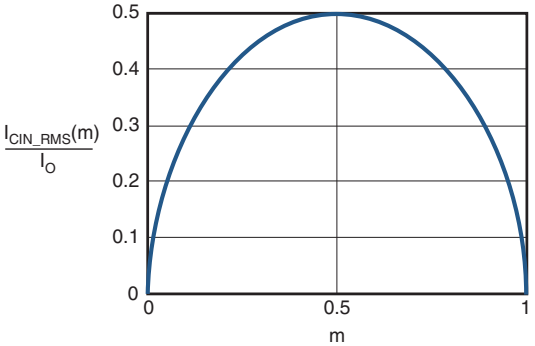


Figure 7. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where, C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be over-stressed.

Thermal Management and Layout Consideration

In the AOZ2151TQI-19 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ2151TQI-19.

In the AOZ2151TQI-19 buck regulator circuit, the major power dissipating components are the AOZ2151TQI-19 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor and output current.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ2151TQI-19 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \cdot \Theta_{JA} + T_A$$

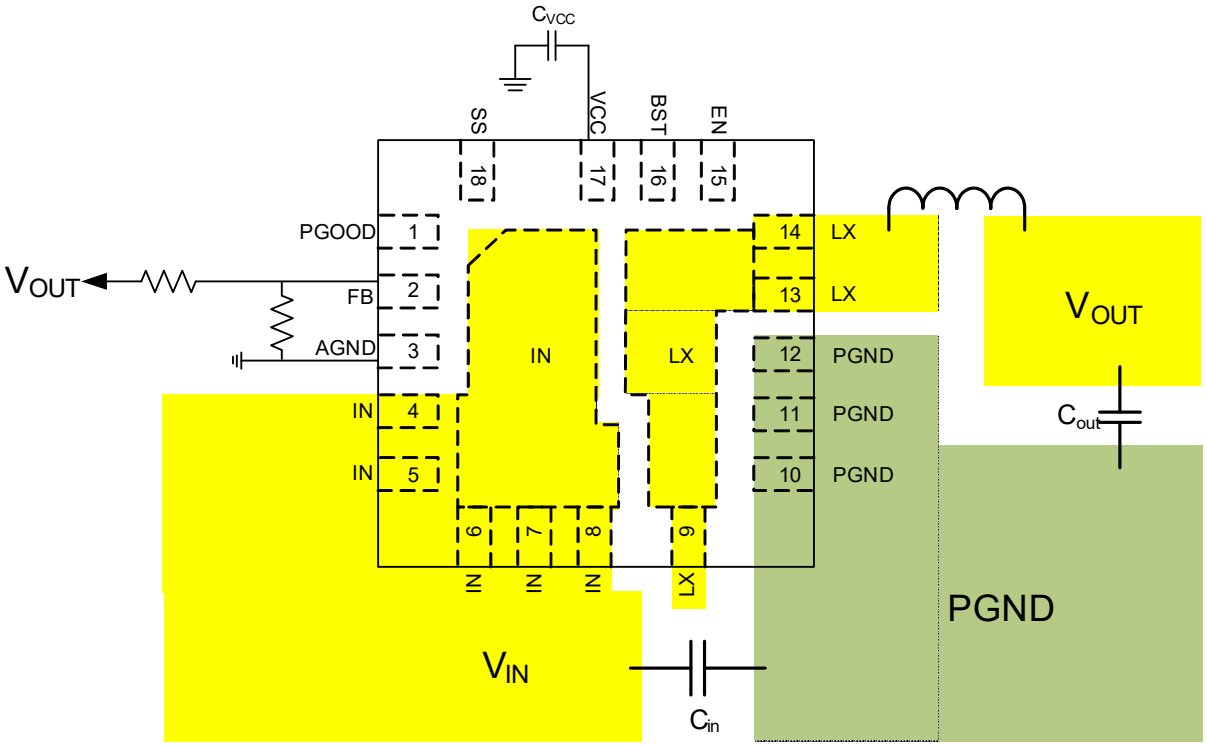
The maximum junction temperature of AOZ2151TQI-19 is 150ºC, which limits the maximum load current capability.

The thermal performance of the AOZ2151TQI-19 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

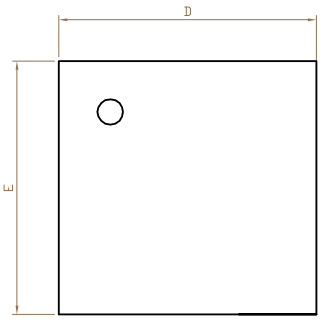
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

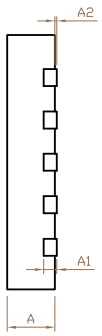
1. The LX pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to LX pin to help thermal dissipation.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor C_{VCC} should be connected to V_{CC} and AGND as close as possible.
5. Voltage divider R1 and R2 should be placed as close as possible to FB and AGND.
6. Keep sensitive signal traces such as feedback trace far away from the LX pins.
7. Pour copper plane on all unused board area and connect it to stable DC nodes, like V_{IN}, GND or V_{OUT}.



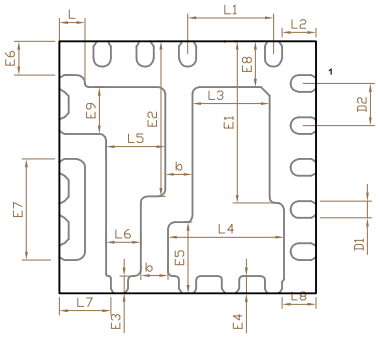
Package Dimensions, QFN 3x3, 18 Lead EP2_S



TOP VIEW

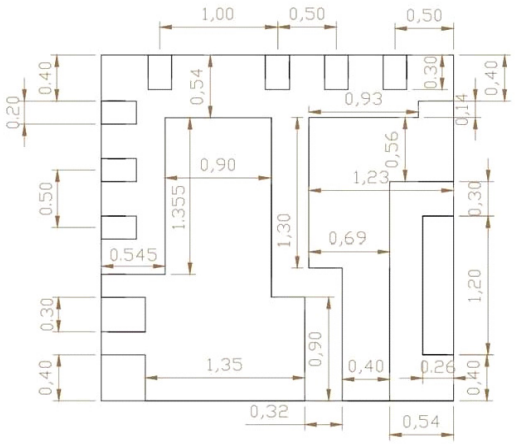


SIDE VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN



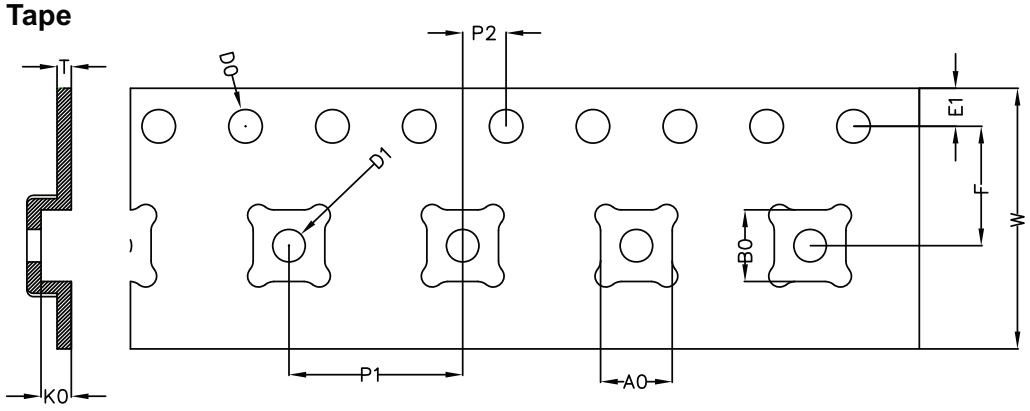
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.55	0.9	0.018	0.022	0.026
A1	0.10	0.15	0.25	0.00		0.008
A2		0.020REF			0.001REF	
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.82	1.92	2.02	0.072	0.076	0.080
E2	1.74	1.84	1.94	0.069	0.072	0.076
E3	0.17	0.21	0.31	0.007	0.008	0.012
E4	0.17	0.21	0.31	0.007	0.008	0.012
E5	0.75	0.85	0.95	0.030	0.033	0.037
E6	0.35	0.40	0.45	0.014	0.016	0.018
E7	1.10	1.20	1.30	0.043	0.047	0.051
E8	0.49	0.54	0.59	0.019	0.021	0.023
E9	0.51	0.56	0.61	0.020	0.022	0.024
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	0.15	0.20	0.25	0.006	0.008	0.010
D2	0.45	0.50	0.55	0.01	0.02	0.022
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.90	1.00	1.10	0.035	0.039	0.043
L2	0.35	0.40	0.45	0.014	0.016	0.018
L3	0.80	0.90	1.00	0.031	0.035	0.039
L4	1.26	1.36	1.46	0.05	0.05	0.057
L5	0.64	0.69	0.74	0.025	0.027	0.029
L6	0.35	0.40	0.45	0.014	0.016	0.018
L7	0.55	0.60	0.65	0.022	0.024	0.026
L8	0.35	0.40	0.45	0.014	0.016	0.018
b	0.27	0.32	0.37	0.011	0.013	0.015

NOTE
CONTROLLING DIMENSIONS IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN 3x3, 18 Lead EP2_S

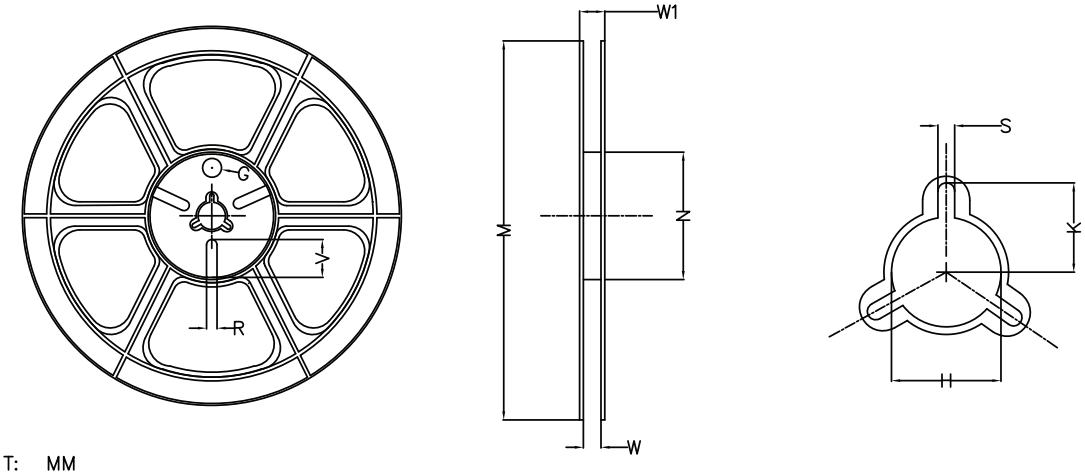
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E1	F	P0	P1	P2	T
QFN3X3_18L	3.30 ±0.10	3.30 ±0.10	0.80 ±0.10	1.55 ±0.05	1.50 Min.	12.00 +0.30 −0.00	1.75 ±0.10	5.50 ±0.10	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	0.30 ±0.05

Reel

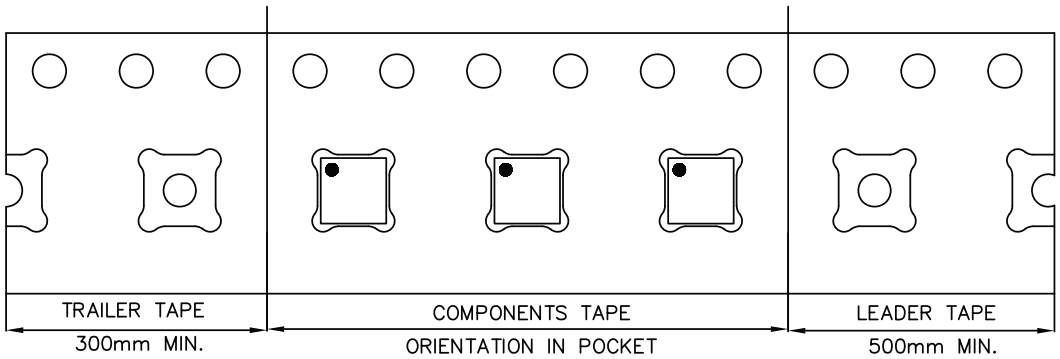


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	S	K	G	R	V
12 mm	ø330	ø330.00 ±2.00	ø101.6 ±2.00	12.40 +2.00 −0.00	12.40 +3.00 −0.20	ø13.20 ±0.30	1.70–2.60	---	---	---	---

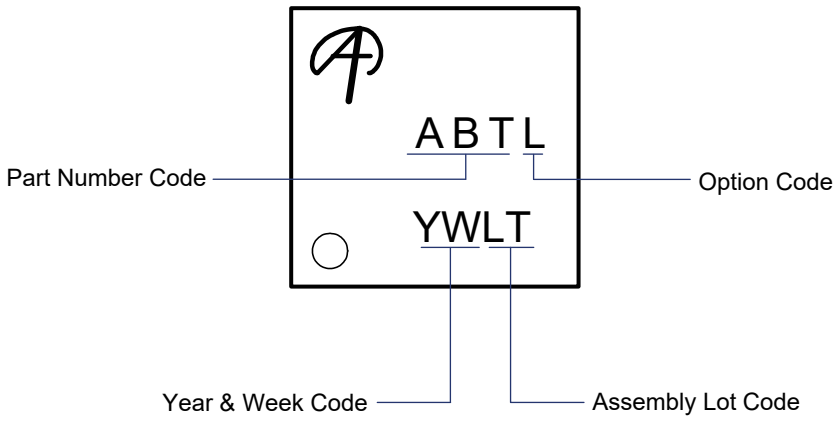
Leader/Trailer & Orientation

Unit Per Reel:
5000pcs



Part Marking

AOZ22151TQI-19
(QFN 3x3)



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.