AMP04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 5 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP04E Min	AMP04E Typ	AMP04E Max	AMP04F Min	AMP04F Typ	AMP04F Max	Unit
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			30	150			300	µV
		–40°C ≤ T_A ≤ +85°C			300			600	µV
Input Offset Voltage Drift	TCV_{IOS}				3			6	µV/°C
Output Offset Voltage	V_{OOS}			0.5	1.5			3	mV
		–40°C ≤ T_A ≤ +85°C			3			6	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	µV/°C
INPUT CURRENT									
Input Bias Current	I_B			22	30			40	nA
		–40°C ≤ T_A ≤ +85°C			50			60	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			1	5			10	nA
		–40°C ≤ T_A ≤ +85°C			10			15	nA
Input Offset Current Drift	TCI_{OS}			8			8		pA/°C
INPUT									
Common-Mode Input Resistance				4			4		GΩ
Differential Input Resistance				4			4		GΩ
Input Voltage Range	V_{IN}		0		3.0	0		3.0	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100	90	105		80			dB
		G = 1000	90	105		80			dB
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 2.5 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100	85			75			dB
		G = 1000	85			75			dB
Power Supply Rejection	PSRR	4.0 V ≤ V_S ≤ 12 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 1	95			85			dB
		G = 10	105			95			dB
		G = 100	105			95			dB
		G = 1000	105			95			dB
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1 to 100							
		–40°C ≤ T_A ≤ +85°C			0.8			1.0	%
		G = 1000		0.4			0.75		%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005					%
		G = 10, R_L = 5 kΩ		0.015					%
		G = 100, R_L = 5 kΩ		0.025					%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	4.0	4.2		4.0			V
		R_L = 2 kΩ							
		–40°C ≤ T_A ≤ +85°C	3.8			3.8			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ							
		–40°C ≤ T_A ≤ +85°C			2.0			2.5	mV
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA

Parameter	Symbol	Conditions	AMP04E Min	AMP04E Typ	AMP04E Max	AMP04F Min	AMP04F Typ	AMP04F Max	Unit
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/√Hz
		f = 1 kHz, G = 10		45			45		nV/√Hz
		f = 100 Hz, G = 100		30			30		nV/√Hz
		f = 100 Hz, G = 1000		25			25		nV/√Hz
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/√Hz
Input Noise Voltage	e_N p-p	0.1 Hz to 10 Hz, G = 1		7			7		µV p-p
		0.1 Hz to 10 Hz, G = 10		1.5			1.5		µV p-p
		0.1 Hz to 10 Hz, G = 100		0.7			0.7		µV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, –3 dB		300			300		kHz
POWER SUPPLY									
Supply Current	I_{SY}			550	700			700	µA
		–40°C ≤ T_A ≤ +85°C			850			850	µA

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP04E Min	AMP04E Typ	AMP04E Max	AMP04F Min	AMP04F Typ	AMP04F Max	Unit
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			80	400			600	µV
		–40°C ≤ T_A ≤ +85°C			600			900	µV
Input Offset Voltage Drift	TCV_{IOS}				3			6	µV/°C
Output Offset Voltage	V_{OOS}			1	3			6	mV
		–40°C ≤ T_A ≤ +85°C			6			9	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	µV/°C
INPUT CURRENT									
Input Bias Current	I_B			17	30			40	nA
		–40°C ≤ T_A ≤ +85°C			50			60	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			2	5			10	nA
		–40°C ≤ T_A ≤ +85°C			15			20	nA
Input Offset Current Drift	TCI_{OS}			28			28		pA/°C
INPUT									
Common-Mode Input Resistance				4			4		GΩ
Differential Input Resistance				4			4		GΩ
Input Voltage Range	V_{IN}		–12		+12	–12		+12	V
Common-Mode Rejection	CMR	–12 V ≤ V_{CM} ≤ +12 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100	90	105		80			dB
		G = 1000	90	105		80			dB
Common-Mode Rejection	CMR	–11 V ≤ V_{CM} ≤ +11 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100	85			75			dB
		G = 1000	85			75			dB
Power Supply Rejection	PSRR	±2.5 V ≤ V_S ≤ ±18 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 1	75			70			dB
		G = 10	90			80			dB
		G = 100	95			85			dB
		G = 1000	95			85			dB

Parameter	Symbol	Conditions	AMP04E Min	AMP04E Typ	AMP04E Max	AMP04F Min	AMP04F Typ	AMP04F Max	Unit
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1000		0.4			0.75		%
		G = 1 to 100 –40°C ≤ T_A ≤ +85°C			0.8			1.0	%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005			0.005		%
		G = 10, R_L = 5 kΩ		0.015			0.015		%
		G = 100, R_L = 5 kΩ		0.025			0.025		%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	13	13.4		13			V
		R_L = 2 kΩ –40°C ≤ T_A ≤ +85°C	12.5			12.5			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ –40°C ≤ T_A ≤ +85°C			–14.5			–14.5	V
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/√Hz
		f = 1 kHz, G = 10		45			45		nV/√Hz
		f = 100 Hz, G = 100		30			30		nV/√Hz
		f = 100 Hz, G = 1000		25			25		nV/√Hz
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/√Hz
Input Noise Voltage	e_N p-p	0.1 Hz to 10 Hz, G = 1		5			5		µV p-p
		0.1 Hz to 10 Hz, G = 10		1			1		µV p-p
		0.1 Hz to 10 Hz, G = 100		0.5			0.5		µV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, –3 dB		700			700		kHz
POWER SUPPLY									
Supply Current	I_{SY}			750	900			900	µA
		–40°C ≤ T_A ≤ +85°C			1100			1100	µA

Specifications subject to change without notice.

WAFER TEST LIMITS (V_S = 5 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Unit
OFFSET VOLTAGE				
Input Offset Voltage	V_{IOS}		300	µV max
Output Offset Voltage	V_{OOS}		3	mV max
INPUT CURRENT				
Input Bias Current	I_B		40	nA max
Input Offset Current	I_{OS}		10	nA max
INPUT				
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V		
		G = 1	55	dB min
		G = 10	75	dB min
		G = 100	80	dB min
		G = 1000	80	dB min
Common-Mode Rejection	CMR	V_S = ±15 V, –12 V ≤ V_{CM} ≤ +12 V		
		G = 1	55	dB min
		G = 10	75	dB min
		G = 100	80	dB min

Parameter	Symbol	Conditions	Limit	Unit
Power Supply Rejection	PSRR	G = 1000 4.0 V ≤ V_S ≤ 12 V	80	dB min
		G = 1	85	dB min
		G = 10	95	dB min
		G = 100	95	dB min
		G = 1000	95	dB min
GAIN (G = 100 K/R_{GAIN}) Gain Equation Accuracy		G = 1 to 100	0.75	% max
OUTPUT Output Voltage Swing High Output Voltage Swing Low	 V_{OH} V_{OL}	 R_L = 2 kΩ R_L = 2 kΩ	 4.0 2.5	 V min mV max
POWER SUPPLY Supply Current	 I_{SY}	 V_S = ±15	 900 700	 µA max µA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage[2] . . . . . ±18 V
Differential Input Voltage . . . . . 36 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range

P, S Package . . . . . –65°C to +150°C
Operating Temperature Range

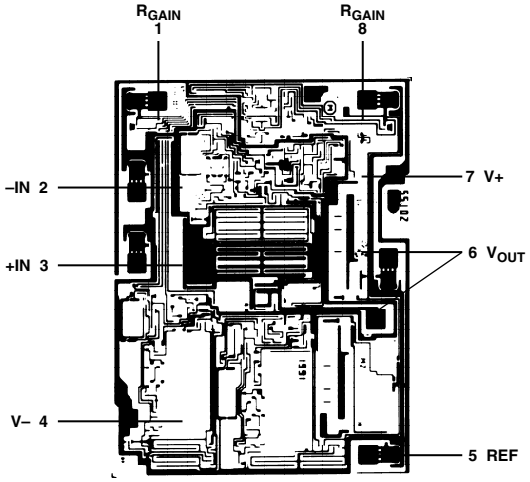
AMP04E, F . . . . . –40°C to +85°C
Junction Temperature Range

P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for a P-DIP package; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



AMP04 Die Size 0.075 × 0.99 inch, 7,425 sq. mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 81.

APPLICATIONS

Common-Mode Rejection

The purpose of the instrumentation amplifier is to amplify the difference between the two input signals while ignoring offset and noise voltages common to both inputs. One way of judging the device's ability to reject this offset is the common-mode gain, which is the ratio between a change in the common-mode voltage and the resulting output voltage change. Instrumentation amplifiers are often judged by the common-mode rejection ratio, which is equal to $20 \times \log_{10}$ of the ratio of the user-selected differential signal gain to the common-mode gain, commonly called the CMRR. The AMP04 offers excellent CMRR, guaranteed to be greater than 90 dB at gains of 100 or greater. Input offsets attain very low temperature drift by proprietary laser-trimmed thin-film resistors and high gain amplifiers.

Input Common-Mode Range Includes Ground

The AMP04 employs a topology (Figure 1) that uniquely allows the common-mode input voltage to truly extend to zero volts where other instrumentation amplifiers fail. To illustrate, take for example the single supply, gain of 100 instrumentation amplifier as in Figure 2. As the inputs approach zero volts, in order for the output to go positive, amplifier A's output (V_{OA}) must be allowed to go below ground, to –0.094 volts. Clearly this is not possible in a single supply environment. Consequently this instrumentation amplifier configuration's input common-mode voltage cannot go below about 0.4 volts. In comparison, the AMP04 has no such restriction. Its inputs will function with a zero-volt common-mode voltage.

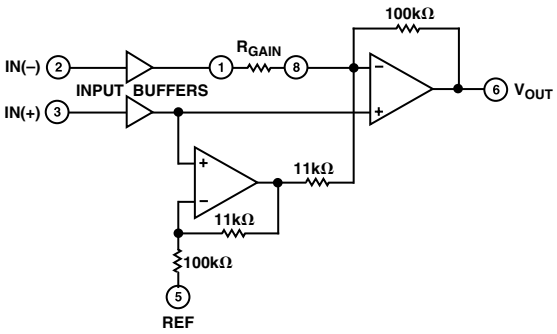


Figure 1. Functional Block Diagram

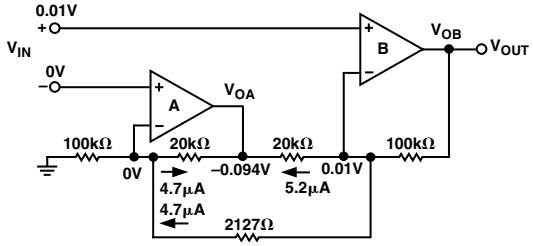


Figure 2. Gain = 100 Instrumentation Amplifier

Input Common-Mode Voltage Below Ground

Although not tested and guaranteed, the AMP04 inputs are biased in a way that they can amplify signals linearly with common-mode voltage as low as –0.25 volts below ground. This holds true over the industrial temperature range from –40°C to +85°C.

Extended Positive Common-Mode Range

On the high side, other instrumentation amplifier configurations, such as the three op amp instrumentation amplifier, can have severe positive common-mode range limitations. Figure 3 shows an example of a gain of 1001 amplifier, with an input common-mode voltage of 10 volts. For this circuit to function, V_{OB} must swing to 15.01 volts in order for the output to go to 10.01 volts. Clearly no op amp can handle this swing range (given a 15 V supply) as the output will saturate long before it reaches the supply rails. Again the AMP04's topology does not have this limitation. Figure 4 illustrates the AMP04 operating at the same common-mode conditions as in Figure 3. None of the internal nodes has a signal high enough to cause amplifier saturation. As a result, the AMP04 can accommodate much wider common-mode range than most instrumentation amplifiers.

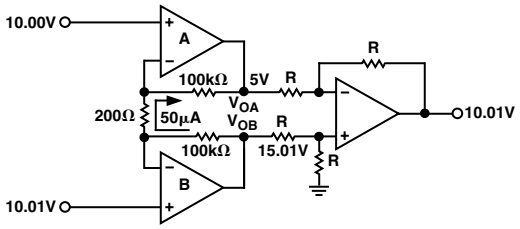


Figure 3. Gain = 1001, Three Op Amp Instrumentation Amplifier

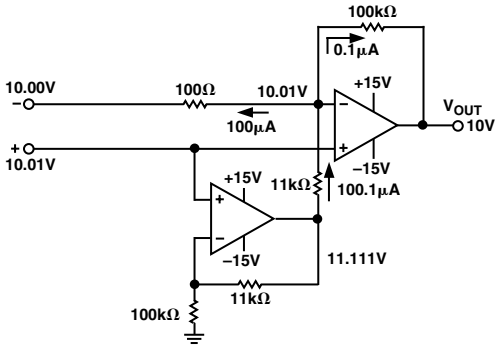


Figure 4. Gain = 1000, AMP04

Programming the Gain

The gain of the AMP04 is programmed by the user by selecting a single external resistor—R_{GAIN}:

$$Gain = 100\ k\Omega/R_{GAIN}$$

The output voltage is then defined as the differential input voltage times the gain.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times Gain$$

In single supply systems, offsetting the ground is often desired for several reasons. Ground may be offset from zero to provide a quieter signal reference point, or to offset "zero" to allow a unipolar signal range to represent both positive and negative values.

In noisy environments such as those having digital switching, switching power supplies or externally generated noise, ground may not be the ideal place to reference a signal in a high accuracy system.

Often, real world signals such as temperature or pressure may generate voltages that are represented by changes in polarity. In a single supply system the signal input cannot be allowed to go below ground, and therefore the signal must be offset to accommodate this change in polarity. On the AMP04, a reference input pin is provided to allow offsetting of the input range.

The gain equation is more accurately represented by including this reference input.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times Gain + V_{REF}$$

Grounding

The most common problems encountered in high performance analog instrumentation and data acquisition system designs are found in the management of offset errors and ground noise. Primarily, the designer must consider temperature differentials and thermocouple effects due to dissimilar metals, IR voltage drops, and the effects of stray capacitance. The problem is greatly compounded when high speed digital circuitry, such as that accompanying data conversion components, is brought into the proximity of the analog section. Considerable noise and error contributions such as fast-moving logic signals that easily propagate into sensitive analog lines, and the unavoidable noise common to digital supply lines must all be dealt with if the accuracy of the carefully designed analog section is to be preserved.

Besides the temperature drift errors encountered in the amplifier, thermal errors due to the supporting discrete components should be evaluated. The use of high quality, low-TC components where appropriate is encouraged. What is more important, large thermal gradients can create not only unexpected changes in component values, but also generate significant thermoelectric voltages due to the interface between dissimilar metals such as lead solder, copper wire, gold socket contacts, Kovar lead frames, etc. Thermocouple voltages developed at these junctions commonly exceed the TCV_{OS} contribution of the AMP04. Component layout that takes into account the power dissipation at critical locations in the circuit and minimizes gradient effects and differential common-mode voltages by taking advantage of input symmetry will minimize many of these errors.

High accuracy circuitry can experience considerable error contributions due to the coupling of stray voltages into sensitive areas, including high impedance amplifier inputs which benefit from such techniques as ground planes, guard rings, and shields. Careful circuit layout, including good grounding and signal routing practice to minimize stray coupling and ground loops is recommended. Leakage currents can be minimized by using high quality socket and circuit board materials, and by carefully cleaning and coating complete board assemblies.

As mentioned above, the high speed transition noise found in logic circuitry is the sworn enemy of the analog circuit designer. Great care must be taken to maintain separation between them to minimize coupling. A major path for these error voltages will be found in the power supply lines. Low impedance, load related variations and noise levels that are completely acceptable in the high thresholds of the digital domain make the digital supply unusable in nearly all high performance analog applications. The user is encouraged to maintain separate power and ground between the analog and digital systems wherever possible, joining only at the supply itself if necessary, and to observe careful grounding layout and bypass capacitor scheduling in sensitive areas.

Input Shield Drivers

High impedance sources and long cable runs from remote transducers in noisy industrial environments commonly experience significant amounts of noise coupled to the inputs. Both stray capacitance errors and noise coupling from external sources can be minimized by running the input signal through shielded cable. The cable shield is often grounded at the analog input common, however improved dynamic noise rejection and a reduction in effective cable capacitance is achieved by driving the shield with a buffer amplifier at a potential equal to the voltage seen at the input. Driven shields are easily realized with the AMP04. Examination of the simplified schematic shows that the potentials at the gain set resistor pins of the AMP04 follow the inputs precisely. As shown in Figure 5, shield drivers are easily realized by buffering the potential at these pins by a dual, single supply op amp such as the OP213. Alternatively, applications with single-ended sources or that use twisted-pair cable could drive a single shield. To minimize error contributions due to this additional circuitry, all components and wiring should remain in proximity to the AMP04 and careful grounding and bypassing techniques should be observed.

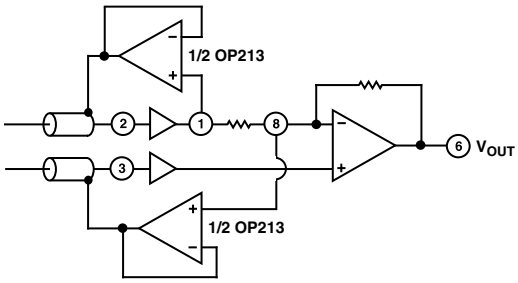


Figure 5. Cable Shield Drivers

Compensating for Input and Output Errors

To achieve optimal performance, the user needs to take into account a number of error sources found in instrumentation amplifiers. These consist primarily of input and output offset voltages and leakage currents.

The input and output offset voltages are independent from one another, and must be considered separately. The input offset component will of course be directly multiplied by the gain of the amplifier, in contrast to the output offset voltage that is independent of gain. Therefore, the output error is the dominant factor at low gains, and the input error grows to become the greater problem as gain is increased. The overall equation for offset voltage error referred to the output (RTO) is:

$$V_{OS}\,(RTO) = (V_{IOS} \times G) + V_{OOS}$$

where V_{IOS} is the input offset voltage and V_{OOS} the output offset voltage, and G is the programmed amplifier gain.

The change in these error voltages with temperature must also be taken into account. The specification TCV_{OS}, referred to the output, is a combination of the input and output drift specifications. Again, the gain influences the input error but not the output, and the equation is:

$$TCV_{OS}\,(RTO) = (TCV_{IOS} \times G) + TCV_{OOS}$$

In some applications the user may wish to define the error contribution as referred to the input, and treat it as an input error. The relationship is:

$$TCV_{OS}\,(RTI) = TCV_{IOS} + (TCV_{OOS} / G)$$

The bias and offset currents of the input transistors also have an impact on the overall accuracy of the input signal. The input leakage, or bias currents of both inputs will generate an additional offset voltage when flowing through the signal source resistance. Changes in this error component due to variations with signal voltage and temperature can be minimized if both input source resistances are equal, reducing the error to a common-mode voltage which can be rejected. The difference in bias current between the inputs, the offset current, generates a differential error voltage across the source resistance that should be taken into account in the user's design.

In applications utilizing floating sources such as thermocouples, transformers, and some photo detectors, the user must take care to provide some current path between the high impedance inputs and analog ground. The input bias currents of the AMP04, although extremely low, will charge the stray capacitance found in nearby circuit traces, cables, etc., and cause the input to drift erratically or to saturate unless given a bleed path to the analog common. Again, the use of equal resistance values will create a common input error voltage that is rejected by the amplifier.

Reference Input

The V_{REF} input is used to set the system ground. For dual supply operation it can be connected to ground to give zero volts out with zero volts differential input. In single supply systems it could be connected either to the negative supply or to a pseudo-ground between the supplies. In any case, the REF input must be driven with low impedance.

Noise Filtering

Unlike most previous instrumentation amplifiers, the output stage's inverting input (Pin 8) is accessible. By placing a capacitor across the AMP04's feedback path (Figure 6, Pins 6 and 8)

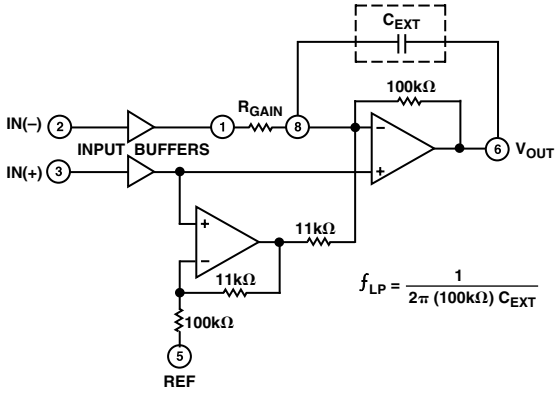


Figure 6. Noise Band Limiting

a single-pole low-pass filter is produced. The cutoff frequency (f_{LP}) follows the relationship:

$$f_{LP} = \frac{1}{2\pi\,(100\ k\Omega)\,C_{EXT}}$$

Filtering can be applied to reduce wide band noise. Figure 7a shows a 10 Hz low-pass filter, gain of 1000 for the AMP04. Figures 7b and 7c illustrate the effect of filtering on noise. The photo in Figure 7b shows the output noise before filtering. By adding a 0.15 µF capacitor, the noise is reduced by about a factor of 4 as shown in Figure 7c.

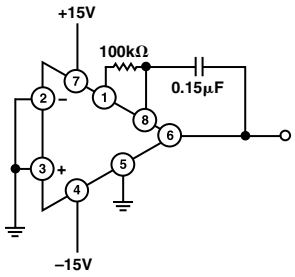


Figure 7a. 10 Hz Low-Pass Filter

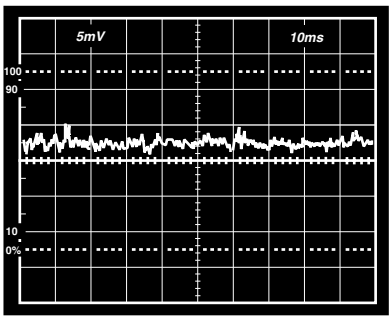


Figure 7b. Unfiltered AMP04 Output

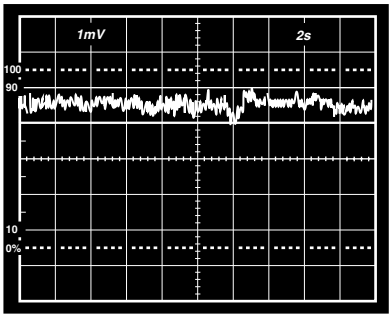


Figure 7c. 10 Hz Low-Pass Filtered Output

Power Supply Considerations

In dual supply applications (for example ±15 V) if the input is connected to a low resistance source less than 100 Ω, a large current may flow in the input leads if the positive supply is applied before the negative supply during power-up. A similar condition may also result upon a loss of the negative supply. If these conditions could be present in you system, it is recommended that a series resistor up to 1 kΩ be added to the input leads to limit the input current.

This condition can not occur in a single supply environment as losing the negative supply effectively removes any current return path.

Offset Nulling in Dual Supply

Offset may be nulled by feeding a correcting voltage at the V_{REF} pin (Pin 5). However, it is important that the pin be driven with a low impedance source. Any measurable resistance will degrade the amplifier's common-mode rejection performance as well as its gain accuracy. An op amp may be used to buffer the offset null circuit as in Figure 8.

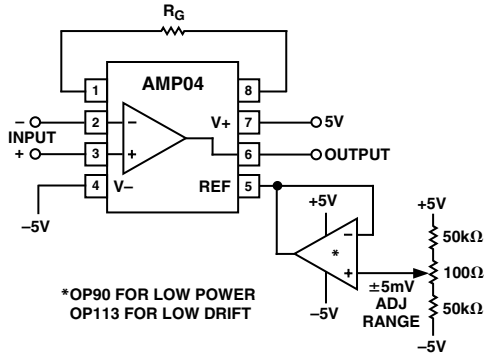


Figure 8. Offset Adjust for Dual Supply Applications

Offset Nulling in Single Supply

Nulling the offset in single supply systems is difficult because the adjustment is made to try to attain zero volts. At zero volts out, the output is in saturation (to the negative rail) and the output voltage is indistinguishable from the normal offset error. Consequently the offset nulling circuit in Figure 9 must be used with caution.

First, the potentiometer should be adjusted to cause the output to swing in the positive direction; then adjust it in the reverse direction, causing the output to swing toward ground, until the output just stops changing. At that point the output is at the saturation limit.

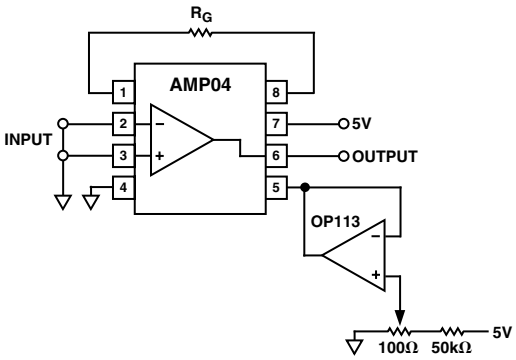


Figure 9. Offset Adjust for Single Supply Applications

Alternative Nulling Method

An alternative null correction technique is to inject an offset current into the summing node of the output amplifier as in Figure 10. This method does not require an external op amp. However, the drawback is that the amplifier will move off its null as the input common-mode voltage changes. It is a less desirable nulling circuit than the previous method.

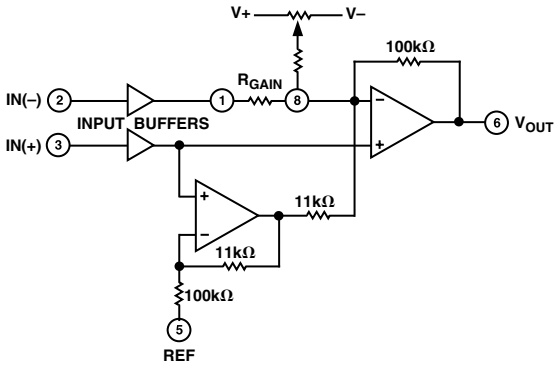


Figure 10. Current Injection Offsetting Is Not Recommended

APPLICATION CIRCUITS

Low Power Precision Single Supply RTD Amplifier

Figure 11 shows a linearized RTD amplifier that is powered from a single 5 volt supply. However, the circuit will work up to 36 volts without modification. The RTD is excited by a 100 μA constant current that is regulated by amplifier A (OP295). The 0.202 volts reference voltage used to generate the constant current is divided down from the 2.500 volt reference. The AMP04 amplifies the bridge output to a 10 mV/°C output coefficient.

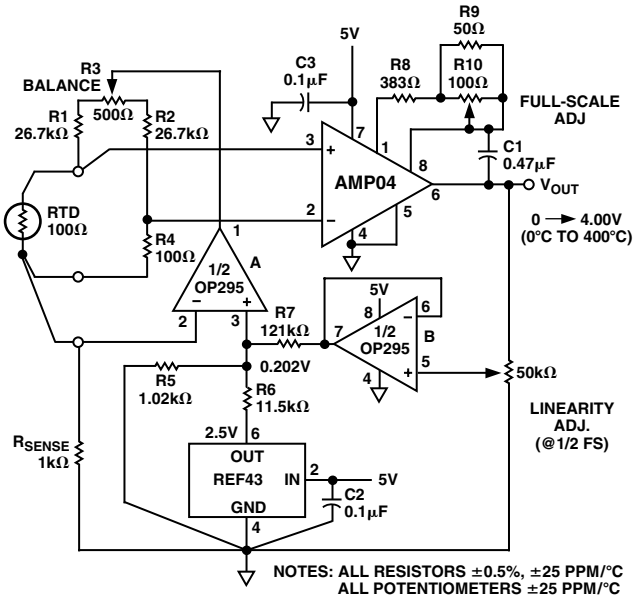


Figure 11. Precision Single Supply RTD Thermometer Amplifier

The RTD is linearized by feeding a portion of the signal back to the reference circuit, increasing the reference voltage as the temperature increases. When calibrated properly, the RTD's nonlinearity error will be canceled.

To calibrate, either immerse the RTD into a zero-degree ice bath or substitute an exact 100 Ω resistor in place of the RTD. Then adjust bridge BALANCE potentiometer R3 for a 0 volt output. Note that a 0 volt output is also the negative output swing limit of the AMP04 powered with a single supply. Therefore, be sure to adjust R3 to first cause the output to swing positive and then back off until the output just stops swinging negatively.

Next, set the LINEARITY ADJ potentiometer to the midrange. Substitute an exact 247.04 Ω resistor (equivalent to 400°C temperature) in place of the RTD. Adjust the FULL-SCALE potentiometer for a 4.000 volts output.

Finally substitute a 175.84 Ω resistor (equivalent to 200°C temperature), and adjust the LINEARITY ADJ potentiometer for a 2.000 volts at the output. Repeat the full-scale and the half-scale adjustments as needed.

When properly calibrated, the circuit achieves better than ±0.5°C accuracy within a temperature measurement range from 0°C to 400°C.

Precision 4-20 mA Loop Transmitter with Noninteractive Trim

Figure 12 shows a full bridge strain gage transducer amplifier circuit that is powered off the 4-20 mA current loop. The AMP04 amplifies the bridge signal differentially and is converted to a current by the output amplifier. The total quiescent current drawn by the circuit, which includes the bridge, the amplifiers, and the resistor biasing, is only a fraction of the 4 mA null current that flows through the current-sense resistor R_{SENSE}. The voltage across R_{SENSE} feeds back to the OP90's input, whose common-mode is fixed at the current summing reference voltage, thus regulating the output current.

With no bridge signal, the 4 mA null is simply set up by the 50 kΩ NULL potentiometer plus the 976 kΩ resistors that inject an offset that forces an 80 mV drop across R_{SENSE}. At a 50 mV full-scale bridge voltage, the AMP04 amplifies the voltage-to-current converter for a full-scale of 20 mA at the output. Since the OP90's input operates at a constant 0 volt common-mode voltage, the null and the span adjustments do not interact with one another. Calibration is simple and easy with the NULL adjusted first, followed by SPAN adjust. The entire circuit can be remotely placed, and powered from the 4-20 mA 2-wire loop.

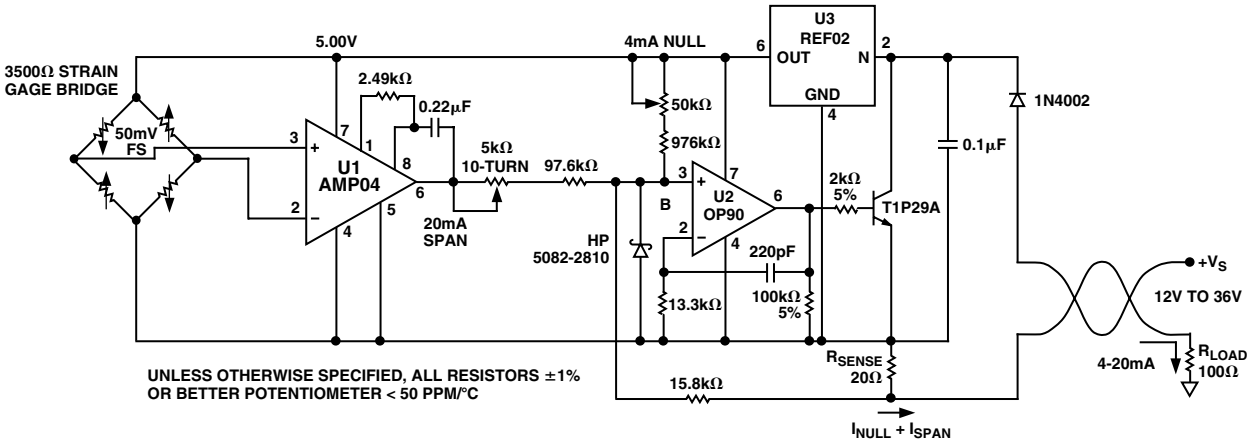


Figure 12. Precision 4-20 mA Loop Transmitter Features Noninteractive Trims

4-20 mA Loop Receiver

At the receiving end of a 4-20 mA loop, the AMP04 makes a convenient differential receiver to convert the current back to a usable voltage (Figure 13). The 4-20 mA signal current passes through a 100 Ω sense resistor. The voltage drop is differentially amplified by the AMP04. The 4 mA offset is removed by the offset correction circuit.

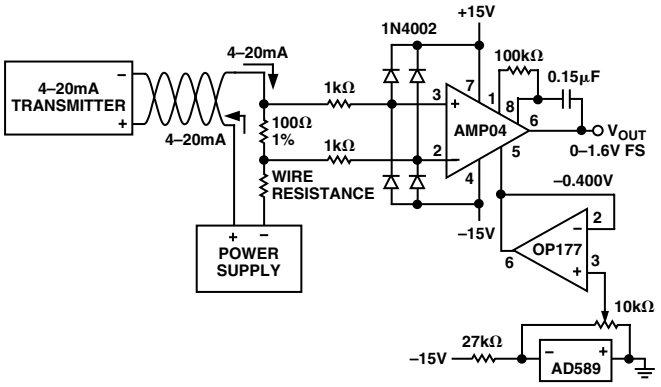


Figure 13. 4-to-20 mA Line Receiver

Low Power, Pulsed Load-Cell Amplifier

Figure 14 shows a 350 Ω load cell that is pulsed with a low duty cycle to conserve power. The OP295's rail-to-rail output capability allows a maximum voltage of 10 volts to be applied to the bridge. The bridge voltage is selectively pulsed on when a measurement is made. A negative-going pulse lasting 200 ms should be applied to the MEASURE input. The long pulsewidth is necessary to allow ample settling time for the long time constant of the low-pass filter around the AMP04. A much faster settling time can be achieved by omitting the filter capacitor.

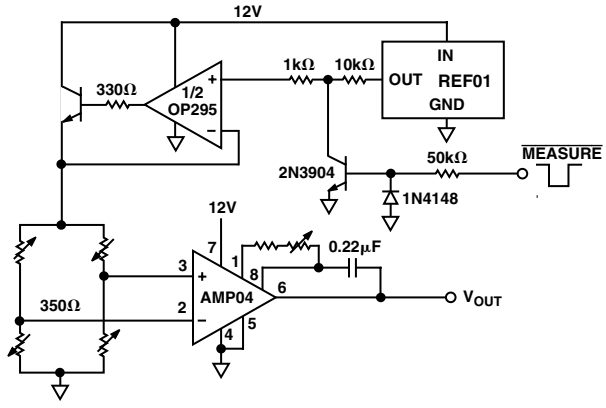


Figure 14. Pulsed Load Cell Bridge Amplifier

Single Supply Programmable Gain Instrumentation Amplifier

Combining with the single supply ADG221 quad analog switch, the AMP04 makes a useful programmable gain amplifier that can handle input and output signals at zero volts. Figure 15 shows the implementation. A logic low input to any of the gain control ports will cause the gain to change by shorting a gain-set resistor across AMP04's Pins 1 and 8. Trimming is required at higher gains to improve accuracy because the switch ON-resistance becomes a more significant part of the gain-set resistance. The gain of 500 setting has two switches connected in parallel to reduce the switch resistance.

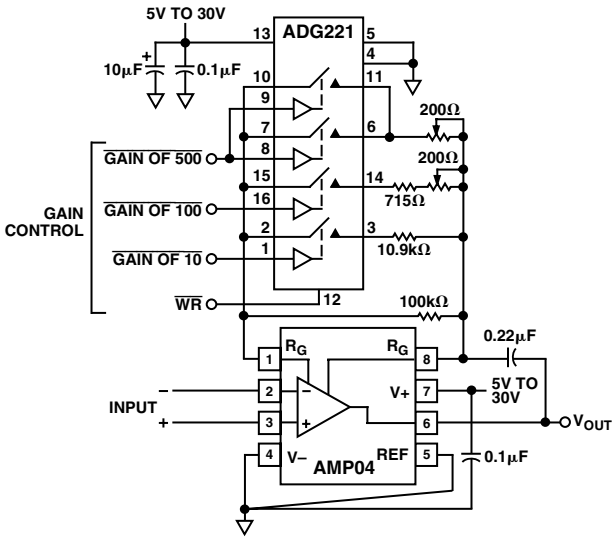


Figure 15. Single Supply Programmable Gain Instrumentation Amplifier

The switch ON resistance is lower if the supply voltage is 12 volts or higher. Additionally, the overall amplifier's temperature coefficient also improves with higher supply voltage.

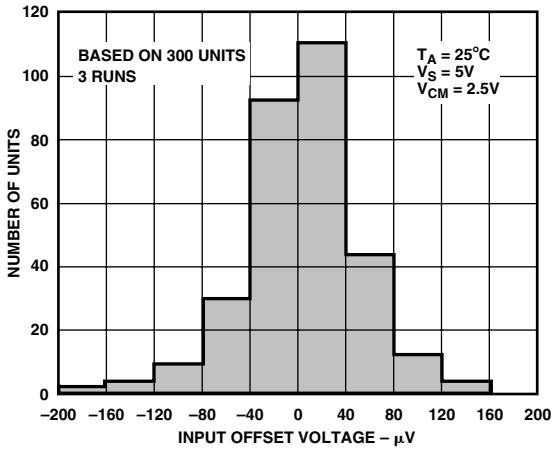


Figure 16. Input Offset (V_{IOS}) Distribution @ 5 V

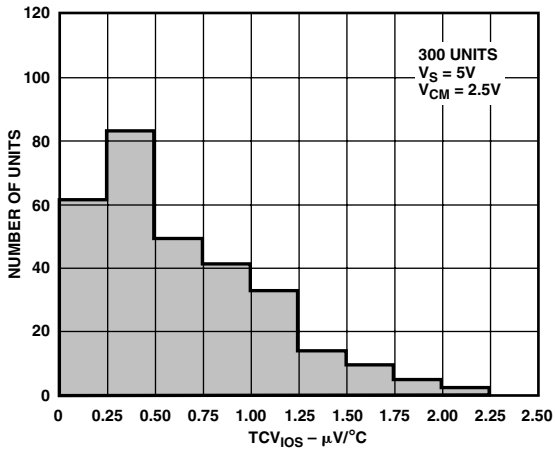


Figure 17. Input Offset Drift (TCV_{IOS}) Distribution @ 5 V

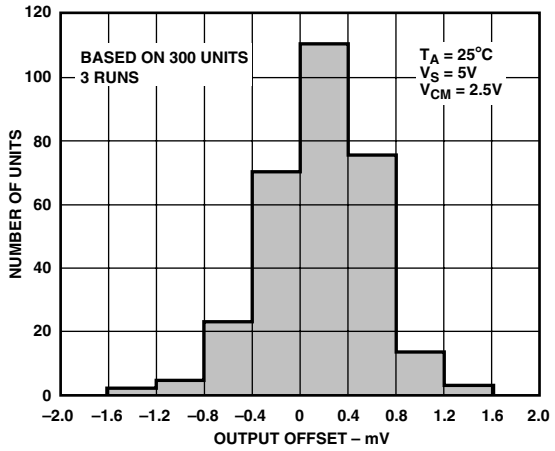


Figure 18. Output Offset (V_{OOS}) Distribution @ 5 V

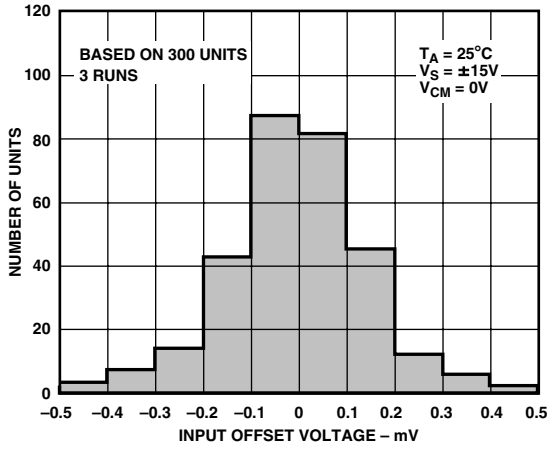


Figure 19. Input Offset (V_{IOS}) Distribution @ ±15 V

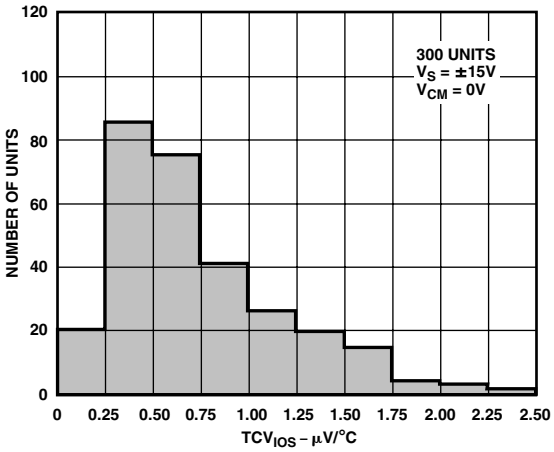


Figure 20. Input Offset Drift (TCV_{IOS}) Distribution @ ±15 V

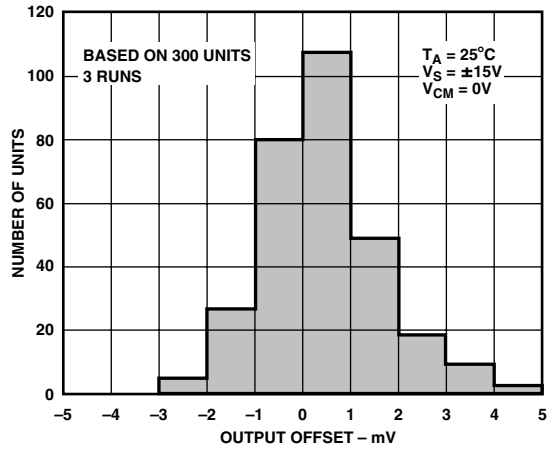


Figure 21. Output Offset (V_{OOS}) Distribution @ ±15 V

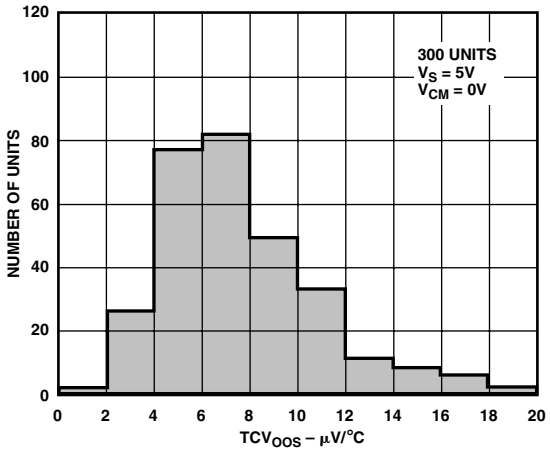


Figure 22. Output Offset Drift (TCV_{OOS}) Distribution @ 5 V

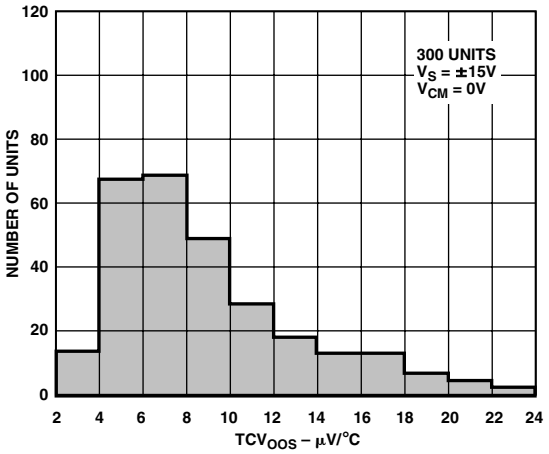


Figure 25. Output Offset Drift (TCV_{OOS}) Distribution @ ±15 V

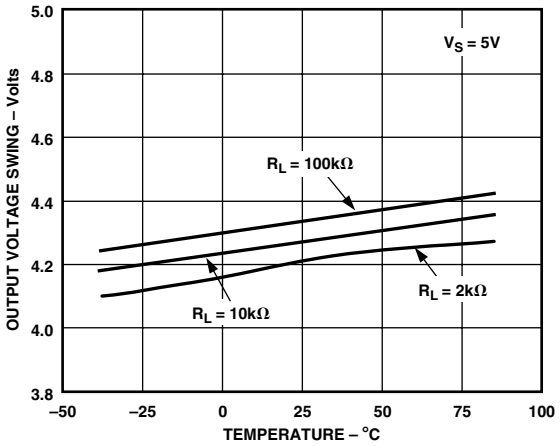


Figure 23. Output Voltage Swing vs. Temperature @ 5 V

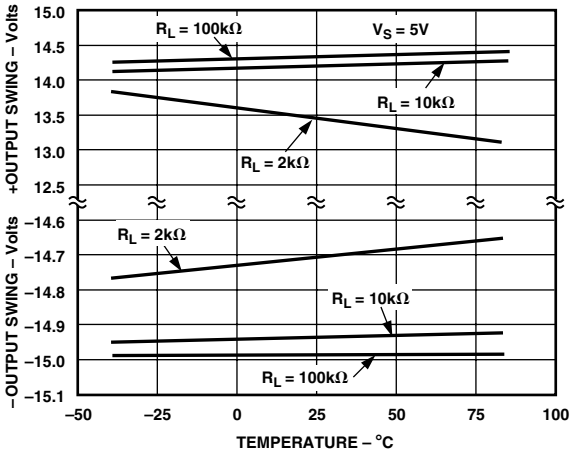


Figure 26. Output Voltage Swing vs. Temperature @ ±15 V

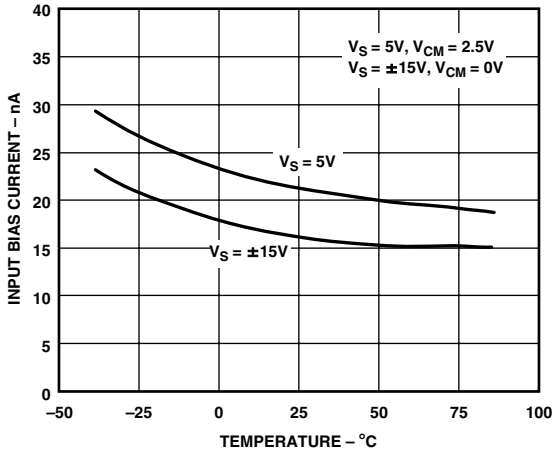


Figure 24. Input Bias Current vs. Temperature

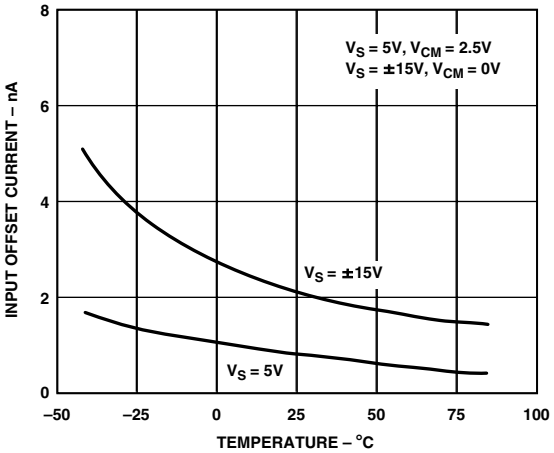


Figure 27. Input Offset Current vs. Temperature

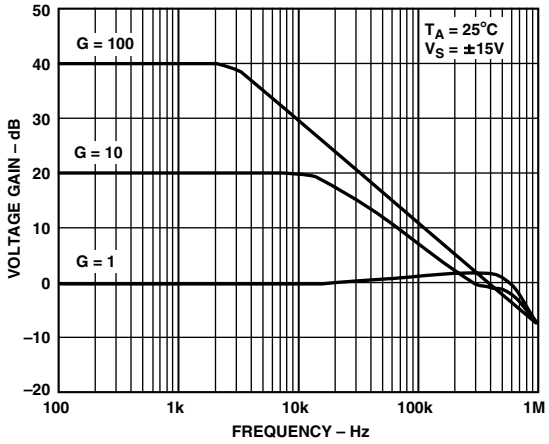


Figure 28. Closed-Loop Voltage Gain vs. Frequency

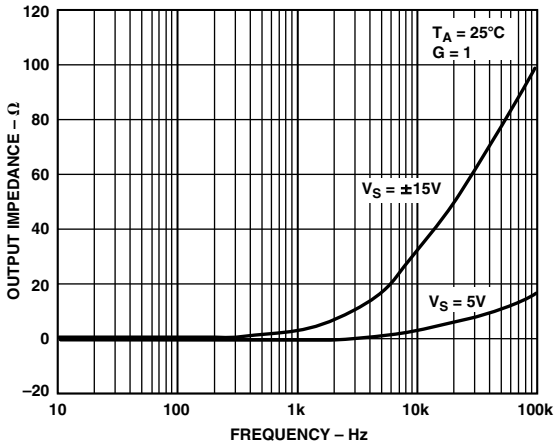


Figure 31. Closed-Loop Output Impedance vs. Frequency

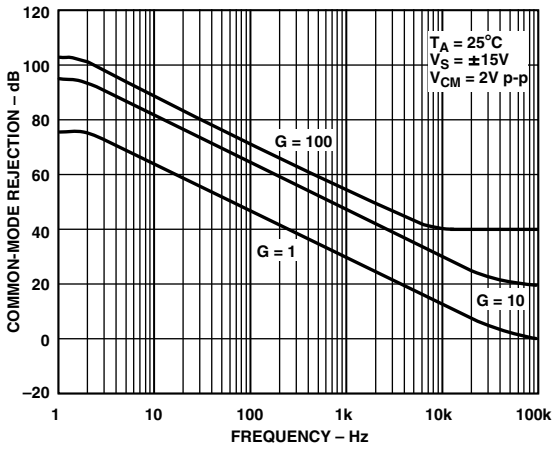


Figure 29. Common-Mode Rejection vs. Frequency

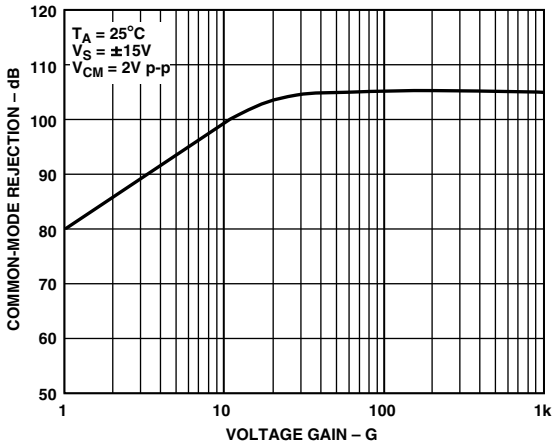


Figure 32. Common-Mode Rejection vs. Voltage Gain

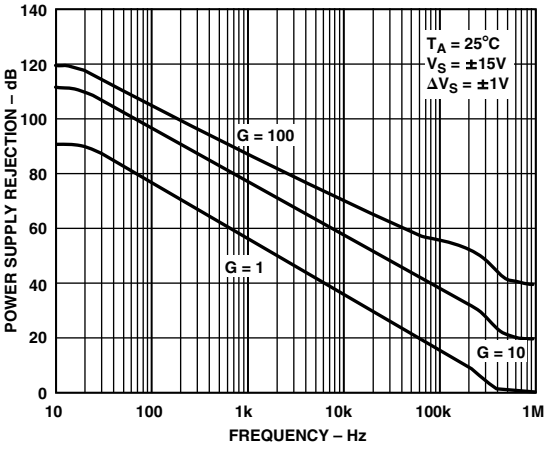


Figure 30. Positive Power Supply Rejection vs. Frequency

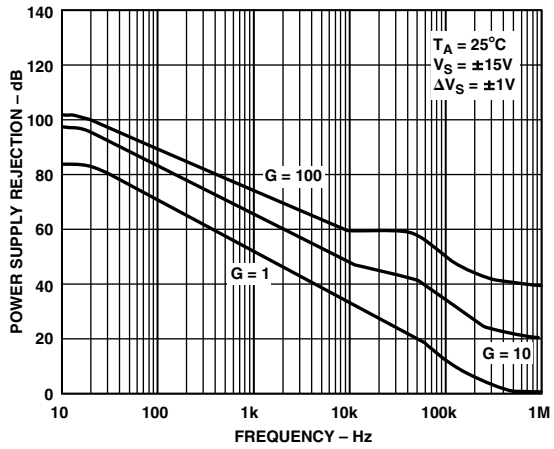


Figure 33. Negative Power Supply Rejection vs. Frequency

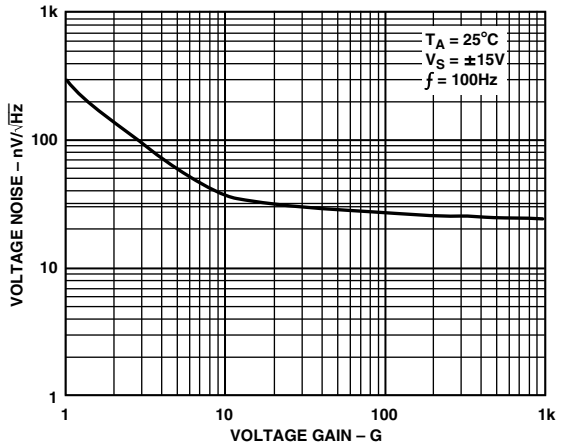


Figure 34. Voltage Noise Density vs. Gain

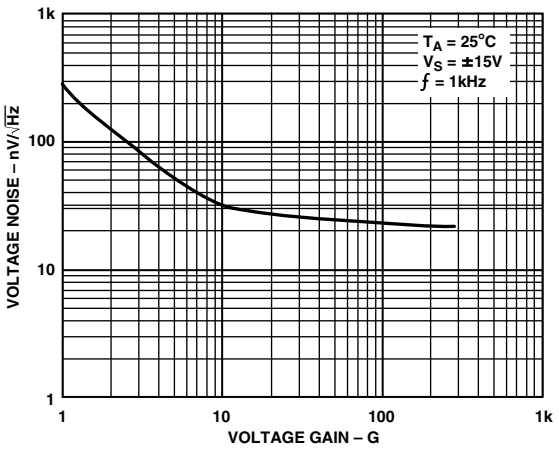


Figure 37. Voltage Noise Density vs. Gain, f = 1 kHz

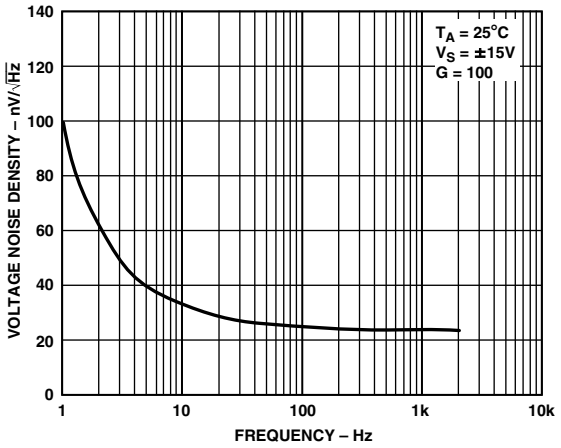


Figure 35. Voltage Noise Density vs. Frequency

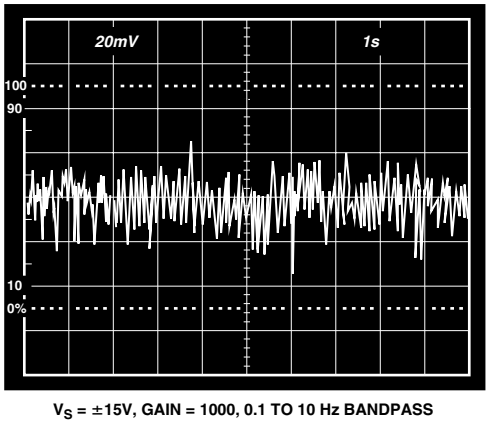


Figure 38. Input Noise Voltage

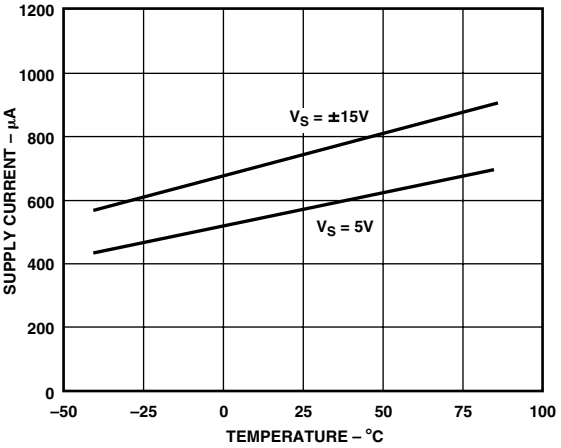


Figure 36. Supply Current vs. Temperature

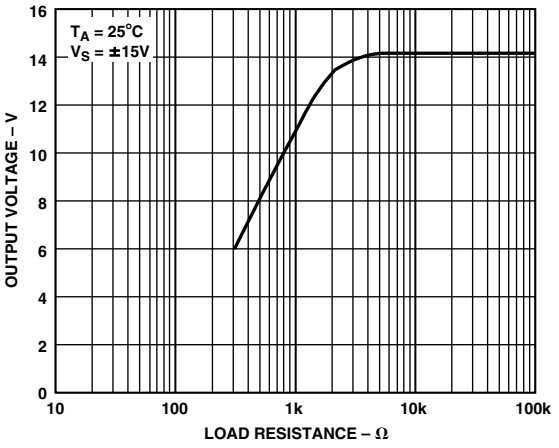
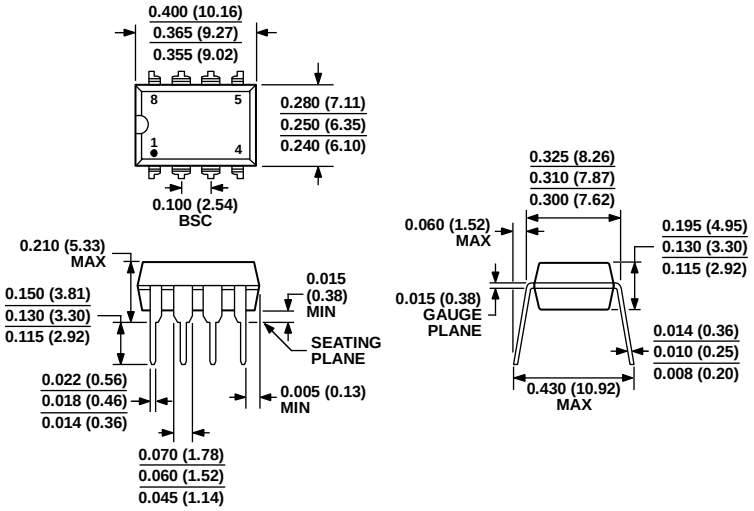


Figure 39. Maximum Output Voltage vs. Load Resistance

OUTLINE DIMENSIONS

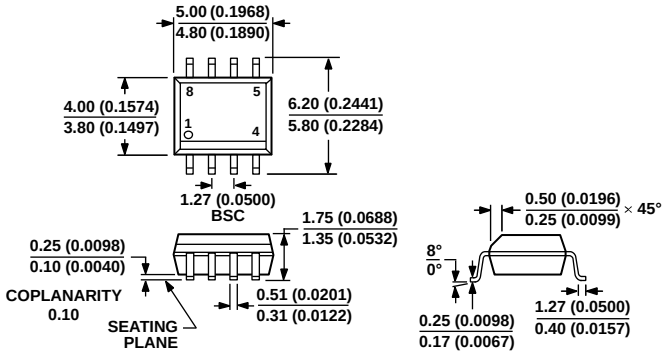


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 40. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 41. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow-Body
(R-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AMP04EPZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AMP04ESZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04ESZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04FPZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AMP04FS	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04FS-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04FSZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04FSZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04FSZ-RL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AMP04GBC	25°C	Die	

[1] Z = RoHS Compliant Part.

REVISION HISTORY

6/15—Rev. B to Rev. C