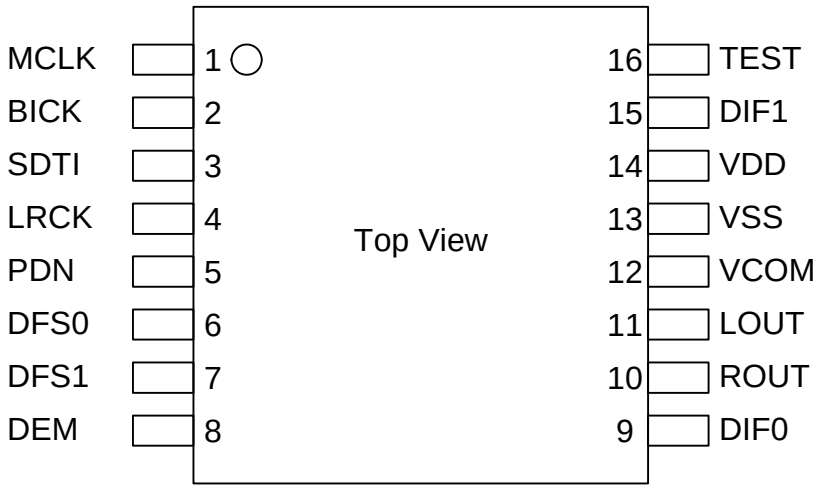
■ Ordering Guide

AK4386ET	–20 ~ +85°C	16pin TSSOP (0.65mm pitch)
AK4386VT	–40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4386	Evaluation Board for AK4386	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	Input Channel Clock Pin
5	PDN	I	Full Power Down Mode Pin "L" : Power down, "H" : Power up
6	DFS0	I	Sampling Speed Select 0 Pin
7	DFS1	I	Sampling Speed Select 1 Pin
8	DEM	I	De-emphasis Filter Enable Pin "L" : OFF, "H" : ON (De-emphasis of fs=44.1kHz is enable.)
9	DIF0	I	Audio Interface Format 0 Pin
10	ROUT	O	Rch Analog Output Pin
11	LOUT	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Output Pin, 0.55 × VDD Normally connected to VSS with a 4.7μF (min. 1μF, max. 10μF) electrolytic capacitor.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin, 2.2 ~ 3.6V
15	DIF1	I	Audio Interface Format 1 Pin
16	TEST	I	TEST Pin This pin should be connected to VDD.

Note: All digital input pins should not be left floating.

■ Handling of Unused Pin

The unused output pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT, ROUT	This pin should be open.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply		VDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	–0.3	VDD+0.3	V
Ambient Temperature (Powered applied)	AK4386ET	Ta	–20	85	°C
	AK4386VT	Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	2.2	3.0	3.6	V

Note 1. All voltages with respect to ground.

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=3.0V; VSS=0V; fs=44.1kHz, 96kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data;
Measurement frequency=20Hz ~ 20kHz at fs=44.1kHz, 20Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Dynamic Characteristics:						
Resolution					24	Bits
THD+N	fs=44.1kHz BW=20kHz	0dBFS		–86	–76	dB
		–60dBFS		–37	-	dB
	fs=96kHz BW=40kHz	0dBFS		–84	-	dB
		–60dBFS		–34	-	dB
DR	(–60dBFS with A-weighted)		92	100		dB
S/N	(A-weighted)		92	100		dB
Interchannel Isolation			80	100		dB
DC Accuracy:						
Interchannel Gain Mismatch				0.2	0.5	dB
Gain Drift				100	-	ppm/°C
Output Voltage		(Note 2)	1.85	2.0	2.15	Vpp
Load Resistance		(Note 3)	10			kΩ
Load Capacitance					25	pF
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = “H”, fs=44.1kHz)				6	9	mA
Normal Operation (PDN pin = “H”, fs=96kHz)				6.5	10	mA
Power Save mode (PDN pin = “H”, MCLK Stop)				1.5	2.5	mA
Full Power-down mode (PDN pin = “L”)		(Note 4)		10	50	μA

Note 2. Full-scale voltage (0dB). Output voltage scales with the voltage of VDD, Vout = 0.67 × VDD (typ).
Note 3. For AC-load.
Note 4. All digital input pins are fixed to VDD or VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VDD=2.2 ~ 3.6V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
DAC Digital Filter:						
Passband (Note 5)	±0.05dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 5)		SB	24.1			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation		SA	64			dB
Group Delay (Note 6)		GD	-	24.0	-	1/fs
Digital Filter + SCF + CTF:						
Frequency Response	0 ~ 20kHz	FR	-	±0.5	-	dB
	~ 40kHz (Note 7)		-	±1.0	-	dB

Note 5. The passband and stopband frequencies scale with fs (system sampling rate).
Note 6. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.
Note 7. At fs=96kHz.

DC CHARACTERISTICS

(Ta=25°C; VDD=2.2 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VDD	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD=2.2 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency					
Half Speed Mode (512/768/1024/1536fs)	fCLK	4.096		36.864	MHz
Normal Speed Mode (256/384/512/768fs)	fCLK	2.048		36.864	MHz
Double Speed Mode (128/192/256/384fs)	fCLK	6.144		36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Half Speed Mode (DFS1-0 = "10")	fsh	8		24	kHz
Normal Speed Mode (DFS1-0 = "00")	fsn	8		48	kHz
Double Speed Mode (DFS1-0 = "01")	fsd	48		96	kHz
Duty Cycle	dCLK	45		55	%
Audio Interface Timing					
BICK Period					
Half Speed Mode	tBCK	1/128fs			ns
Normal Speed Mode	tBCK	1/128fs			ns
Double Speed Mode	tBCK	1/64fs			ns
BICK Pulse Width Low	tBCKL	70			ns
Pulse Width High	tBCKH	70			ns
BICK "↑" to LRCK Edge (Note 8)	tBLR	40			ns
LRCK Edge to BICK "↑" (Note 8)	tLRB	40			ns
SDTI Hold Time	tSDH	40			ns
SDTI Setup Time	tSDS	40			ns
Power-Down & Reset Timing					
PDN Pulse Width (Note 9)	tPD	4 × C			ms

Note 8. BICK rising edge must not occur at the same time as LRCK edge.

Note 9. The AK4386 can be reset by bringing PDN pin = "L".

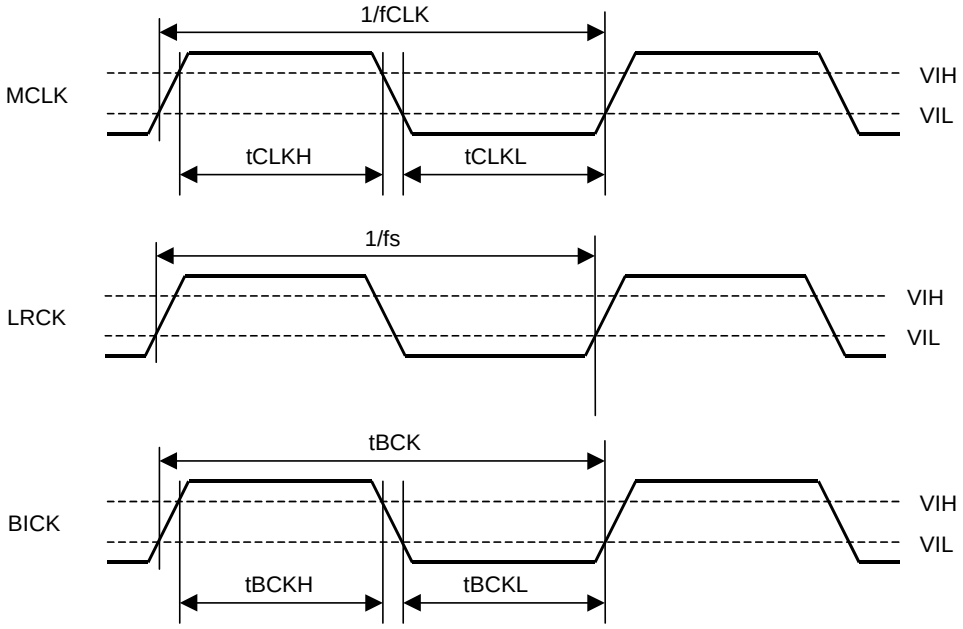
The PDN pulse width is proportional to the value of the capacitor (C) connected to VCOM pin. tPD = 4 × C.

When C = 4.7μF, tPD is 19ms(min).

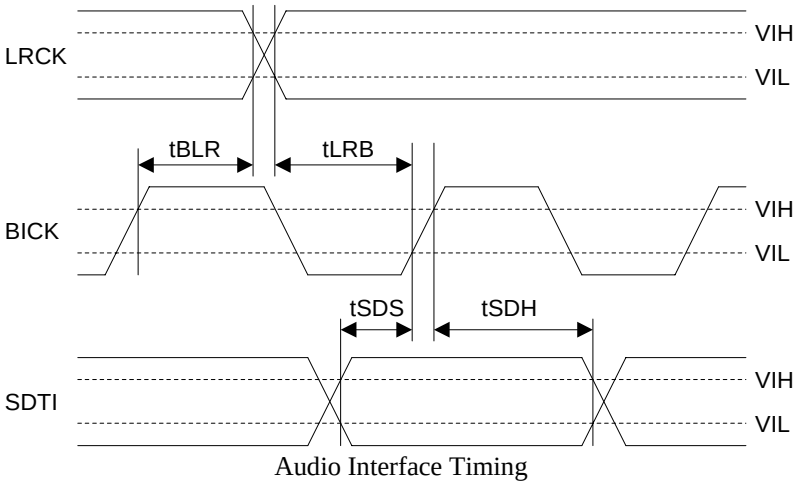
The value of the capacitor (C) connected with VCOM pin should be 1μF ≤ C ≤ 10μF.

When the states of DIF1-0 pins change, the AK4386 should be reset by PDN pin.

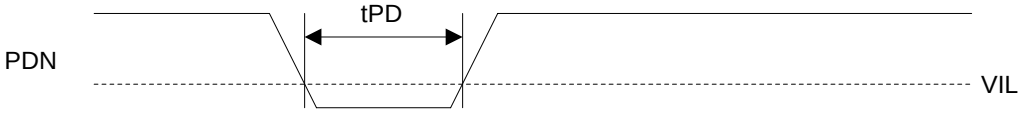
■ Timing Diagram



Clock Timing



Audio Interface Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4386, are MCLK, BICK and LRCK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The MCLK frequency is detected from the relation between MCLK and LRCK automatically. The Half speed, the Normal speed and the Double speed mode are selected with the DFS1-0 pins (Table 1). The sampling speed mode is set depending on the MCLK frequency automatically for Auto mode (DFS1 pin = DFS0 pin = "H") (Table 2).

The AK4386 is automatically placed in the power save mode when MCLK stops in the normal operation mode (PDN pin = "H"), and the analog output becomes the VCOM voltage. After MCLK is input again, the AK4386 is powered up. After exiting reset at power-up etc., the AK4386 is in the power-down mode until MCLK and LRCK are input.

When the states of DIF1-0 pins change in the normal operation mode, the AK4386 should be reset by PDN pin.

Mode	DFS1	DFS0	fs	MCLK Frequency
Normal Speed	L	L	8 ~ 48kHz	256/384/512/768fs
Double Speed	L	H	48 ~ 96kHz	128/192/256/384fs
Half Speed	H	L	8 ~ 24kHz	512/768/1024/1536fs
Auto	H	H	8 ~ 96kHz	Table 2

Table 1. System Clock Example

MCLK Frequency	Sampling Speed Mode	fs
512/768fs	Normal Speed	8 ~ 48kHz
128/192/256/384fs	Double Speed	48 ~ 96kHz
1024/1536fs	Half Speed	8 ~ 24kHz

Table 2. Auto Mode

■ Audio Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF1-0 pins as shown in Table 3 can select four serial data modes. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 3 can be used for 16bit I^2S Compatible format by zeroing the unused LSBs at BICK ≥ 48fs or BICK = 32fs.

Mode	DIF1	DIF0	SDTI Format	BICK	Figure
0	L	L	16bit, LSB justified	≥ 32fs	Figure 1
1	L	H	24bit, LSB justified	≥ 48fs	Figure 2
2	H	L	24bit, MSB justified	≥ 48fs	Figure 3
3	H	H	16/24bit, I^2S Compatible	≥ 48fs or 32fs	Figure 4

Table 3. Audio Interface Format

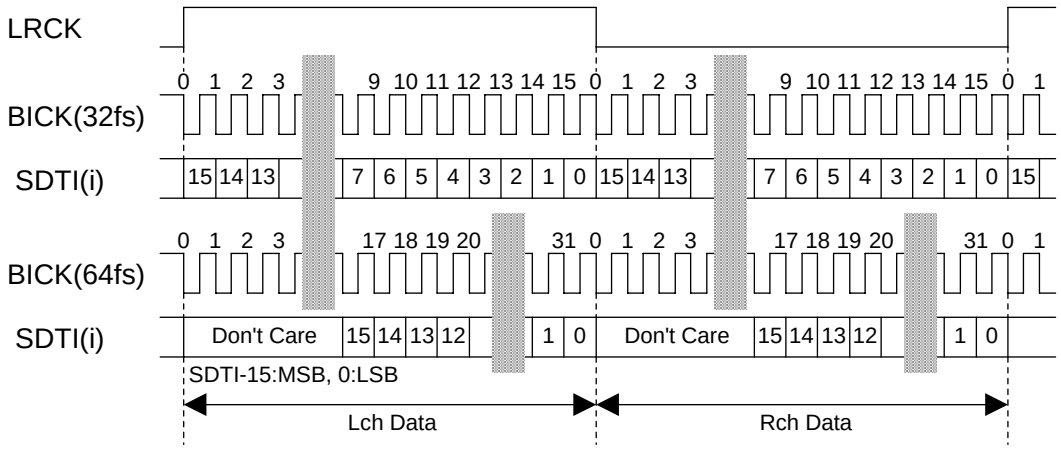


Figure 1. Mode 0 Timing

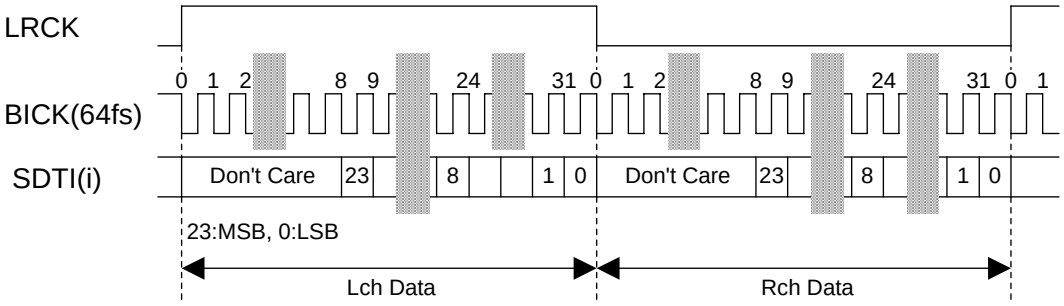


Figure 2. Mode 1 Timing

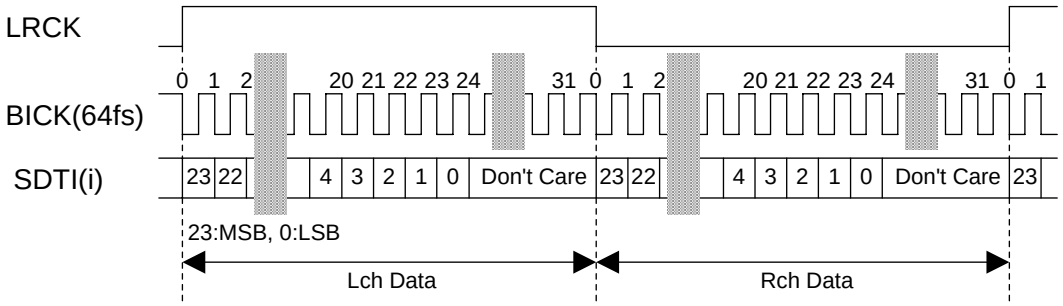


Figure 3. Mode 2 Timing

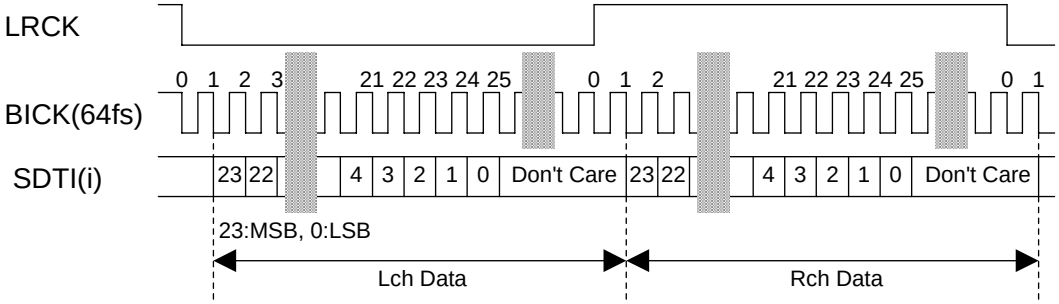


Figure 4. Mode 3 Timing

■ De-emphasis Filter

The AK4386 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to 44.1kHz sampling. The de-emphasis filter is enabled by setting DEM pin "H". In case of Half speed and Double speed mode, the digital de-emphasis filter is always off.

Mode	DFS1 pin	DFS0 pin	DEM pin	De-emphasis Filter
Normal Speed	L	L	L	OFF
	L	L	H	ON
Double Speed	L	H	*	OFF
Half Speed	H	L	*	OFF
Auto	H	H	L	OFF
	H	H	H	ON (Note)

Table 4. De-emephasis Filter (*: Don't care)

Note. The digital de-emphasis filter corresponds to 44.1kHz sampling.
In case of Half speed and Double speed mode, the digital de-emphasis filter is always off.

■ Power-down

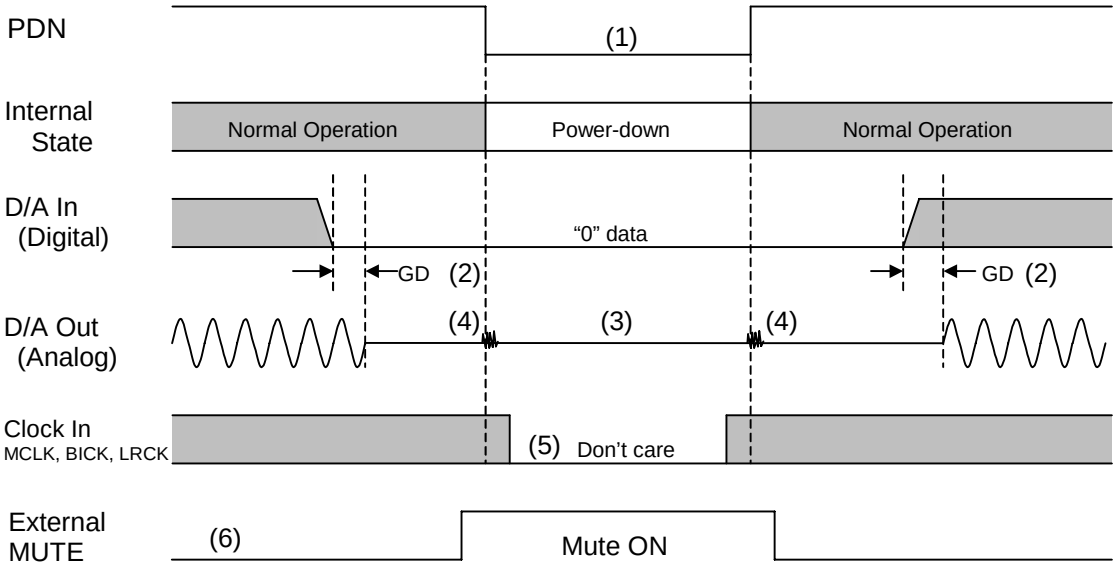
The AK4386 is placed in the power-down mode by bringing PDN pin = "L". and the digital filter is reset at the same time. This reset should always be done after power up.

When PDN pin = "L", DAC outputs go to Hi-Z. Also, the internal power down is automatically done when MCLK stops during operating (PDN pin ="H"), and the analog outputs go to the VCOM voltage. MCLK pin should be fixed to "H" or "L" when MCLK stops.

Mode	PDN pin	MCLK	DAC Output	State
0	L	Don't care	Hi-Z	Full Power Down
1	H	Supplied	Normal Output	Normal
2		Not Supplied	VCOM Voltage	Power Save

Table 5. Power down mode

(1) Power down by PDN pin

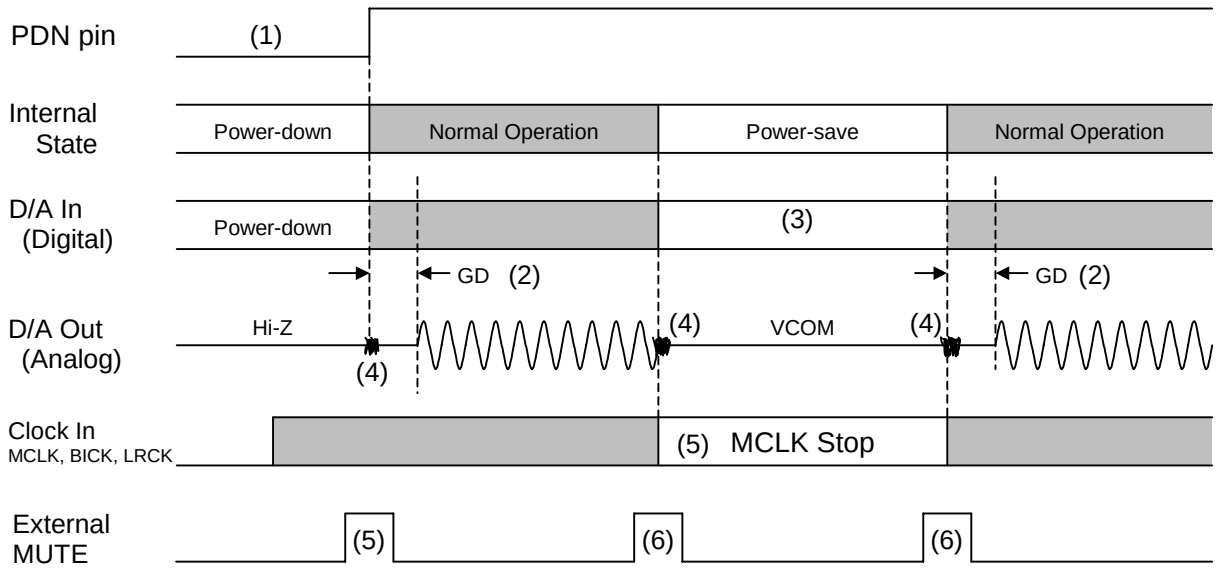


Notes:

(1) PDN pin should be "L" for 19ms or more when an electrolytic capacitor 4.7μF is attached between VCOM pin and VSS.)
(2) The analog output corresponding to digital input has the group delay (GD).
(3) When PDN pin = "L", the analog output is Hi-Z.
(4) Click noise occurs in 3 ~ 4LRCK at both edges (↑ ↓) of PDN signal. This noise is output even if "0" data is input.
(5) The external clocks (MCLK, BICK and LRCK) can be stopped in the power down mode (PDN pin = "L").
(6) Please mute the analog output externally if the click noise (4) influences system application. The timing example is shown in this figure.

Figure 5. Power-down/up sequence example 1

(2) Power save by MCLK stop (PDN pin = "H")



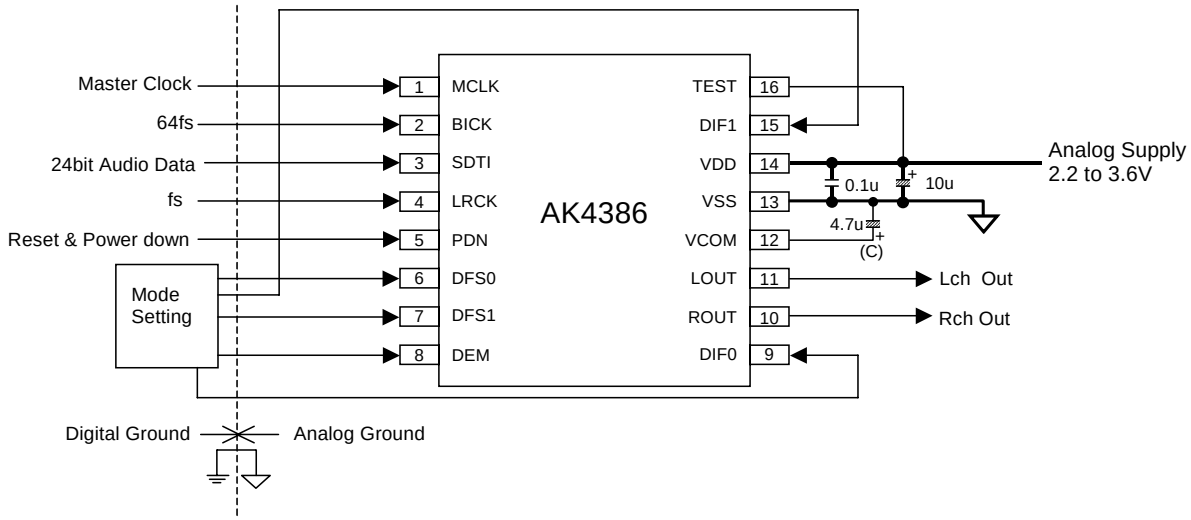
Notes:

(1) PDN pin should be "L" for 19ms or more when an electrolytic capacitor 4.7μF is attached between VCOM pin and VSS.)
(2) The analog output corresponding to digital input has the group delay (GD).
(3) The digital data can be stopped. The click noise after MCLK is input again by inputting the "0" data to this section can be reduced.
(4) Click noise occurs in 3 ~ 4LRCK at both edges (↑ ↓) of PDN signal, MCLK inputs and MCLK stops. This noise is output even if "0" data is input.
(5) The external clocks (BICK and LRCK) can be stopped in the power down mode (MCLK stop).
(6) Please mute the analog output externally if the click noise (4) influences system application. The timing example is shown in this figure.

Figure 6. Power-down/up sequence example 2

SYSTEM DESIGN

Figure 7 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:

- VSS of the AK4386 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- When AOUT drive some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- The value of the capacitor connected to VCOM pin should be 1μF ≤ C ≤ 10μF.
- All digital input pins should not be left floating.

Figure 7. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4386 requires careful attention to power supply and grounding arrangements. VDD is usually supplied from the analog supply in the system. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4386 as possible, with the small value ceramic capacitor being the closest.

2. Voltage Reference

The differential Voltage between VDD and VSS sets the analog output range. VCOM is used as a common voltage of the analog signal. VCOM pin is a signal ground of this chip. An electrolytic capacitor about 4.7μF should be attached between VCOM pin and VSS. No load current may be drawn from VCOM pin. Especially, the ceramic capacitor should be connected to this pin as near as possible.

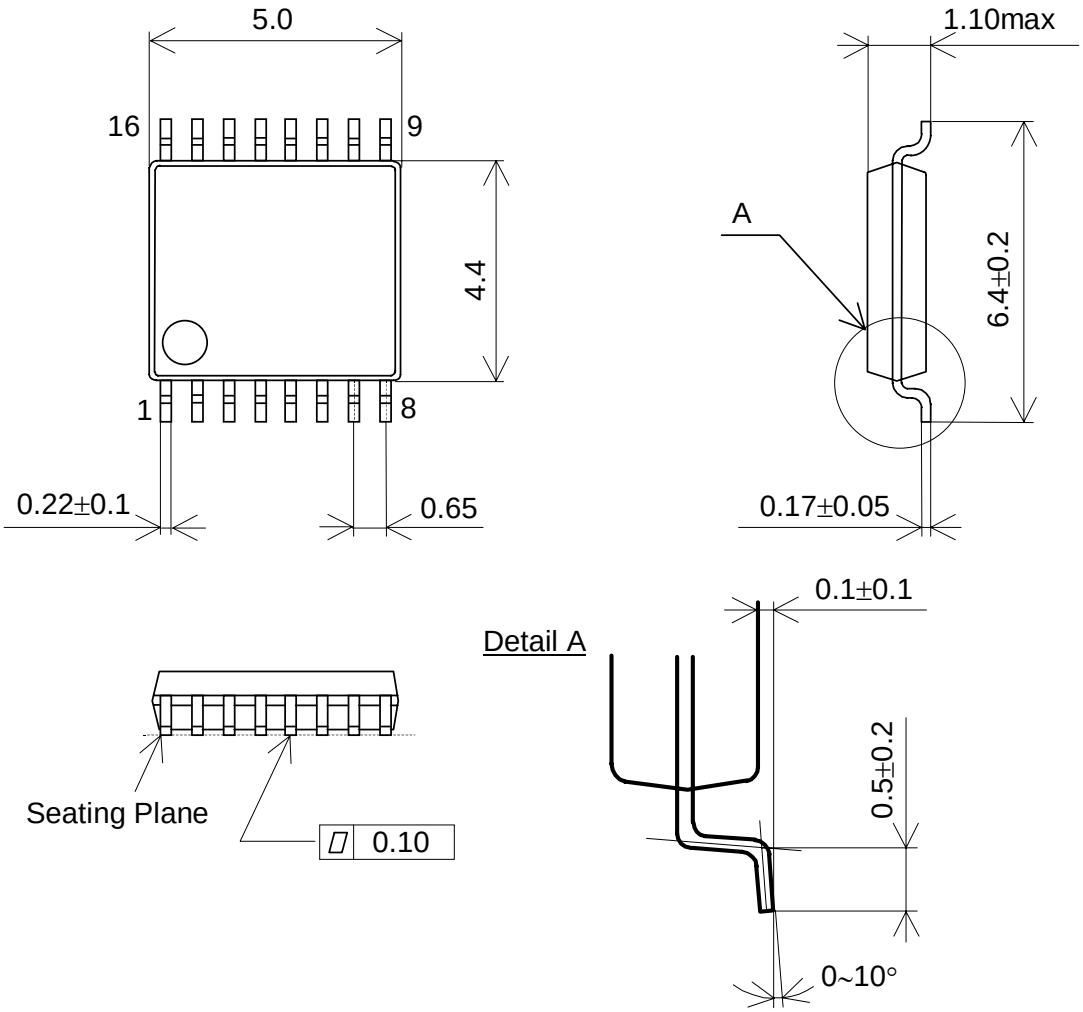
3. Analog Outputs

The analog outputs are single-ended and centered around the VCOM voltage (0.55 × VDD). The output signal range is typically 2.0Vpp (typ@VDD=3.0V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage (0.55 × VDD) for 000000H (@24bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

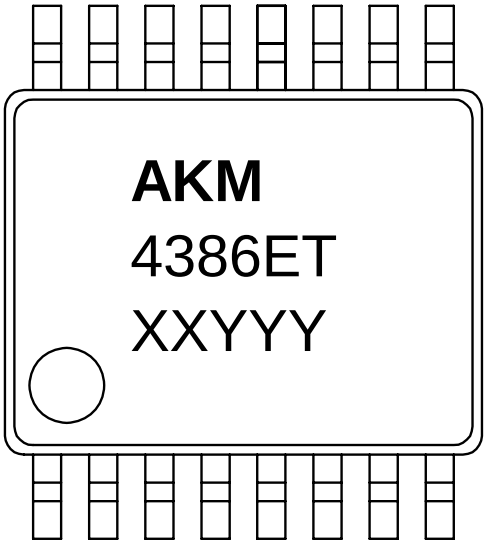
16pin TSSOP (Unit: mm)



■ Material & Lead finish

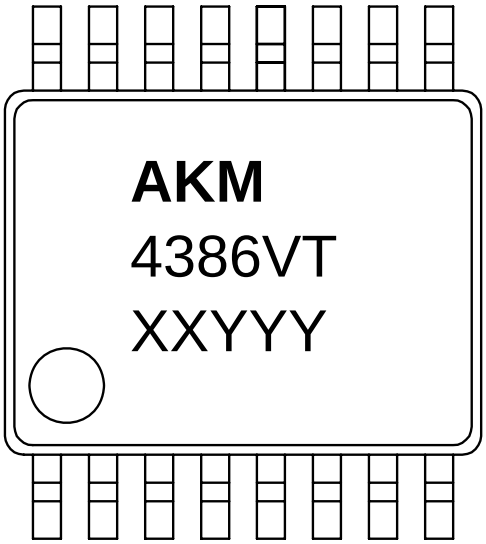
Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING (AK4386ET)



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code : 4386ET

MARKING (AK4386VT)



4) Pin #1 indication
5) Date Code : XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
6) Marketing Code : 4386VT

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
03/12/01	00	First edition		
08/10/23	01	Spec Addition		The AK4386ET was added. VT and ET datasheets were combined together.