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REVISION HISTORY

11/14—Rev. 0 to Rev. A

Changed Minimum Supply Voltage from 3.0 V to 3.135 V (Throughout) ... 1
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4/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A Grade			B Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	65	100	18	32	36	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			15	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing Direction	t_{PSKOD}			50			6	ns	

Table 2.

Parameter	Symbol	1 Mbps—A, B Grades			10 Mbps—B Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									No load
ADuM3300W	I_{DD1}		2.4	3.3		7.0	8.1	mA	
	I_{DD2}		1.1	2.1		2.7	3.6	mA	
ADuM3301W	I_{DD1}		2.0	3.1		5.5	6.9	mA	
	I_{DD2}		1.6	2.6		3.9	5.4	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	2.0			V	
Logic Low	V_{IL}			0.8	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Leakage per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
VE_x Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{Ex} = 0 V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	μA	
Supply Current per Channel						
Quiescent Supply Current						All data inputs at logic low
Input	$I_{DDI(Q)}$		0.66	0.97	mA	
Output	$I_{DDO(Q)}$		0.39	0.55	mA	
Dynamic Supply Current						
Input	$I_{DDI(D)}$		0.20		mA/Mbps	
Output	$I_{DDO(D)}$		0.05		mA/Mbps	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	$V_{Ix} = V_{DDx}$
Propagation Delay						
Output Disable	t_{PHZ}, t_{PLZ}		6	8	ns	High/low output to high impedance
Output Enable	t_{PZH}, t_{PZL}		6	8	ns	High impedance to high/low output
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. V_{CM} = 1000 V, transient magnitude = 800 V.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.135 V ≤ V_{DD1} ≤ 3.6 V, 3.135 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	75	100	20	38	45	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing Direction	t_{PSKOD}			50			6	ns	

Table 5.

		1 Mbps—A, WB Grades			10 Mbps—B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									No load
ADuM3300W	I_{DD1}		1.4	2.1		3.8	5.3	mA	
	I_{DD2}		0.7	1.4		1.5	2.1	mA	
ADuM3301W	I_{DD1}		1.1	1.9		3.0	4.1	mA	
	I_{DD2}		0.9	1.7		2.2	3.0	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	1.6			V	
Logic Low	V_{IL}			0.4	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, $V_{Ix} = V_{IxH}$
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, $V_{Ix} = V_{IxH}$
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	I_{Ox} = 400 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Leakage per Channel	I_I	−10	+0.01	+10	µA	$0\ V \le V_{Ix} \le V_{DDx}$
VE_x Input Pull-Up Current	I_{PU}	−10	−3		µA	$V_{Ex} = 0\ V$
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Supply Current per Channel						
Quiescent Supply Current						All data inputs at logic low
Input	$I_{DDI(Q)}$		0.37	0.57	mA	
Output	$I_{DDO(Q)}$		0.25	0.37	mA	
Dynamic Supply Current						
Input	$I_{DDI(D)}$		0.1		mA/Mbps	
Output	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	$V_{Ix} = V_{DDx}$
Propagation Delay						
Output Disable	t_{PHZ}, t_{PLZ}		6	8	ns	High/low output to high impedance
Output Enable	t_{PZH}, t_{PZL}		6	8	ns	High impedance to high/low output
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. V_{CM} = 1000 V, transient magnitude = 800 V.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.135 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	70	100	20	30	42	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing Direction	t_{PSKOD}			50			6	ns	

Table 8.

		1 Mbps—A, B Grades			10 Mbps—B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									No load
ADuM3300W	I_{DD1}		2.4	3.3		2.0	8.1	mA	
	I_{DD2}		0.7	1.4		0.9	2.1	mA	
ADuM3301W	I_{DD1}		7.0	3.1		5.5	6.9	mA	
	I_{DD2}		1.5	1.7		2.2	3.0	mA	

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}					
5 V		2.0			V	
3.3 V		1.6			V	
Logic Low	V_{IL}					
5 V				0.8	V	
3.3 V				0.4	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Leakage per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
VE_x Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{Ex} = 0 V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	μA	
Supply Current per Channel						
Quiescent Supply Current						All data inputs at logic low
Input	$I_{DDI(Q)}$		0.66	0.97	mA	
Output	$I_{DDO(Q)}$		0.25	0.37	mA	
Dynamic Supply Current						
Input	$I_{DDI(D)}$		0.20		mA/Mbps	
Output	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDx}
Propagation Delay						
Output Disable	t_{PHZ}, t_{PLZ}		6	8	ns	High/low output to high impedance
Output Enable	t_{PZH}, t_{PZL}		6	8	ns	High impedance to high/low output
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. V_{CM} = 1000 V, transient magnitude = 800 V.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.135 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	70	100	20	30	42	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing Direction	t_{PSKOD}			50			6	ns	

Table 11.

Parameter	Symbol	1 Mbps—A, B Grades			10 Mbps—B Grade			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									No load
ADuM3300W	I_{DD1}		1.4	2.1		3.8	5.3	mA	
	I_{DD2}		1.1	2.1		2.7	3.6	mA	
ADuM3301W	I_{DD1}		1.1	1.9		3.0	4.1	mA	
	I_{DD2}		1.6	2.6		3.9	5.4	mA	

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}					
5 V		2.0			V	
3.3 V		1.6			V	
Logic Low	V_{IL}					
5 V				0.8	V	
3.3 V				0.4	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox} = -20$ µA, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low	V_{OL}		0.0	0.1	V	$I_{Ox} = 20$ µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400$ µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
Input Leakage per Channel	I_I	−10	+0.01	+10	µA	$0 V \le V_{Ix} \le V_{DDx}$
VE_x Input Pull-Up Current	I_{PU}	−10	−3		µA	$V_{Ex} = 0$ V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Supply Current per Channel						
Quiescent Supply Current						
Input	$I_{DDI(Q)}$		0.37	0.57	mA	All data inputs at logic low
Output	$I_{DDO(Q)}$		0.39	0.55	mA	All data inputs at logic low
Dynamic Supply Current						
Input	$I_{DDI(D)}$		0.10		mA/Mbps	
Output	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	$V_{Ix} = V_{DDx}$
Propagation Delay						
Output Disable	t_{PHZ}, t_{PLZ}		6	8	ns	High/low output to high impedance
Output Enable	t_{PZH}, t_{PZL}		6	8	ns	High impedance to high/low output
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. V_{CM} = 1000 V, transient magnitude = 800 V.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE						
Input to Output[1]	R_{I-O}		10^{12}		Ω	
CAPACITANCE						
Input to Output[1]	C_{I-O}		2.0		pF	f = 1 MHz
Input[2]	C_I		4.0		pF	
THERMAL RESISTANCE						
IC Junction-to- Ambient	θ_{JA}		45		°C/W	

[1] The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM3300W/ADuM3301W are approved by the organizations listed in Table 14. See Table 19 and the Insulation Lifetime section for more information regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 14.

UL	CSA	VDE
Recognized under UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single insulation, 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3300W/ADuM3301W is proof tested by applying an insulation test voltage of ≥3000 V rms for 1 sec (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3300W/ADuM3301W is proof tested by applying an insulation test voltage of ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance through air in the plane of the printed circuit board (PCB)
Minimum External Tracking (Creepage)	L(I02)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 16.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m =$ 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	840	V peak
After Environmental Tests Subgroup 1				
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Highest Allowable Overvoltage		V_{IOTM}	4000	V peak
Surge Isolation Voltage	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation @ 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

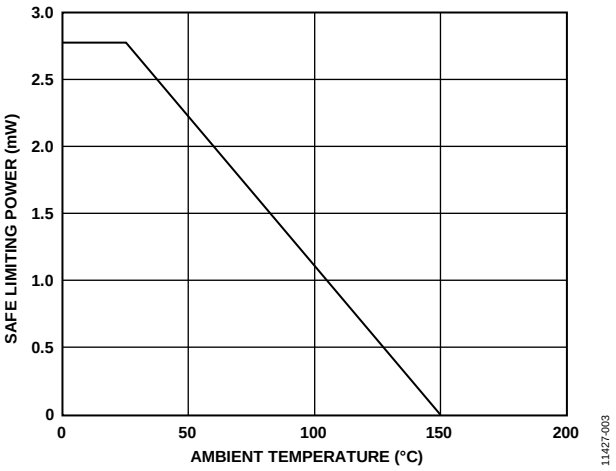


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.135	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective grounds. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 18.

Parameter	Rating[1]
Temperature Range	
Storage (T_{ST})	−65°C to +150°C
Operating (Ambient, T_A)	−40°C to +125°C
Supply Voltages[1] (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltage[1, 2] (V_{IA}, V_{IB}, V_{IC}, V_{E1}, V_{E2})	−0.5 V to V_{DDI} + 0.5 V
Output Voltage[1, 2] (V_{OA}, V_{OB}, V_{OC})	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4] (CM_H, CM_L)	−100 kV/µs to +100 kV/µs

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[2] All voltages are relative to their respective grounds.
[3] See Figure 3 for maximum rated power values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 19. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	560	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	1131	V peak	50-year minimum lifetime
DC Voltage			
Basic Insulation	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

Table 20. Truth Table Abbreviations

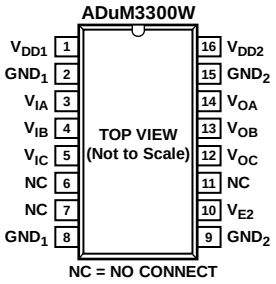
Letter	Description
H	High level
L	Low level
NC	No connect
X	Irrelevant (don't care)
Z	High impedance

Table 21. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{Ex} Input[2]	V_{DDI} State[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration when the V_{Ex} state is H or NC.
					Outputs return to a high impedance state within 8 ns of V_{DDO} power restoration when the V_{Ex} state is L.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, or C). V_{EX} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[2] In noisy environments, connecting V_{Ex} to an external logic high or low is recommended.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED TO EACH OTHER, AND IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.
2. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED TO EACH OTHER, AND IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.

11427-004

Figure 4. ADuM3300W Pin Configuration

Table 22. ADuM3300W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6, 7, 11	NC	No Connection. Do not connect to these pins.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	V_{E2}	Output Enable 2. Active high logic input. The V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. The V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.

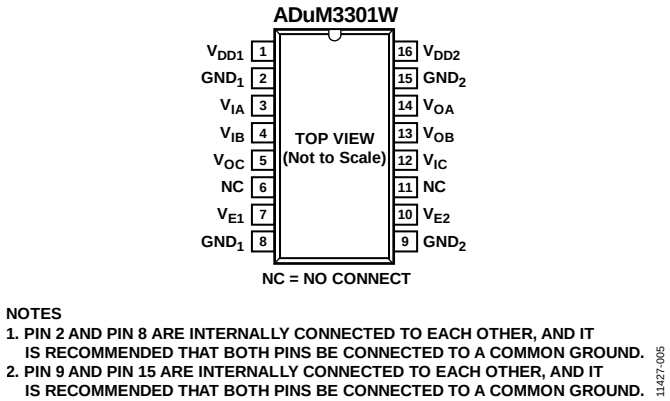


Figure 5. ADuM3301W Pin Configuration

Table 23. ADuM3301W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6, 11	NC	No Connection. Do not connect to these pins.
7	V_{E1}	Output Enable 1. Active high logic input. The V_{OC} output is enabled when V_{E1} is high or disconnected. The V_{OC} output is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	V_{E2}	Output Enable 2. Active high logic input. The V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. The V_{OA} and V_{OB} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

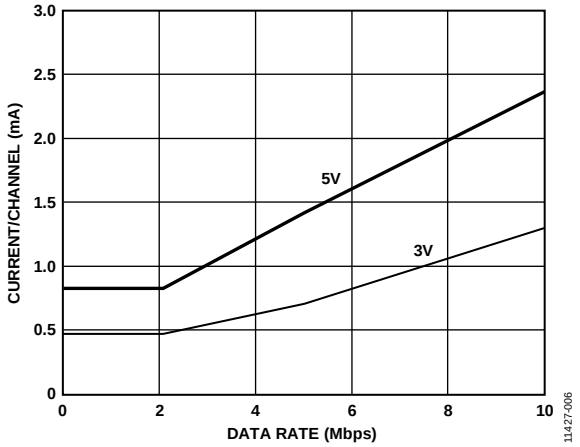


Figure 6. Typical Input Supply Current per Channel vs. Data Rate (No Load) for 5 V and 3.3 V Operation

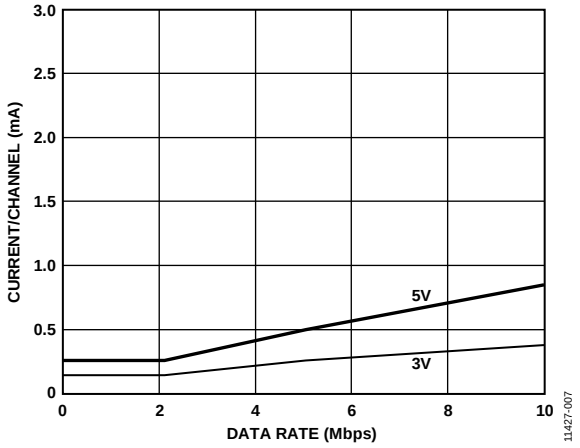


Figure 7. Typical Output Supply Current per Channel vs. Data Rate (No Load) for 5 V and 3.3 V Operation

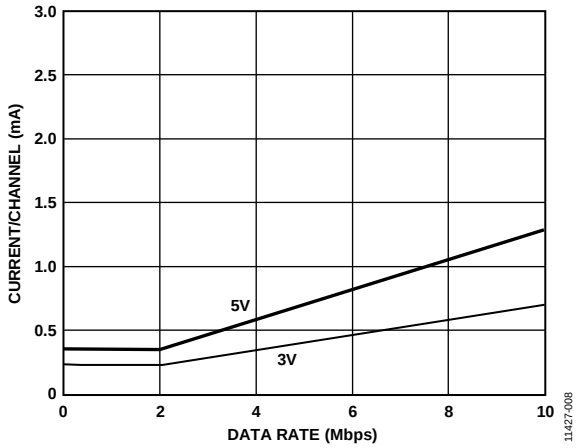


Figure 8. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load) for 5 V and 3.3 V Operation

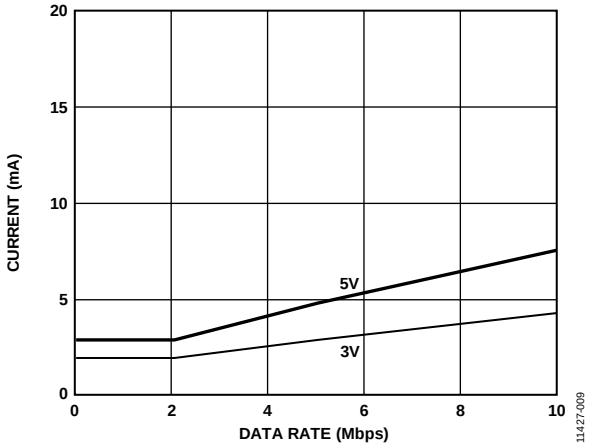


Figure 9. Typical ADuM3300W V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

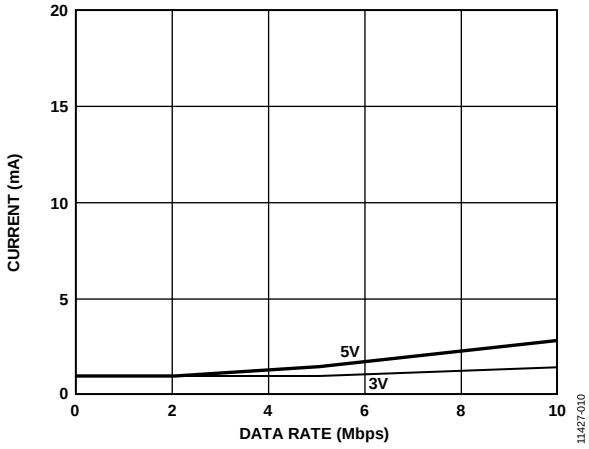


Figure 10. Typical ADuM3300W V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

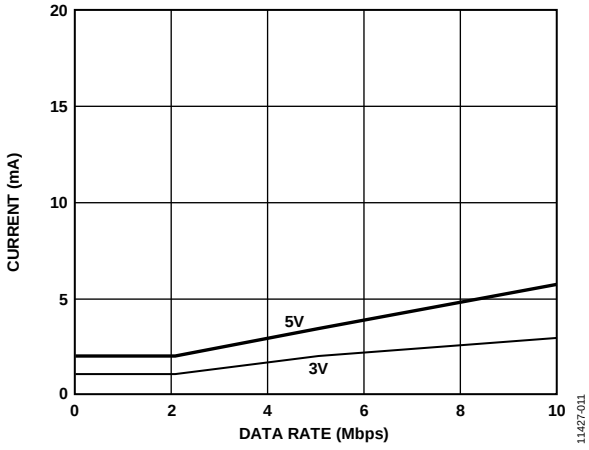


Figure 11. Typical ADuM3301W V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

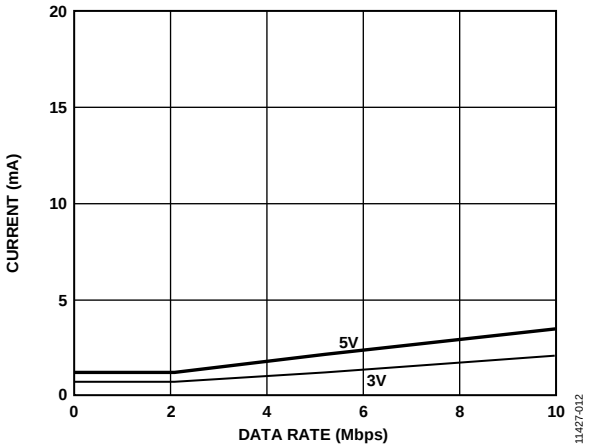


Figure 12. Typical ADuM3301W V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

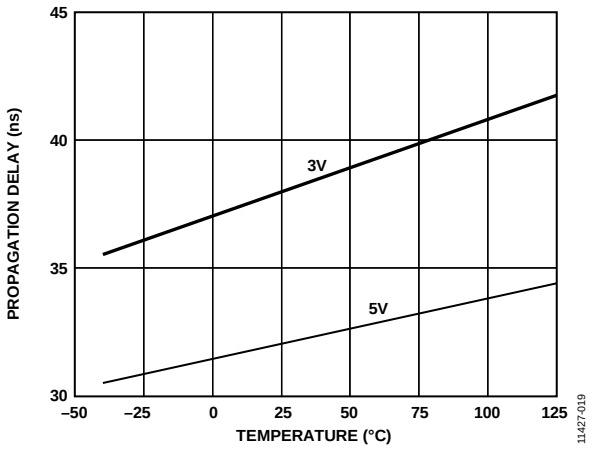


Figure 13. Propagation Delay vs. Temperature, B Grade for 5 V and 3.3 V Operation

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD LAYOUT

The ADuM3300W/ADuM3301W digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 14). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. Use capacitor values between 0.01 µF and 0.1 µF. Do not exceed 2 mm for total lead length between both ends of the capacitor and the input power supply pin. Consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16, unless the ground pair on each package side is connected close to the package.

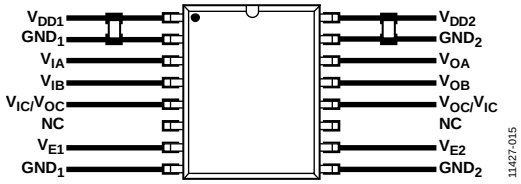


Figure 14. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur affects all pins equally on a given component side. Failure to ensure this can cause voltage differentials between pins, thereby exceeding the absolute maximum ratings for the device, leading to latch-up or permanent damage. See the AN-1109 Application Note for board layout guidelines.

SYSTEM LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM3300W/ADuM3301W incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include

- ESD protection cells are added to all input/output interfaces.
- Key metal trace resistances are reduced using wider geometry and paralleling of lines with vias.
- Guarding and isolation technique employed between the PMOS and NMOS devices minimizes the SCR effect inherent in CMOS devices.
- 45° corners on metal traces eliminate areas of high electric field concentration.
- Larger ESD clamps between each supply pin and its respective ground prevent supply pin overvoltage.

Although the ADuM3300W/ADuM3301W improve system level ESD reliability, these devices are no substitute for a robust system level design. See the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler® Isolation Products*, for detailed recommendations on board layout and system level design.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output (see Figure 15).

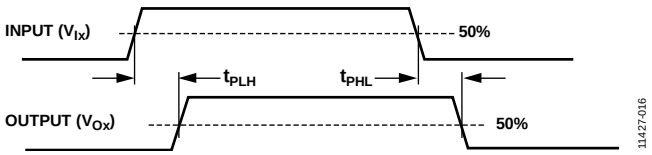


Figure 15. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3300W or ADuM3301W component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3300W and ADuM3301W components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit (see Table 21).

The limitation on the magnetic field immunity of the ADuM3300W/ADuM3301W is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM3300W/ADuM3301W is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, establishing a 0.5 V margin in which induced voltages are tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum\pi r_n^2; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the n^{th} turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3300W/ADuM3301W and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 16.

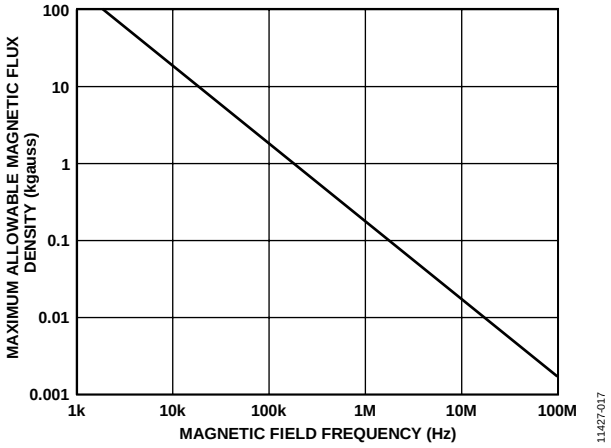


Figure 16. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such a magnetic field event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM3300W or ADuM3301W transformers. Figure 17 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM3300W/ADuM3301W are extremely immune and can be affected only by extremely large currents operating at high frequency very close to the component (see Figure 17). For the 1 MHz example noted, a 0.5 kA current would have to be placed 5 mm away from the ADuM3300W or ADuM3301W to affect the operation of the component.

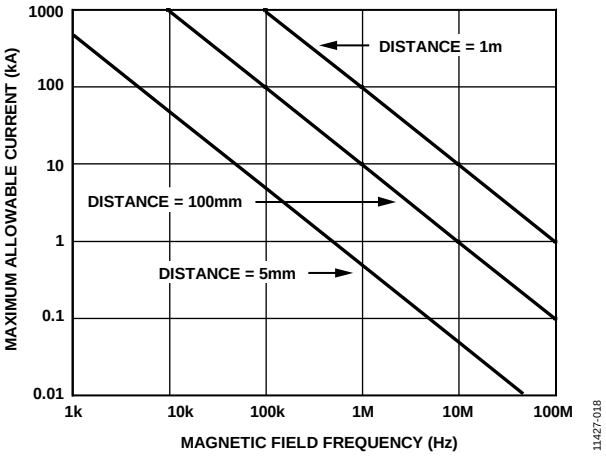


Figure 17. Maximum Allowable Current for Various Current to ADuM3300W/ADuM3301W Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board (PCB) traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM3300W or ADuM3301W isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad f \le 0.5\, f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \qquad f > 0.5\, f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \qquad f \le 0.5\, f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \qquad f > 0.5\, f_r$$

where:
$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 6 provides per channel input supply current as a function of data rate. Figure 7 and Figure 8 provide per channel output supply current as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 12 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM3300W/ADuM3301W channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices executes an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM3300W and ADuM3301W.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 19 summarize the peak voltage for 50 years of service life. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life.

The insulation lifetime of the ADuM3300W/ADuM3301W depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 18, Figure 19, and Figure 20 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 19 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Treat any cross insulation voltage waveform that does not conform to Figure 19 or Figure 20 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 19.

Note that the voltage presented in Figure 19 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

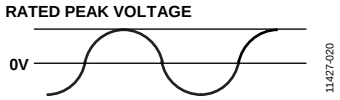


Figure 18. Bipolar AC Waveform

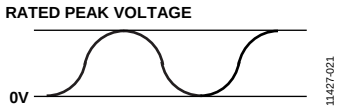


Figure 19. Unipolar AC Waveform

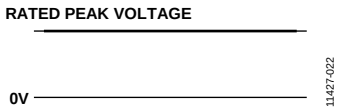


Figure 20. DC Waveform

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

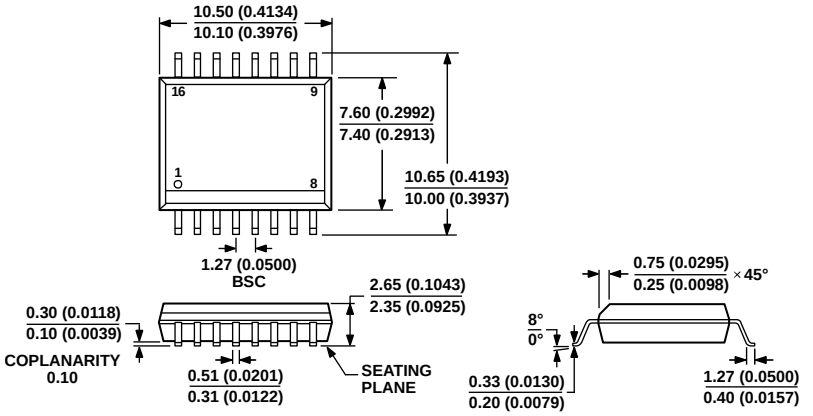


Figure 21. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Temperature Range	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Package Option[3]
ADuM3300WARWZ	−40°C to +125°C	3	0	1	100	40	RW-16
ADuM3300WBRWZ	−40°C to +125°C	3	0	10	36	3.5	RW-16
ADuM3301WARWZ	−40°C to +125°C	2	1	1	100	40	RW-16
ADuM3301WBRWZ	−40°C to +125°C	2	1	10	36	3.5	RW-16

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Tape and reel are available. The addition of an -RL suffix designates a 13-inch (1,000 units) tape and reel option.

AUTOMOTIVE PRODUCTS

The ADuM3300W and ADuM3301W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

NOTES

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