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GENERAL DESCRIPTION

The ADSP-BF512/BF512F, BF514/BF514F, BF516/BF516F, BF518/BF518F processors are members of the Blackfin family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The processors are completely code compatible with other Blackfin processors.

Table 1. Processor Comparison

Feature	ADSP-BF512	ADSP-BF512F	ADSP-BF514	ADSP-BF514F	ADSP-BF516	ADSP-BF516F	ADSP-BF518	ADSP-BF518F
IEEE-1588	–	–	–	–	–	–	1	1
Ethernet MAC	–	–	–	–	1	1	1	1
RSI	–	–	1	1	1	1	1	1
TWI	1	1	1	1	1	1	1	1
SPORTs	2	2	2	2	2	2	2	2
UARTs	2	2	2	2	2	2	2	2
SPIs	2	2	2	2	2	2	2	2
GP Timers	8	8	8	8	8	8	8	8
Watchdog Timers	1	1	1	1	1	1	1	1
RTC	1	1	1	1	1	1	1	1
PPI	1	1	1	1	1	1	1	1
Internal 4 Mbit SPI flash	–	1	–	1	–	1	–	1
Rotary Counter	1	1	1	1	1	1	1	1
3-phase PWM Pairs	3	3	3	3	3	3	3	3
GPIOs	40	40	40	40	40	40	40	40
Memory (bytes) L1 Instruction SRAM	32K							
Memory (bytes) L1 Instruction SRAM/Cache	16K							
Memory (bytes) L1 Data SRAM	32K							
Memory (bytes) L1 Data SRAM/Cache	32K							
Memory (bytes) L1 Scratchpad	4K							
Memory (bytes) L3 Boot ROM	32K							
Maximum Speed Grade	400 MHz							
Package Options	176-Lead LQFP With Exposed Pad							
	168-Ball CSP_BGA							

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF51x processors are highly integrated system-on-a-chip solutions for the next generation of embedded network connected applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include an IEEE-compliant 802.3 10/100 Ethernet MAC with IEEE-1588 support (ADSP-BF518/ADSP-BF518F only), an RSI controller, a TWI controller, two UART ports, two SPI ports, two serial ports (SPORTs), nine general purpose 32-bit timers (eight with PWM capability), three-phase PWM for motor control, a real-time clock, a watchdog timer, and a parallel peripheral interface (PPI).

PROCESSOR PERIPHERALS

The ADSP-BF51x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1 on Page 4). The processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, rotary counter, TWI, three-phase PWM, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

BLACKFIN PROCESSOR CORE

As shown in Figure 1 on Page 4, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

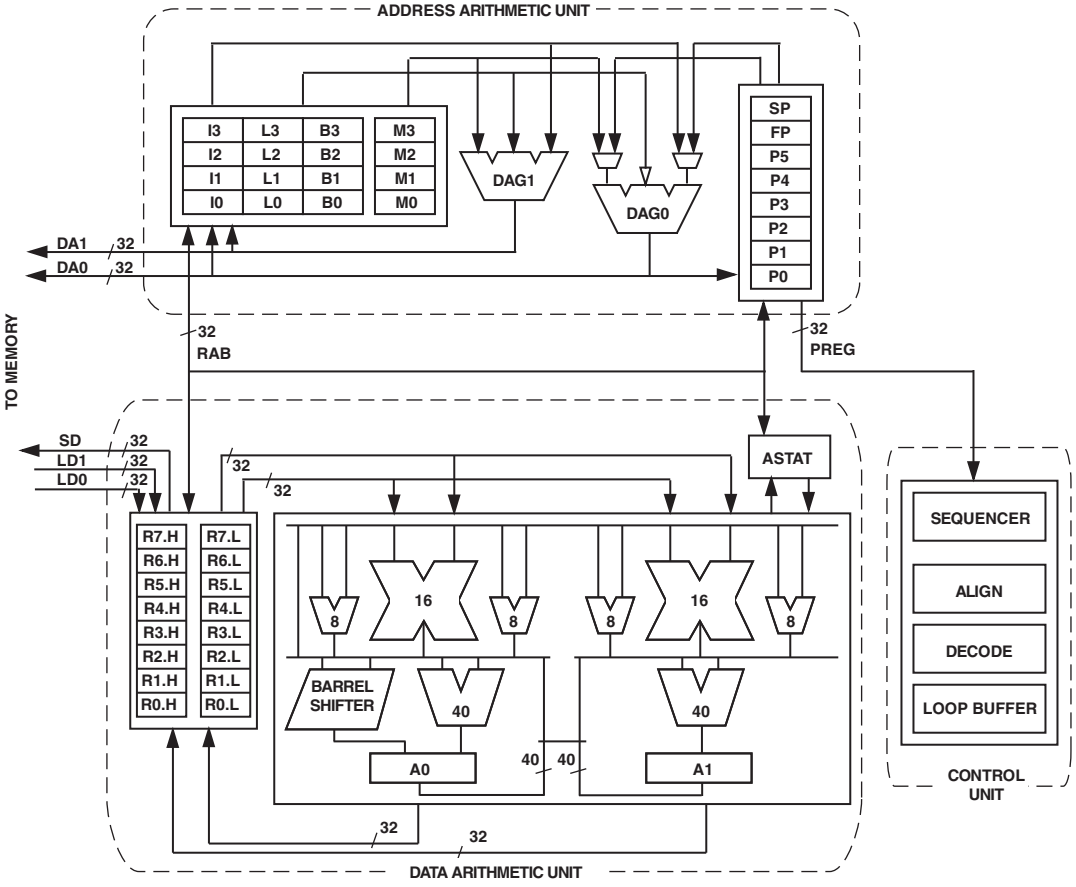


Figure 1. Blackfin Processor Core

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF51x processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency on-chip memory as cache or SRAM, and larger, lower-cost and performance off-chip memory systems. See Figure 2.

The on-chip L1 memory system is the highest-performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high-bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF51x processors have three blocks of on-chip memory providing high-bandwidth access to the core.

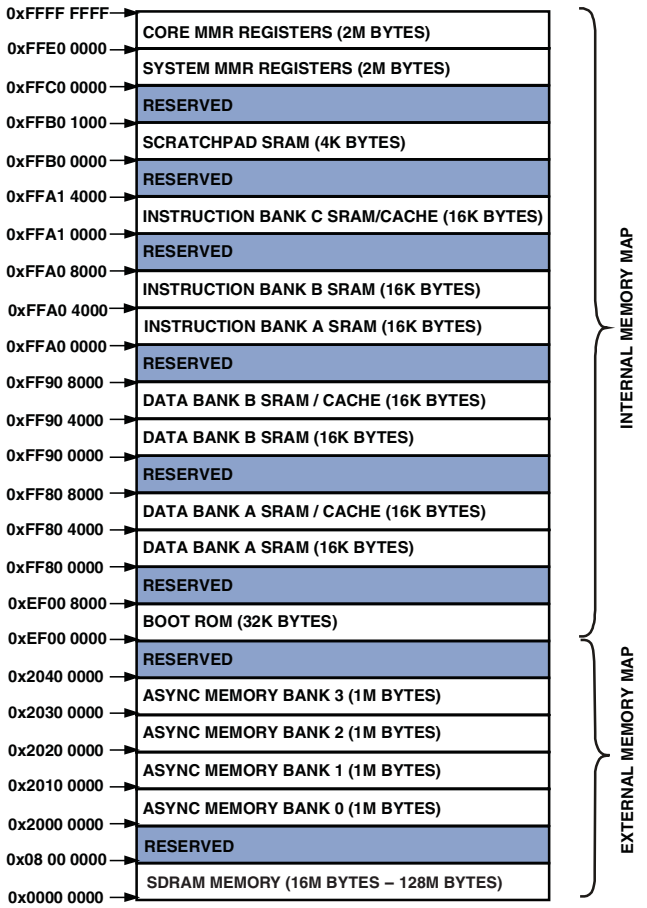


Figure 2. ADSP-BF51x Internal/External Memory Map

The first block is the L1 instruction memory, consisting of 48K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. A separate row can be open for each SDRAM internal bank and the SDRAM controller supports up to four internal SDRAM banks, improving overall performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

Flash Memory

The ADSP-BF512F/ADSP-BF514F/ADSP-BF516F/ ADSP-BF518F processors contain a SPI flash memory within the package of the processor and connected to SPI0 (Figure 3).

The SPI flash memory has a 4M bit capacity and 1.8V (nominal) operating voltage. The program/erase endurance is 100,000 cycles per block, and this memory has greater than 100 years data retention capability. Also included are support for software write protection and support for fast erase and byte-program.

The processors internally connect to the flash memory die with the MOSI, MISO, SPISSEL, and SPI_CLK signals similar to an external SPI flash (for signal descriptions, see Table 2 on Page 7). To further provide a secure processing environment, these internally connected signals are not exposed outside of the package. For this reason, programming the ADSP-BF51xF flash memory is performed by running code on the processor. It cannot be programmed from external signals and data transfers between the SPI flash and the processor cannot be probed externally. The Flash memory has the following additional features

- Serial Interface Architecture—SPI Compatible with Mode 0 and Mode 3
- Superior Reliability—Endurance of 100,000 cycles and greater than 100 years data retention
- Flexible Erase Capability—Uniform 4K Byte sectors and uniform 32 and 64K Byte overlay blocks
- Fast Erase and Byte-Program—Chip-erase time=125 ms (typical), Sector-/Block-Erase Time=62ms (typical) Byte-Program Time=50 µS (typical)
- Auto Address Increment (AAI) Programming—Decreases total chip programming time over byte-program operations
- End-of-Write Detection—Software polling the BUSY bit in status register, busy status readout on SO pin
- Software Write Protection—Write protection through block-protection bits in status register

Combinational Logic Truth Table

$\overline{SEL4}$ or PH8	MISO_EXT, SPICLK_EXT, MOSI_EXT
0	Three-state
1	As programmed

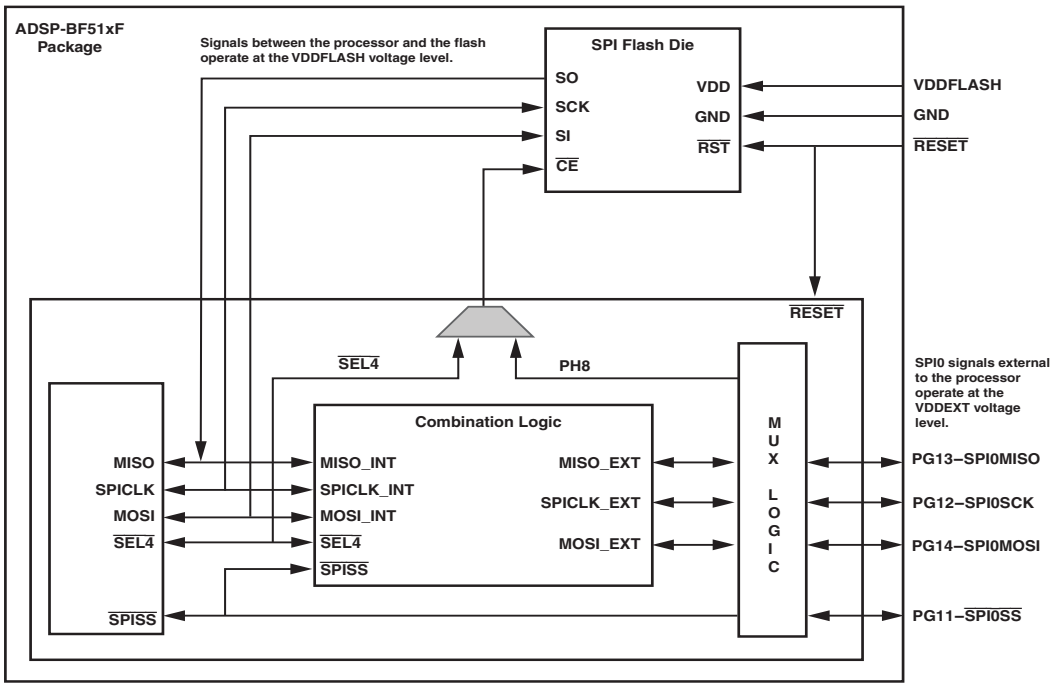


Figure 3. Flash Memory Block Diagram

Table 2. Internal Flash Memory Signal Descriptions

Symbol	Pin Name	Function
SCK	Serial Clock	Provides the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	Transfers commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	Transfers data serially out of the device. Data is shifted out on the falling edge of the serial clock. Flash busy status pin in AAI mode if SO is configured as a hardware RY/$\overline{BY}$ pin.
$\overline{CE}$	Chip Enable	The device is enabled by a high to low transition on $\overline{CE}$. $\overline{CE}$ must remain low for the duration of any command sequence.
$\overline{RST}$	Reset	Resets the operation of the device and the internal logic. This signal is tied to the ADSP-BF51x $\overline{RESET}$ signal.

One-Time Programmable Memory

The processors have 64K bits of one-time programmable non-volatile memory that can be programmed by the developer only one time. It includes the array and logic to support read access and programming. Additionally, its pages can be write protected.

OTP enables developers to store both public and private data on-chip. In addition to storing public and private key data for applications requiring security, it also allows developers to store completely user-definable data such as customer ID, product ID, and MAC address. Hence generic parts can be shipped which are then programmed and protected by the developer within this non-volatile memory.

I/O Memory Space

The processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The processors contain a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the processors are configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 18.

Event Handling

The event controller handles all asynchronous and synchronous events to the processor. The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor through the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow; that is, the exception is taken before the instruction is allowed to complete. Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt

inputs to support the peripherals of the processors. Table 3 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 4 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

Table 4. Peripheral Interrupt Assignment

Peripheral Interrupt Event	General Purpose Interrupt (at Reset)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Registers	
PLL Wakeup Interrupt	IVG7	0	0	IAR0	IMASK0 and ISR0
DMA Error 0 (generic)	IVG7	1	0	IAR0	IMASK0 and ISR0
DMAR0 Block Interrupt	IVG7	2	0	IAR0	IMASK0 and ISR0
DMAR1 Block Interrupt	IVG7	3	0	IAR0	IMASK0 and ISR0
DMAR0 Overflow Error	IVG7	4	0	IAR0	IMASK0 and ISR0
DMAR1 Overflow Error	IVG7	5	0	IAR0	IMASK0 and ISR0
PPI Error	IVG7	6	0	IAR0	IMASK0 and ISR0
MAC Status	IVG7	7	0	IAR0	IMASK0 and ISR0
SPORT0 Status	IVG7	8	0	IAR1	IMASK0 and ISR0
SPORT1 Status	IVG7	9	0	IAR1	IMASK0 and ISR0
PTP Error Interrupt	IVG7	10	0	IAR1	IMASK0 and ISR0
Reserved	IVG7	11	0	IAR1	IMASK0 and ISR0
UART0 Status	IVG7	12	0	IAR1	IMASK0 and ISR0
UART1 Status	IVG7	13	0	IAR1	IMASK0 and ISR0
RTC	IVG8	14	1	IAR1	IMASK0 and ISR0
DMA 0 Channel (PPI)	IVG8	15	1	IAR1	IMASK0 and ISR0
DMA 3 Channel (SPORT0 RX)	IVG9	16	2	IAR2	IMASK0 and ISR0
DMA 4 Channel (SPORT0 TX/RSI)	IVG9	17	2	IAR2	IMASK0 and ISR0
DMA 5 Channel (SPORT1 RX/SPI1)	IVG9	18	2	IAR2	IMASK0 and ISR0
DMA 6 Channel (SPORT1 TX)	IVG9	19	2	IAR2	IMASK0 and ISR0
TWI	IVG10	20	3	IAR2	IMASK0 and ISR0
DMA 7 Channel (SPI0)	IVG10	21	3	IAR2	IMASK0 and ISR0

Table 4. Peripheral Interrupt Assignment (Continued)

Peripheral Interrupt Event	General Purpose Interrupt (at Reset)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Registers	
DMA8 Channel (UART0 RX)	IVG10	22	3	IAR2	IMASK0 and ISR0
DMA9 Channel (UART0 TX)	IVG10	23	3	IAR2	IMASK0 and ISR0
DMA10 Channel (UART1 Rx)	IVG10	24	3	IAR3	IMASK0 and ISR0
DMA11 Channel (UART1 Tx)	IVG10	25	3	IAR3	IMASK0 and ISR0
OTP Memory Interrupt	IVG11	26	4	IAR3	IMASK0 and ISR0
GP Counter	IVG11	27	4	IAR3	IMASK0 and ISR0
DMA1 Channel (MAC RX)	IVG11	28	4	IAR3	IMASK0 and ISR0
Port H Interrupt A	IVG11	29	4	IAR3	IMASK0 and ISR0
DMA2 Channel (MAC TX)	IVG11	30	4	IAR3	IMASK0 and ISR0
Port H Interrupt B	IVG11	31	4	IAR3	IMASK0 and ISR0
Timer 0	IVG12	32	5	IAR4	IMASK1 and ISR1
Timer 1	IVG12	33	5	IAR4	IMASK1 and ISR1
Timer 2	IVG12	34	5	IAR4	IMASK1 and ISR1
Timer 3	IVG12	35	5	IAR4	IMASK1 and ISR1
Timer 4	IVG12	36	5	IAR4	IMASK1 and ISR1
Timer 5	IVG12	37	5	IAR4	IMASK1 and ISR1
Timer 6	IVG12	38	5	IAR4	IMASK1 and ISR1
Timer 7	IVG12	39	5	IAR4	IMASK1 and ISR1
Port G Interrupt A	IVG12	40	5	IAR5	IMASK1 and ISR1
Port G Interrupt B	IVG12	41	5	IAR5	IMASK1 and ISR1
MDMA Stream 0	IVG13	42	6	IAR5	IMASK1 and ISR1
MDMA Stream 1	IVG13	43	6	IAR5	IMASK1 and ISR1
Software Watchdog Timer	IVG13	44	6	IAR5	IMASK1 and ISR1
Port F Interrupt A	IVG13	45	6	IAR5	IMASK1 and ISR1
Port F Interrupt B	IVG13	46	6	IAR5	IMASK1 and ISR1
SPI0 Status	IVG7	47	0	IAR5	IMASK1 and ISR1
SPI1 Status	IVG7	48	0	IAR6	IMASK1 and ISR1
Reserved	IVG7	49	0	IAR6	IMASK1 and ISR1
Reserved	IVG7	50	0	IAR6	IMASK1 and ISR1
RSI Interrupt0	IVG10	51	3	IAR6	IMASK1 and ISR1
RSI Interrupt1	IVG10	52	3	IAR6	IMASK1 and ISR1
PWM Trip Interrupt	IVG10	53	3	IAR6	IMASK1 and ISR1
PWM Sync Interrupt	IVG10	54	3	IAR6	IMASK1 and ISR1
PTP Status Interrupt	IVG10	55	3	IAR6	IMASK1 and ISR1

Event Control

The ADSP-BF51x processors provide a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide.

- CEC interrupt latch register (ILAT) – Indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – Controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be

latched in the ILAT register. This register may be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)

- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 4 on Page 8.

- SIC interrupt mask registers (SIC_IMASKx) – Control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status registers (SIC_ISRx) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable registers (SIC_IWRx) – By enabling the corresponding bit in these registers, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. For more information see Dynamic Power Management on Page 15.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF51x processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC, RSI, SPORTs, SPIs, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processors' DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels that transfer data between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The processors also have an external DMA controller capability via dual external DMA request signals when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

REAL-TIME CLOCK

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processors. The RTC peripheral has a dedicated power supply so that it can remain powered up and clocked even when the rest of the processor is in a low-power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

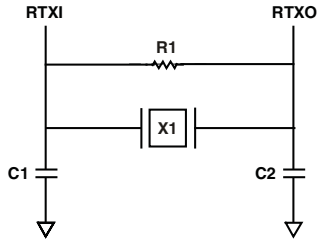
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode or cause a transition from the hibernate state.

Connect RTC signals RTXI and RTXO with external components as shown in Figure 4.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 4. External Components for RTCT

WATCHDOG TIMER

The ADSP-BF51x processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are nine general-purpose programmable timer units in the ADSP-BF51x processors. Eight timers have an external signal that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF signals, an external clock input to the PPI_CLK input signal, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

3-PHASE PWM

Features of the 3-phase PWM generation unit are:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to an external synchronization
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

The processors integrate a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction (ACIM) or permanent magnet synchronous (PMSM) motor control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control

of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

The six PWM output signals consist of three high-side drive signals (PWM_AH, PWM_BH, and PWM_CH) and three low-side drive signals (PWM_AL, PWM_BL, and PWM_CL). The polarity of the generated PWM signal be set with software, so that either active HI or active LO PWM patterns can be produced.

The switching frequency of the generated PWM pattern is programmable using the 16-bit PWMTM register. The PWM generator can operate in single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period, so that the resultant PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

GENERAL-PURPOSE (GP) COUNTER

A 32-bit GP counter is provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumb wheels. The counter can also operate in general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input signal or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three signals have a programmable debouncing circuit.

An internal signal forwarded to the GP timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

SERIAL PORTS

The ADSP-BF51x processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive signals, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The processors have two SPI-compatible ports (SPI0 and SPI1) that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three signals for transferring data: two data signals (master output-slave input–MOSI, and master input-slave output–MISO) and a clock signal (serial clock–SCK). An SPI chip select input signal ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and multiple SPI chip select output signals let the processor select other SPI devices. The SPI select signals are reconfigured general-purpose I/O signals. Using these signals, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS

The ADSP-BF51x processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from seven to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

Where the 16-bit UART_Divisor comes from the UART_DLH (most significant 8 bits) and UART_DLL (least significant 8 bits) registers.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

TWO WIRE INTERFACE (TWI)

The processors include a TWI module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two signals for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface signals are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

REMOVABLE STORAGE INTERFACE (RSI)

The RSI controller, available on the ADSP-BF514, ADSP-BF516, ADSP-BF518, and ADSP-BF518F acts as the host interface for multi-media cards (MMC), secure digital memory cards (SD Card), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

10/100 ETHERNET MAC

The ADSP-BF518/ADSPBF518F processors offer the capability to directly connect to a network by way of an embedded fast Ethernet media access controller (MAC) that supports both 10-BaseT (10M bits/sec) and 100-BaseT (100M bits/sec) operation. The 10/100 Ethernet MAC peripheral on the processor is fully compliant to the IEEE 802.3-2002 standard and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are:

- Support of MII and RMII protocols for external PHYs
- Full duplex and half duplex modes
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing
- Flow control (in full-duplex operation): generation and detection of pause frames
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers
- SCLK operating range down to 25 MHz (active and sleep operating modes)
- Internal loopback from transmit to receive

Some advanced features are:

- Buffered crystal output to external PHY for support of a single crystal system
- Automatic checksum computation of IP header and IP payload fields of Rx frames

- Independent 32-bit descriptor-driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations
- Convenient frame alignment modes support even 32-bit alignment of encapsulated receive or transmit IP packet data in memory after the 14-byte MAC header
- Programmable Ethernet event interrupt supports any combination of:
  - Selected receive or transmit frame status conditions
  - PHY interrupt condition
  - Wakeup frame detected
  - Selected MAC management counter(s) at half-full
  - DMA descriptor error
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value
- Programmable receive address filters, including a 64-bin address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames
- Advanced power management supporting unattended transfer of receive and transmit frames and status to/from external memory via DMA during low-power sleep mode
- System wakeup from sleep operating mode upon magic packet or any of four user-definable wakeup frame filters
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression
- In RMII operation, seven unused signals may be configured as GPIO signals for other purposes

IEEE 1588 SUPPORT

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The ADSP-BF518/ADSP-BF518F processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC). This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the PTP_SYNC engine are:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of 12.5 ns resolution
- Lock adjustment
- Programmable PTM message support
- Dedicated interrupts
- Programmable alarm
- Multiple input clock sources (SCLK, MII clock, external clock up to 50 MHz)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

PORTS

Because of the rich set of peripherals, the processors group the many peripheral signals to four ports—port F, port G, port H, and port J. Most of the associated pins/balls are shared by multiple signals. The ports function as multiplexer controls.

General-Purpose I/O (GPIO)

The ADSP-BF51x processors have 40 bidirectional, general-purpose I/O (GPIO) signals allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Each GPIO-capable signal shares functionality with other peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output nor input drivers are active by default. Each general-purpose port signal can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO signal as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO signals to be modified in a single instruction, without affecting the level of any other GPIO signals. Four control registers are provided. One register is written in order to set signal values, one register is written in order to clear signal values, one register is written in order to toggle signal values, and one register is written in order to specify a signal value. Reading the GPIO status register allows software to interrogate the sense of the signals.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO signal to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual signal values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO signals defined as inputs can be configured to generate hardware interrupts, while output signals can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual signals are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE (PPI)

The ADSP-BF51x processors provide a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, ITU-R-601/656 video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock signal, up to three frame synchronization signals, and up to 16 data signals.

In ITU-R-656 modes, the PPI receives and parses a data stream of 8-bit or 10-bit data elements. On-chip decode of embedded preamble control and synchronization information is supported.

Three distinct ITU-R-656 modes are supported:

- Active video only mode – The PPI does not read in any data between the End of Active Video (EAV) and Start of Active Video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI.
- Vertical blanking only mode – The PPI only transfers vertical blanking interval (VBI) data, as well as horizontal blanking information and control byte sequences on VBI lines.
- Entire field mode – The entire incoming bitstream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals.

Though not explicitly supported, ITU-R-656 output functionality can be achieved by setting up the entire frame structure (including active video, blanking, and control information) in memory and streaming the data out the PPI in a frame sync-less mode. The processor's 2-D DMA features facilitate this transfer by allowing the static frame buffer (blanking and control codes) to be placed in memory once, and simply updating the active video information on a per-frame basis.

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. The modes are divided into four main categories, each allowing up to 16 bits of data transfer per PPI_CLK cycle:

- Data receive with internally generated frame syncs
- Data receive with externally generated frame syncs
- Data transmit with internally generated frame syncs
- Data transmit with externally generated frame syncs

These modes support ADC/DAC connections, as well as video communication with hardware signalling. Many of the modes support more than one level of frame synchronization. If desired, a programmable delay can be inserted between assertion of a frame sync and reception/transmission of data.

CODE SECURITY WITH LOCKBOX SECURE TECHNOLOGY

A security system consisting of a blend of hardware and software provides customers with a flexible and rich set of code security features with Lockbox secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets.

DYNAMIC POWER MANAGEMENT

The ADSP-BF51x processors provide four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. When configured for a 0 volt core supply voltage, the processor enters the hibernate state. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 5 for a summary of the power settings for each mode.

Table 5. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wakeup causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the Active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and system blocks (SCLK). Any critical information stored internally (memory contents, register contents, etc.) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved. Writing b#00 to the FREQ bits in the VR_CTL register also causes EXT_WAKE to transition low, which can be used to signal an external voltage regulator to shut down.

Since V_{DDEXT} is still supplied in this mode, all of the external signals three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

The Ethernet module can signal an external regulator to wake up using EXT_WAKE. If PF15 does not connect as a $\overline{\text{PHYINT}}$ signal to an external PHY device, it can be pulled low by any other device to wake the processor up. The processor can also be woken up by a real-time clock wakeup event or by asserting the $\overline{\text{RESET}}$ pin. All hibernate wakeup events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register. The EXT_WAKE signal is provided to indicate the occurrence of wakeup events.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in the hibernate state. State variables may be held in external SRAM or SDRAM. The SCKELOW bit in the VR_CTL register controls whether or not SDRAM operates in self-refresh mode, which allows it to retain its content while the processor is in hibernation and through the subsequent reset sequence.

Power Savings

As shown in Table 6, the processors support up to six different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor Operating Conditions; even if the feature/peripheral is not used.

Table 6. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC, Memory, OTP	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
Memory logic	V_{DDMEM}
OTP logic	V_{DDOTP}
Optional internal flash	$V_{DDFLASH}$
All other I/O	V_{DDEXT}

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

$$\textit{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ \textit{Power Savings} = (1 - \textit{Power Savings Factor}) \times 100\%$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

T_{NOM} is the duration running at $f_{CCLKNOM}$

T_{RED} is the duration running at $f_{CCLKRED}$

VOLTAGE REGULATION INTERFACE

The ADSP-BF51x processors require an external voltage regulator to power the V_{DDINT} domain. To reduce standby power consumption in the hibernate state, the external voltage regulator can be signaled through EXT_WAKE to remove power from the processor core. EXT_WAKE is high-true for power-up and may be connected directly to the low-true shut down input of many common regulators.

The Power Good ($\overline{PG}$) input signal allows the processor to start only after the internal voltage has reached a chosen level. In this way, the startup time of the external regulator is detected after hibernation. For a complete description of the $\overline{PG}$ functionality, refer to the *ADSP-BF51x Blackfin Processor Hardware Reference*.

CLOCK SIGNALS

The ADSP-BF51x processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

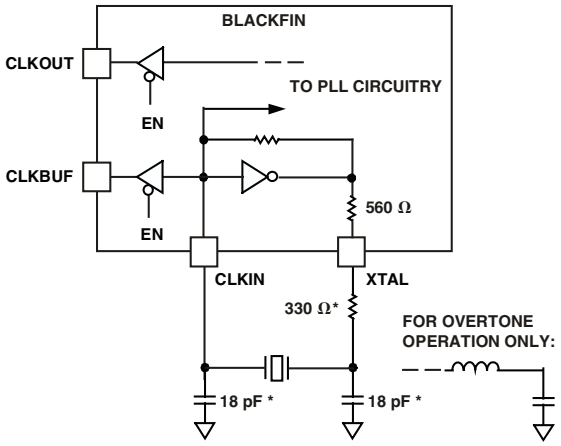
If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor CLKIN signal. When an external clock is used, the XTAL pin/ball must be left unconnected.

Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 5. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins/balls. The on-chip resistance between the CLKIN pin/ball and the XTAL pin/ball is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 5 fine tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 5 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 5. A design procedure for third-overtone operation is discussed in detail in application note *(EE-168) Using Third Overtone Crystals with the ADSP-218x DSP* on the Analog Devices website (www.analog.com)—use site search on "EE-168."

The CLKBUF signal is an output signal, which is a buffered version of the input clock. This signal is particularly useful in Ethernet applications to limit the number of required clock sources in the system. In this type of application, a single



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18 pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 5. External Crystal Connections

25 MHz or 50 MHz crystal may be applied directly to the processor. The 25 MHz or 50 MHz output of CLKBUF can then be connected to an external Ethernet MII or RMII PHY device.

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 6, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 5×, but it can be modified by a software instruction sequence.

On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register. The maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT}, V_{DDEXT}, and V_{DDMEM}, the VCO is always permitted to run up to the frequency specified by the part's speed grade. The CLKOUT signal reflects the SCLK frequency to the off-chip world. It belongs to the SDRAM interface, but it functions as reference signal in other timing specifications as well. While active by default, it can be disabled using the EBIU_SDGCTL and EBIU_AMGCTL registers.

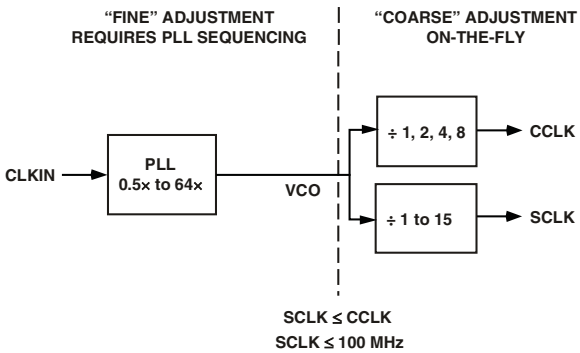


Figure 6. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 7 illustrates typical system clock ratios.

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

Table 7. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	50	50
0110	6:1	300	50
1010	10:1	400	40

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 8. This programmable core clock capability is useful for fast core frequency modifications.

Table 8. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

The maximum CCLK frequency not only depends on the part's speed grade (see Page 68), it also depends on the applied V_{DDINT} voltage. See Table 12 for details. The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDINT}, V_{DDEXT}, and V_{DDMEM} voltages (see Table 15 on Page 25).

BOOTING MODES

The processor has several mechanisms (listed in Table 9) for automatically loading internal and external memory after a reset. The boot mode is defined by three BMODE input bits dedicated to this purpose. There are two categories of boot modes. In master boot modes the processor actively loads data from parallel or serial memories. In slave boot modes the processor receives data from external host devices.

The boot modes listed in Table 9 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time or by proper OTP programming at pre-boot time. The BMODE bits of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 9.

Table 9. Booting Modes

BMODE2–0	Description
000	Idle - No boot
001	Boot from 8- or 16-bit external flash memory
010	Boot from internal SPI memory
011	Boot from external SPI memory (EEPROM or flash)
100	Boot from SPI0 host
101	Boot from OTP memory
110	Boot from SDRAM
111	Boot from UART0 Host

- Idle/no boot mode (BMODE = 0x0) — In this mode, the processor goes into idle. The idle boot mode helps recover from illegal operating modes, such as when the user has mis configured the OTP memory.
- Boot from 8-bit or 16-bit external flash memory (BMODE = 0x1) — In this mode, the boot kernel loads the first block header from address 0x2000 0000 and—depending on instructions containing in the header—the boot kernel performs 8-bit or 16-bit boot or starts program execution at the address provided by the header. By default, all configuration settings are set for the slowest device possible (3-cycle hold time, 15-cycle R/W access times, 4-cycle setup).

  The ARDY is not enabled by default, but it can be enabled by OTP programming. Similarly, all interface behavior and timings can be customized by OTP programming. This includes activation of burst-mode or page-mode operation. In this mode, all signals belonging to the asynchronous interface are enabled at the port muxing level.
- Boot from internal SPI memory (BMODE = 0x2) — The processor uses SPI0 to load from code previously loaded to the 4 Mbit internal SPI flash. Only available on the ADSP-BF512F/ADSP-BF514F/ADSP-BF516F/ADSP-BF518F.
- Boot from external SPI EEPROM or flash (BMODE = 0x3) — 8-bit, 16-bit, 24-bit or 32-bit addressable devices are supported. The processor uses the PG15 GPIO signal (at SPI0SSEL2) to select a single SPI EEPROM/flash device connected to the SPI0 interface; then submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the SSEL and MISO signals. By default, a value of 0x85 is written to the SPI0_BAUD register.
- Boot from SPI0 host device (BMODE = 0x4) — The processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. In the host, the HWAIT signal must be interrogated

by the host before every transmitted byte. A pull-up resistor is required on the $\overline{\text{SPI0SS}}$ input. A pull-down on the serial clock may improve signal quality and booting robustness.

- Boot from OTP memory (BMODE = 0x5) — This provides a stand-alone booting method. The boot stream is loaded from on-chip OTP memory. By default the boot stream is expected to start from OTP page 0x40 on and can occupy all public OTP memory up to page 0xDF. This is 2560 bytes. Since the start page is programmable the maximum size of the boot stream can be extended to 3072 bytes.
- Boot from SDRAM (BMODE = 0x6) This is a warm boot scenario, where the boot kernel starts booting from address 0x0000 0010. The SDRAM is expected to contain a valid boot stream and the SDRAM controller must be configured by the OTP settings.
- Boot from UART0 host (BMODE = 0x7) — Using an auto-baud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities.

  When performing the autobaud, the UART expects a "@" (0x40) character (eight bits data, one start bit, one stop bit, no parity bit) on the RX0 signal to determine the bit rate. The UART then replies with an acknowledgement composed of 4 bytes (0xBF—the value of UART0_DLL and 0x00—the value of UART0_DLH). The host can then download the boot stream. To hold off the host the Blackfin processor signals the host with the boot host wait (HWAIT) signal. Therefore, the host must monitor HWAIT before every transmitted byte.

For each of the boot modes, a 16-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

Prior to booting, the pre-boot routine interrogates the OTP memory. Individual boot modes can be customized or even disabled based on OTP programming. External hardware, especially booting hosts may watch the HWAIT signal to determine when the pre-boot has finished and the boot kernel starts the boot process. By programming OTP memory, the user can instruct the preboot routine to also customize the PLL, the SDRAM Controller, and the Asynchronous Interface.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the later case. Bits 6-4 in the system reset configuration (SYSCR) register can be used to bypass pre-boot routine and/or boot kernel in case of a software reset. They can also be used to simulate a wakeup-from-hibernate boot in the software reset case.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to configure the SDRAM controller or to speed up booting by managing PLL, clock frequencies, wait states, or serial bit rates.

The boot ROM also features C-callable function entries that can be called by the user application at run time. This enables second-stage boot or boot management schemes to be implemented with ease.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-harvard architecture, which supports two 16-bit MACs or four 8-bit ALUs plus two load/store plus two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

The ADSP-BF51x processors are supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other Blackfin processors also fully emulates the ADSP-BF51x processors. For more information about development tools, visit www.analog.com.

EZ-KIT Lite Evaluation Board

For evaluation of the processors, use the EZ-KIT Lite® board being developed by Analog Devices. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

DESIGNING AN EMULATOR-COMPATIBLE PROCESSOR BOARD (TARGET)

The Analog Devices family of emulators are tools that every system developer needs in order to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *(EE-68) Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

RELATED DOCUMENTS

The following publications that describe the ADSP-BF512/ADSP-BF514/ADSP-BF516/ADSP-BF518 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF512/BF512F, BF514/BF514F, BF516/BF516F, BF518/BF518F Blackfin Processor Hardware Reference*
- *ADSP-BF53x/BF56x Blackfin Processor Programming Reference*
- *ADSP-BF512/BF512F, BF514/BF514F, BF516/BF516F, BF518/BF518F Blackfin Processor Anomaly List*

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SIGNAL DESCRIPTIONS

The processors' signal definitions are listed in Table 10. In order to maintain maximum function and reduce package size and signal count, some signals have dual, multiplexed functions. In cases where signal function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate.

All I/O signals have their input buffers disabled with the exception of the signals noted in the data sheet that need pull-ups or pull downs if unused.

The SDA (serial data) and SCL (serial clock) pins/balls are open drain and therefore require a pullup resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements. If no IBIS simulation is performed, it is strongly recommended to add series resistor terminations for all Driver Types A, C and D. The termination resistors should be placed near the processor to reduce transients and improve signal integrity. The resistance value, typically 33 Ω or 47 Ω, should be chosen to match the average board trace impedance. Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 10. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
EBIU			
ADDR19–1	O	Address Bus	A
DATA15–0	I/O	Data Bus	A
$\overline{\text{ABE1–0}}$/*SDQM1–0*	O	Byte Enable or Data Mask	A
$\overline{\text{AMS1–0}}$	O	Bank Select	A
$\overline{\text{ARE}}$	O	Asynchronous Memory Read Enable	A
$\overline{\text{AWE}}$	O	Write Enable for Async	A
$\overline{\text{SRAS}}$	O	SDRAM Row Address Strobe	A
$\overline{\text{SCAS}}$	O	SDRAM Column Address Strobe	A
$\overline{\text{SWE}}$	O	SDRAM Write Enable	A
SCKE	O	SDRAM Clock Enable	A
CLKOUT	O	SDRAM Clock Output	B
SA10	O	SDRAM A10 Signal	A
$\overline{\text{SMS}}$	O	SDRAM Bank Select	A
Port F: GPIO and Multiplexed Peripherals			
PF0/*ETxD2/PPI D0/*$\overline{\textit{SPI1SEL2}}$*/TACLK6*	I/O	GPIO/*Ethernet MII Transmit D2/PPI Data 0/SPI1 Slave Select 2/Timer6 Alternate Clock*	C
PF1/*ERxD2/PPI D1/PWM AH/TACLK7*	I/O	GPIO/*Ethernet MII Receive D2/PPI Data 1/PWM AH Output/Timer7 Alternate Clock*	C
PF2/*ETxD3/PPI D2/PWM AL*	I/O	GPIO/*Ethernet Transmit D3/PPI Data 2/PWM AL Output*	C
PF3/*ERxD3/PPI D3/PWM BH/TACLK0*	I/O	GPIO/*Ethernet MII Data Receive D3/PPI Data 3/PWM BH Output/Timer0 Alternate Clock*	C
PF4/*ERxCLK/PPI D4/PWM BL/TACLK1*	I/O	GPIO/*Ethernet MII Receive Clock/PPI Data 4/PWM BL Out/Timer1 Alternate CLK*	C
PF5/*ERxDV/PPI D5/PWM CH/TACI0*	I/O	GPIO/*Ethernet MII Receive Data Valid/PPI Data 5/PWM CH Out /Timer0 Alternate Capture Input*	C
PF6/*COL/PPI D6/PWM CL/TACI1*	I/O	GPIO/*Ethernet MII Collision/PPI Data 6/PWM CL Out/Timer1 Alternate Capture Input*	C
PF7/$\overline{\textit{SPI0SEL1}}$*/PPI D7/PWMSYNC*	I/O	GPIO/*SPI0 Slave Select 1/PPI Data 7/PWM Sync*	C
PF8/*MDC*/PPI D8/$\overline{\textit{SPI1SEL4}}$	I/O	GPIO/*Ethernet Management Channel Clock/PPI Data 8/SPI1 Slave Select 4*	C
PF9/*MDIO/PPI D9/TMR2*	I/O	GPIO/*Ethernet Management Channel Serial Data/PPI Data 9/Timer 2*	C

Table 10. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
PF10/*ETxD0/PPI D10/TMR3*	I/O	GPIO/*Ethernet MII or RMII Transmit D0/PPI Data 10/Timer 3*	C
PF11/*ERxD0/PPI D11/PWM AH/TACI3*	I/O	GPIO/*Ethernet MII Receive D0/PPI Data 11/PWM AH output /Timer3 Alternate Capture Input*	C
PF12/*ETxD1/PPI D12/PWM AL*	I/O	GPIO/*Ethernet MII Transmit D1/PPI Data 12/PWM AL Output*	C
PF13/*ERxD1/PPI D13/PWM BH*	I/O	GPIO/*Ethernet MII or RMII Receive D1/PPI Data 13/PWM BH Output*	C
PF14/*ETxEN/PPI D14/PWM BL*	I/O	GPIO/*Ethernet MII Transmit Enable/PPI Data 14/PWM BL Out*	C
PF15[2]/*$\overline{\text{RMII PHYINT}}$/PPI D15/PWM_SYNCA*	I/O	GPIO/*Ethernet MII PHY Interrupt/PPI Data 15/Alternate PWM Sync*	C
Port G: GPIO and Multiplexed Peripherals			
PG0/*MIICRS/RMIICRS/HWAIT*[3]*/$\overline{\text{SPI1SEL3}}$*	I/O	GPIO/*Ethernet MII or RMII Carrier Sense or RMII Data Valid/HWAIT/SPI1 Slave Select3*	C
PG1/*ERxER/DMAR1/PWM CH*	I/O	GPIO/*Ethernet MII or RMII Receive Error/DMA Req 1/PWM CH Out*	C
PG2/*MIITxCLK/RMIIREF_CLK/DMAR0/PWM CL*	I/O	GPIO/*Ethernet MII or RMII Reference Clock/DMA Req 0/PWM CL Out*	C
PG3/*DR0PRI/RSI_DATA0/$\overline{\text{SPI0SEL5}}$/TACLK3*	I/O	GPIO/*SPORT0 Primary Rx Data/RSI Data 0/SPI0 Slave Select 5/Timer3 Alternate CLK*	C
PG4/*RSCLK0/RSI_DATA1/TMR5/TACI5*	I/O	GPIO/*SPORT0 Rx Clock/RSI Data 1/Timer 5/Timer5 Alternate Capture Input*	D
PG5/*RFS0/RSI_DATA2/PPICLK/TMRCLK*	I/O	GPIO/*SPORT0 Rx Frame Sync/RSI Data 2/PPI Clock/External Timer Reference*	C
PG6/*TFS0/RSI_DATA3/TMR0/PPIFS1*	I/O	GPIO/*SPORT0 Tx Frame Sync/RSI Data 3/Timer0/PPI Frame Sync1*	C
PG7/*DT0PRI/RSI_CMD/TMR1/PPIFS2*	I/O	GPIO/*SPORT0 Tx Primary Data/RSI Command/Timer 1/PPI Frame Sync2*	C
PG8/*TSCLK0/RSI_CLK/TMR6/TACI6*	I/O	GPIO/*SPORT0 Tx Clock/RSI Clock/Timer 6/Timer6 Alternate Capture Input*	D
PG9/*DT0SEC/UART0TX/TMR4*	I/O	GPIO/*SPORT0 Secondary Tx Data/UART0 Transmit/Timer 4*	C
PG10/*DR0SEC/UART0RX/TACI4*	I/O	GPIO/*SPORT0 Secondary Rx Data/UART0 Receive/Timer4 Alternate Capture Input*	C
PG11/*$\overline{\text{SPI0SS}}$/$\overline{\text{AMS2}}$/$\overline{\text{SPI1SEL5}}$/TACLK2*	I/O	GPIO/*SPI0 Slave Device Select/Asynchronous Memory Bank Select 2/SPI1 Slave Select 5/Timer2 Alternate CLK*	C
PG12/*SPI0SCK/PPICLK/TMRCLK/PTP_PPS*	I/O	GPIO/*SPI0 Clock/PPI Clock/External Timer Reference/PTP Pulse Per Second Out*	D
PG13/*SPI0MISO*[4]*/TMR0/PPIFS1/ PTP_CLKOUT*	I/O	GPIO/*SPI0 Master In Slave Out/Timer0/PPI Frame Sync1/PTP Clock Out*	C
PG14/*SPI0MOSI/TMR1/PPIFS2/$\overline{\text{PWM TRIP}}$ /PTP_AUXIN*	I/O	GPIO/*SPI0 Master Out Slave In/Timer 1/PPI Frame Sync2/PWM Trip/PTP Auxiliary Snapshot Trigger Input*	C
PG15/*$\overline{\text{SPI0SEL2}}$/PPIFS3/$\overline{\text{AMS3}}$*	I/O	GPIO/*SPI0 Slave Select 2/PPI Frame Sync3/Asynchronous Memory Bank Select 3*	C
Port H: GPIO and Multiplexed Peripherals			
PH0/*DR1PRI/$\overline{\text{SPI1SS}}$/RSI_DATA4*	I/O	GPIO/*SPORT1 Primary Rx Data/SPI1 Device Select/RSI Data 4*	C
PH1/*RFS1/SPI1MISO/RSI_DATA5*	I/O	GPIO/*SPORT1 Rx Frame Sync/SPI1 Master In Slave Out/RSI Data 5*	C
PH2/*RSCLK1/SPI1SCK/RSI DATA6*	I/O	GPIO/*SPORT1 Rx Clock/SPI1 Clock/RSI Data 6*	D
PH3/*DT1PRI/SPI1MOSI/RSI DATA7*	I/O	GPIO/*SPORT1 Primary Tx Data/SPI1 Master Out Slave In/RSI Data 7*	C
PH4/*TFS1/AOE/$\overline{\text{SPI0SEL3}}$/CUD*	I/O	GPIO/*SPORT1 Tx Frame Sync/Asynchronous Memory Output Enable/SPI0 Slave Select 3/Counter Up Direction*	C
PH5/*TSCLK1/ARDY/PTP_EXT_CLKIN/CDG*	I/O	GPIO/*SPORT1 Tx Clock/Asynchronous Memory Hardware Ready Control/ External Clock for PTP TSYNC/Counter Down Gate*	D
PH6/*DT1SEC/UART1TX/$\overline{\text{SPI1SEL1}}$/CZM*	I/O	GPIO/*SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker*	C
PH7/*DR1SEC/UART1RX/TMR7/TACI2*	I/O	GPIO/*SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input*	C

Table 10. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
Port J			
PJ0:SCL	I/O 5V	TWI Serial Clock (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	E
PJ1:SDA	I/O 5V	TWI Serial Data (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	E
Real Time Clock			
RTXI	I	RTC Crystal Input (This ball should be pulled low when not used.)	
RTXO	O	RTC Crystal Output	
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This signal should be pulled low if the JTAG port is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
Clock			
CLKIN	I	Clock/Crystal Input	
XTAL	O	Crystal Output	
CLKBUF	O	Buffered XTAL Output	C
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Non-maskable Interrupt (This signal should be pulled high when not used.)	
BMODE2-0	I	Boot Mode Strap 2-0	
Voltage Regulation Interface			
$\overline{\text{PG}}$	I	Power Good (This signal should be pulled low when not used.)	
EXT_WAKE	O	Wake up Indication	F
Power Supplies		**ALL SUPPLIES MUST BE POWERED** See Operating Conditions on Page 24.	
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
V_{DDRTC}	P	Real Time Clock Power Supply	
$V_{DDFLASH}$	P	Internal SPI Flash Power Supply	
V_{DDMEM}	P	MEM Power Supply	
V_{PPOTP}	P	OTP Programming Voltage	
V_{DDOTP}	P	OTP Power Supply	
V_{SS}	G	Ground for All Supplies	

[1] See Output Drive Currents on Page 54 for more information about each driver type.
[2] When driven low, the PF15 signal can be used to wake up the processor from the hibernate state, either in normal GPIO mode or in Ethernet mode as $\overline{\text{PHYINT}}$. If the pin/ball is used for wake up, enable the feature with the PHYWE bit in the VR_CTL register, and pull-up the signal with a resistor.
[3] Boot host wait is a GPIO signal toggled by the boot kernel. The mandatory external pull-up/pull-down resistor defines the signal polarity.
[4] A pull-up resistor is required for the boot from external SPI EEPROM or flash (BMODE = 0x3).

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]		tbd	tbd	tbd	V
V_{DDEXT}[2]	External Supply Voltage[3]		1.70	1.8, 2.5 or 3.3	3.6	V
V_{DDRTC}[4]	RTC Power Supply Voltage		2.25		3.6	V
V_{DDMEM}[5]	MEM Supply Voltage		1.70	1.8, 2.5 or 3.3	3.6	V
$V_{DDFLASH}$[4]	Internal SPI Flash Supply Voltage		1.7	1.8	1.9	V
V_{DDOTP}	OTP Supply Voltage		2.25	2.5	2.75	V
V_{PPOTP}	OTP Programming Voltage					
	For Reads[2]		2.25	2.5	2.75	V
	For Writes[6]		6.9	7.0	7.1	V
V_{IH}	High Level Input Voltage[7, 8]	V_{DDEXT}/V_{DDMEM} = 1.90 V	1.1		3.6	V
V_{IH}	High Level Input Voltage[7, 8]	V_{DDEXT}/V_{DDMEM} = 2.75 V	1.7		3.6	V
V_{IH}	High Level Input Voltage[7, 8]	V_{DDEXT}/V_{DDMEM} = 3.6 V	2.0		3.6	V
V_{IHTWI}	High Level Input Voltage	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 x V_{BUSTWI}		V_{BUSTWI}[9]	V
V_{IL}	Low Level Input Voltage[7, 8]	V_{DDEXT}/V_{DDMEM} = 1.7 V	–0.3		0.6	V
V_{IL}	Low Level Input Voltage[7, 8]	V_{DDEXT}/V_{DDMEM} = 2.25 V	–0.3		0.7	V
V_{IL}	Low Level Input Voltage[7, 8]	V_{DDEXT}/V_{DDMEM} = 3.0 V	–0.3		0.8	V
V_{ILTWI}	Low Level Input Voltage	V_{DDEXT} = minimum	–0.3		0.3 x V_{BUSTWI}[10]	V
T_J	Junction Temperature	168-Ball CSP_BGA @ $T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C
T_J	Junction Temperature	168-Ball CSP_BGA @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	176-Lead LQFP @ $T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C
T_J	Junction Temperature	176-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] The expected nominal value is 1.4V ± 5% and initial customer designs should design with a programmable regulator that can be adjusted from 0.95V to 1.5V in 50mV steps.

[2] Must remain powered (even if the associated function is not used).

[3] V_{DDEXT} is the supply to the GPIO.

[4] If not used, power with V_{DDEXT}.

[5] Pins/balls that use V_{DDMEM} are DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, SA10, $\overline{SWE}$, $\overline{SCAS}$, CLKOUT, $\overline{SRAS}$, $\overline{SMS}$, SCKE. These pins/balls are not tolerant to voltages higher than V_{DDMEM}. When using any of the asynchronous memory signals $\overline{AMS3–2}$, ARDY, or $\overline{AOE}$ V_{DDMEM} and V_{DDEXT} must be shorted externally because these signals are multiplexed with GPIO.

[6] The V_{PPOTP} voltage for writes must only be applied when programming OTP memory. There is a finite amount of cumulative time that this voltage may be applied (dependent on voltage and junction temperature) over the lifetime of the part. Please see Table 23 on Page 29 for details.

[7] Bidirectional pins/balls (PF15–0, PG15–0, PH7–0) and input pins/balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF51x are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Parameter value applies to all input and bidirectional pins/balls except SDA and SCL.

[9] The V_{IHTWI} min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See V_{BUSTWI} min and max values in Table 12.

[10] SDA and SCL are pulled up to V_{BUSTWI}. See Table 11.

Table 11 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

Table 11. TWI_DT Field Selections and V_{DDEXT}/V_{BUSTWI}

TWI_DT	V_{DDEXT} Nominal	V_{BUSTWI} Minimum	V_{BUSTWI} Nominal	V_{BUSTWI} Maximum	Unit
000 (default)	3.3	2.97	3.3	3.63	V
001	1.8	1.7	1.8	1.98	V
010	2.5	2.97	3.3	3.63	V
011	1.8	2.97	3.3	3.63	V
100	3.3	4.5	5	5.5	V
101	1.8	2.25	2.5	2.75	V
110	2.5	2.25	2.5	2.75	V
111 (reserved)	–	–	–	–	–

Table 12 describes the timing requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 14 describes phase-locked loop operating conditions.

Table 12. Core Clock (CCLK) Requirements—400 MHz Speed Grade[1]

Parameter		Min	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} =TBD V Minimum)		400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} =TBD V Minimum)		TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = TBD V Minimum)		TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = TBD V Minimum)		TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = TBD V Minimum)		TBD	MHz

[1] The speed grade of a given part is printed on the chip's package as shown in Figure 7 on Page 30 and can also be seen on the Ordering Guide on Page 68. It stands for the maximum allowed CCLK frequency at V_{DDINT} = TBD V and the maximum allowed VCO frequency at any supply voltage.

Table 13. Core Clock (CCLK) Requirements—300 MHz Speed Grade[1]

Parameter		Min	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} =TBD V Minimum)		300	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} =TBD V Minimum)		TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = TBD V Minimum)		TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = TBD V Minimum)		TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = TBD V Minimum)		TBD	MHz

[1] The speed grade of a given part is printed on the chip's package as shown in Figure 7 on Page 30 and can also be seen on the Ordering Guide on Page 68. It stands for the maximum allowed CCLK frequency at V_{DDINT} = TBD V and the maximum allowed VCO frequency at any supply voltage.

Table 14. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	70	Speed Grade[1]	MHz

[1] The speed grade of a given part is printed on the chip's package as shown in Figure 7 on Page 30 and can also be seen on the Ordering Guide on Page 68. It stands for the maximum allowed CCLK frequency at V_{DDINT} = TBD V and the maximum allowed VCO frequency at any supply voltage.

Table 15. Maximum SCLK Conditions

Parameter[1]		V_{DDEXT} = 3.3 V, 2.5 V, or 1.8 V	Unit
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ TBD V)	80	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < TBD V)	TBD	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 32 on Page 35.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 2.25 V, I_{OH} = –0.5 mA	2.0			V
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7/2.25/3.0 V, I_{OL} = 2.0 mA			0.4	V
V_{OLTWI}	Low Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7/2.25/3.0 V, I_{OL} = 2.0 mA			TBD	V
I_{IH}[1]	High Level Input Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{IL}[1]	Low Level Input Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10.0	µA
I_{IHP}[2]	High Level Input Current JTAG	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			75.0	µA
I_{OZH}[3]	Three-State Leakage Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{OZHTWI}[4]	Three-State Leakage Current	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10.0	µA
I_{OZL}[3]	Three-State Leakage Current	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10.0	µA
C_{IN}[5, 6]	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		TBD	TBD	pF
C_{INTWI}[4, 6]	Input Capacitance	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			TBD	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.223 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		1.85		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.223 V, f_{SCLK} = 25 MHz, T_J = 25°C		2.1		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.223 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.44		18		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.223 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		68		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.4 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		99		mA
$I_{DDHIBERNATE}$[8]	Hibernate State Current	V_{DDEXT}=V_{DDMEM}=V_{DDRTC} = 3.30 V V_{DDOTP}=V_{PPOTP}=2.5 V, T_J = 25°C, CLKIN = 0 MHz @ T_J = 25°C		40		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		TBD		µA
$I_{DDSLEEP}$[8, 9]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			Table 19 + (TBD × V_{DDINT} × f_{SCLK})	mA[10]

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDDEEPSLEEP}$[8, 10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 19	mA
I_{DDINT}[10, 11]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 19 + (Table 20 × ASF) + (TBD × V_{DDINT} × f_{SCLK})	mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		1		mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		25		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		0		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		0		mA

[1] Applies to input balls.
[2] Applies to JTAG input balls (TCK, TDI, TMS, $\overline{TRST}$).
[3] Applies to three-statable balls.
[4] Applies to bidirectional balls SCL and SDA.
[5] Applies to all signal balls, except SCL and SDA.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Includes current on V_{DDEXT}, V_{DDUSB}, V_{DDMEM}, V_{DDOTP}, and V_{PPOTP} supplies. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz.
[11] See Table 18 for the list of I_{DDINT} power vectors covered.

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Table 16. Reliability Characteristics

Parameter		Min Specification	Units	Test Method
N_{END}	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}	Data Retention	100	Years	JEDEC Standard A103

Table 17. AC Operating Characteristics

Parameter		Min	Max	Units
f_{CLK}[1]	Serial Clock Frequency		25	MHz
T_{SE}	Sector-Erase		75	ms
T_{BE}	Block-Erase		75	ms
T_{SCE}	Chip-Erase		150	ms
T_{BP}[2]	Byte-Program		60	µs

[1] Maximum clock frequency for Read instruction, 0x03, is 20 MHz.
[2] AAI-Word Program TBP maximum specification is also at 60 µs maximum time.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 26 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 19), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 20).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 18).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 20 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 18. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.85
I_{DD-NOP}	0.70
$I_{DD-IDLE}$	0.41

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF51x processors.

Table 19. Static Current — $I_{DD-DEEPSLEEP}$ (mA)

	Voltage (V_{DDINT})[1]							
T_J (°C)[1]	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
–40	1.0	1.0	1.1	1.1	1.2	1.3	1.7	1.9
–20	1.1	1.2	1.3	1.4	1.6	1.7	1.9	2.0
0	1.3	1.4	1.6	1.8	2.0	2.2	2.3	2.5
25	1.9	2.1	2.3	2.5	2.8	3.1	3.3	3.7
40	2.6	2.8	3.0	3.3	3.7	4.0	4.4	4.9
55	3.5	3.8	4.3	4.6	5.0	5.5	6.1	6.7
70	5.0	5.4	6.0	6.4	7.0	7.7	8.4	9.2
85	7.1	7.7	8.3	9.1	9.9	10.8	11.8	12.8
100	10.0	10.8	11.7	12.7	13.7	15.0	16.1	17.5
105	11.1	12.1	13.1	14.2	15.3	16.6	18.0	19.4

[1] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 24.

Table 20. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

f_{CCLK}	Voltage (V_{DDINT})[2]							
(MHz)[2]	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.40 V	1.45 V	1.50 V
400	N/A	N/A	N/A	93.4	97.7	102.1	106.5	111.0
350	N/A	N/A	N/A	82.4	86.2	90.1	94.0	98.0
300	N/A	64.8	68.1	71.4	74.7	78.1	81.5	85.0
250	52.1	54.8	57.5	60.4	63.2	66.1	69.0	71.9
200	42.5	44.7	47.0	49.4	51.7	54.1	56.5	58.9
150	32.9	34.7	36.5	38.4	40.2	42.1	44.0	45.9
100	23.4	24.7	26.0	27.4	28.7	30.1	31.5	33.0

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 26.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 24.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 21 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 21. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DDINT})	TBD V to +TBD V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.6 V
Input Voltage[1, 3]	–0.5 V to +5.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT}+0.5 V
Load Capacitance[4]	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Underbias	+110ºC

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 22.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 Volts.
[3] Applies to signals SCL, SDA.
[4] For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19–1, DATA15–0, $\overline{ABE1–0}$/SDQM1–0, CLKOUT, SCKE, SA10, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, and $\overline{SMS}$.

Table 22. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)	V_{IN} Max (V)	Maximum Duty Cycle
TBD	TBD	100%
TBD	TBD	40%
TBD	TBD	25%
TBD	TBD	15%
TBD	TBD	10%

[1] Applies to all signal pins/balls with the exception of CLKIN, XTAL, VROUT.

When programming OTP memory on the ADSP-BF51x processor, the V_{PPOTP} pin/ball must be set to the write value specified in the Operating Conditions on Page 24. There is a finite amount of cumulative time that the write voltage may be applied (dependent on voltage and junction temperature) to V_{PPOTP} over the lifetime of the part. Therefore, maximum OTP memory programming time for the processor is shown in Table 23.

Table 23. Maximum OTP Memory Programming Time

	Temperature		
VPPOTP Voltage (V)	25°C	85°C	110°C
6.9	TBD sec	TBD sec	TBD sec
7.0	2400 sec	TBD sec	TBD sec
7.1	1000 sec	TBD sec	TBD sec

The Absolute Maximum Ratings table specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PH4, PH3, PH2, PH1, and PH0 from group 1 in the Total Current Pin Groups–VDDEXT Groups table, each were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. For a list of all groups and their pins, see Table 24 and Table 25. Note that the V_{OH} and V_{OL} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 24. Total Current Pin Groups–V_{DDEXT} Groups

Group	Pins in Group
1	PF9, PF8, PF7, PF6, PF5, PF4, PF3, PF2
2	PF1, PF0, PG15, PG14, PG13, PG12, PG11, PG10
3	PG9, PG8, PG7, PG6, PG5, PG4, PG3, PG2, BMODE0, BMODE1, BMODE2
4	PG1, PG0, TDO, $\overline{EMU}$, TDI, TCK, $\overline{TRST}$, TMS
5	$\overline{RESET}$, $\overline{NMI}$, CLKBUF
6	PH7, PH6, PH5, PH4, PH3, PH2, PH1, PH0
7	PF15, PF14, PF13, PF12, PF11, SDA, SCL, PF10

Table 25. Total Current Pin Groups–V_{DDMEM} Groups

Group	Pins in Group
1	DATA15, DATA14, DATA13, DATA12, DATA11, DATA10
2	DATA9, DATA8, DATA7, DATA6, DATA5, DATA4
3	DATA3, DATA2, DATA1, DATA0, ADDR19, ADDR18
4	ADDR17, ADDR16, ADDR15, ADDR14, ADDR13
5	ADDR12, ADDR11, ADDR10, ADDR9, ADDR8, ADDR7
6	ADDR6, ADDR5, ADDR4, ADDR3, ADDR2, ADDR1
7	$\overline{ABE1}$, $\overline{ABE0}$, SA10, $\overline{SWE}$, $\overline{SCAS}$, $\overline{SRAS}$
8	$\overline{SMS}$, SCKE, $\overline{AMS1}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS0}$, CLKOUT

PACKAGE INFORMATION

The information presented in Figure 7 and Table 26 provides details about the package branding for the processor. For a complete listing of product availability, see Ordering Guide on Page 68.

Figure 7. Product Information on Package

Table 26. Package Brand Information

Brand Key	Field Description
ADSP-BF51x	Product Name
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.v	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designator
yyww	Date Code

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 27 and Figure 8 describe clock and reset operations. Per Absolute Maximum Ratings on Page 29, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of 400 MHz/100 MHz.

Table 27. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	CLKIN Frequency[1, 2, 3, 4]	12	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
Switching Characteristic				
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 12 on Page 25 through Table 14 on Page 25.
[3] The t_{CKIN} period (see Figure 8) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz for commercial/industrial models and 28 MHz for automotive models.
[5] Applies after power-up sequence is complete. See Table 28 and Figure 9 for power-up reset timing.

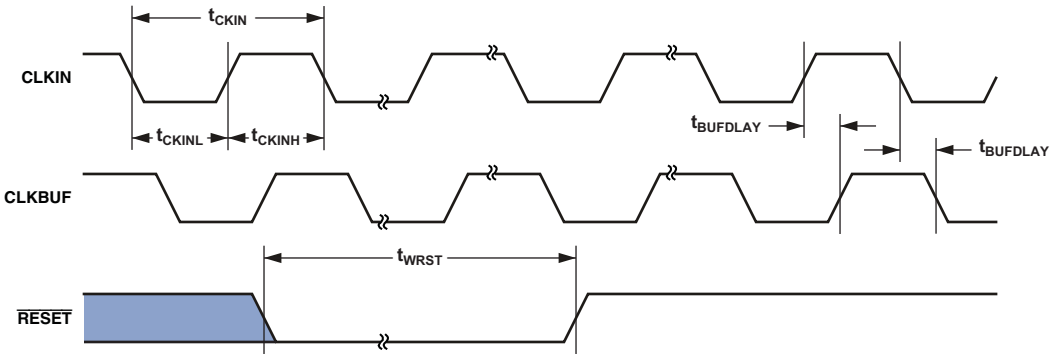


Figure 8. Clock and Reset Timing

Table 28. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, V_{DDMEM}, V_{DDOTP}, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		µs

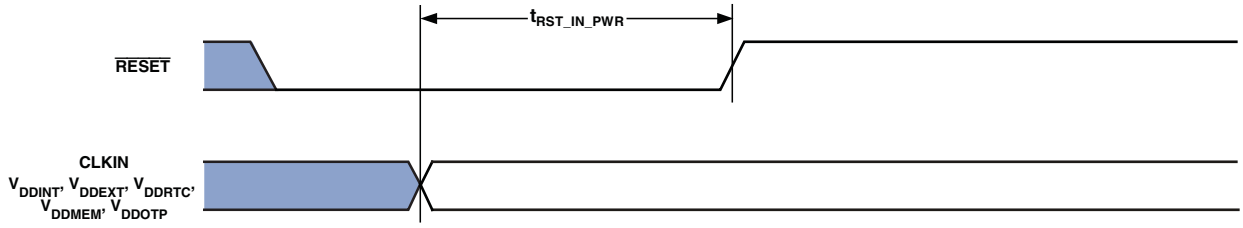


Figure 9. Power-Up Reset Timing

Flash Reset Timing

Driving the $\overline{\text{RESET}}$ pin low resets the Flash device. Driving the $\overline{\text{RESET}}$ pin high puts the device in normal operating mode. The SO pin is in high impedance state while the device is in reset. A successful reset will reset the status register to its power-up state. See Table 29 for default power-up modes. A device reset during an active Program or Erase operation aborts the operation and data of the targeted address range may be corrupted or lost due to the aborted erase or program operation. The device exits AAI Programming Mode in progress and places the SO pin in high impedance state.

Table 29. RESET Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RECR}	Reset Recovery from Read		100	ns
t_{RECP}	Reset Recovery from Program		10	µs
f_{RECE}	Reset Recovery from Erase		1	ms

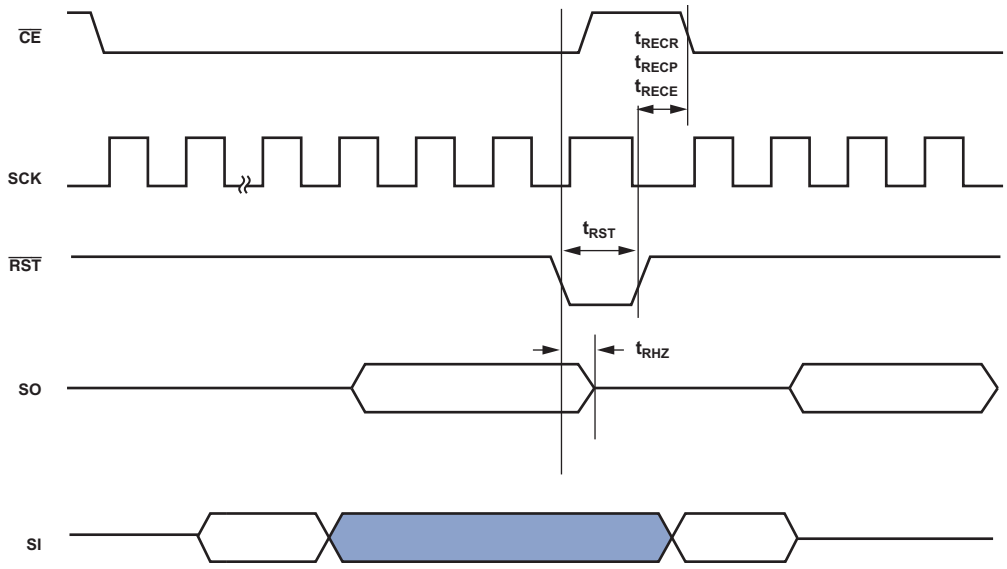


Figure 10. Flash Reset Timing

Asynchronous Memory Read Cycle Timing

Table 30. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins/balls include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

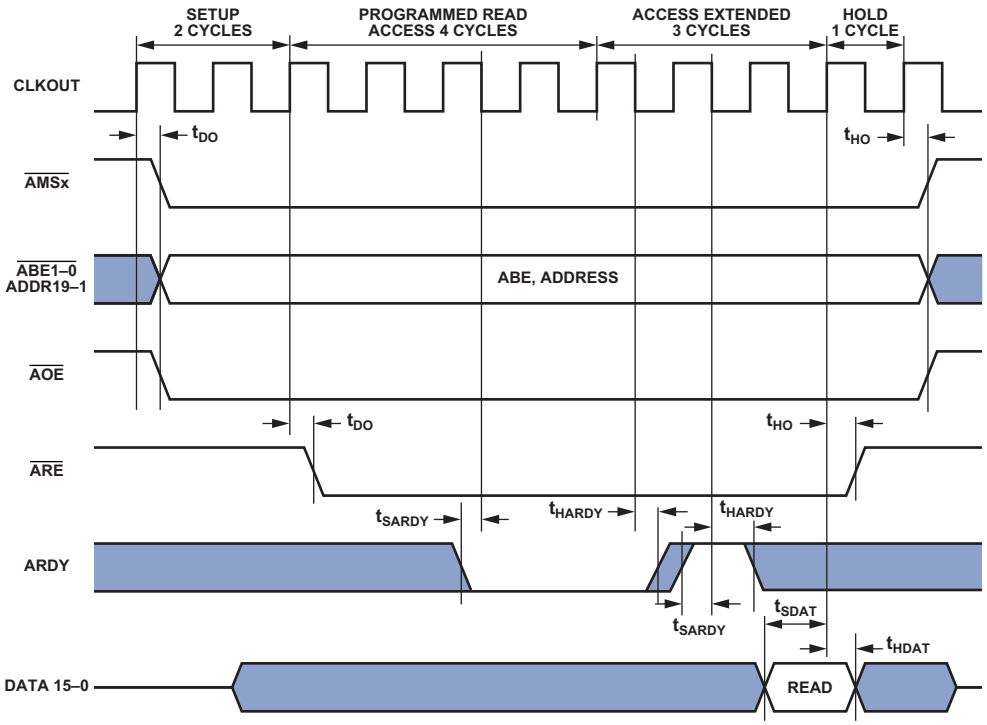


Figure 11. Asynchronous Memory Read Cycle Timing

Asynchronous Memory Write Cycle Timing

Table 31. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins/balls include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

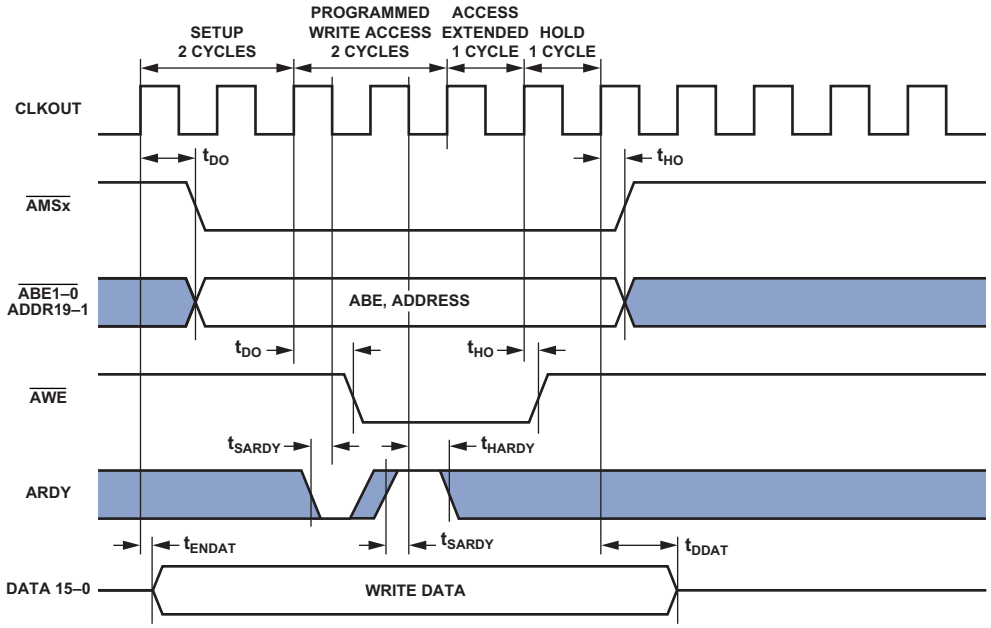


Figure 12. Asynchronous Memory Write Cycle Timing

SDRAM Interface Timing

Table 32. SDRAM Interface Timing

Parameter		V_{DDMEM} = 1.8 V Min	V_{DDMEM} = 1.8 V Max	V_{DDMEM} = 2.5/3.3 V Min	V_{DDMEM} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	0.8		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	12.5		12.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		2.5		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		4.4		4.4	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		4.4		4.4	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		1.0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 15. Package type and reduced supply voltages affect the best-case value listed here.
[2] Command pins/balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

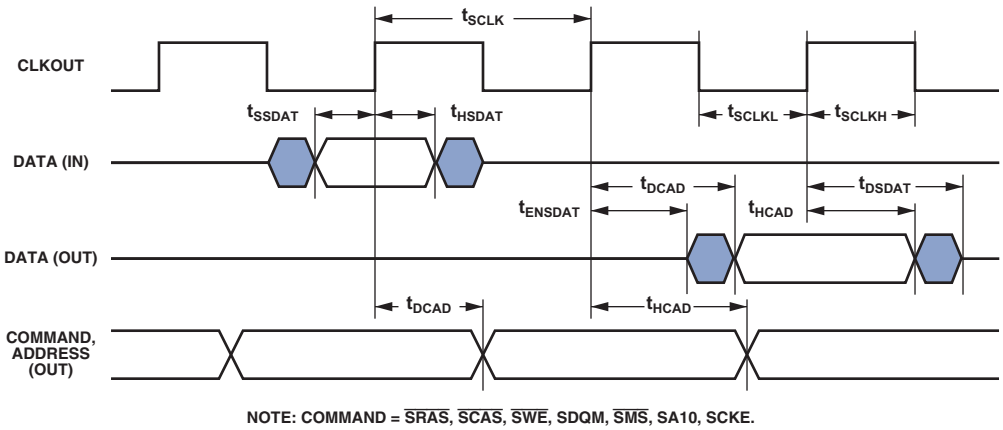


Figure 13. SDRAM Interface Timing

External DMA Request Timing

Table 33 and Figure 14 describe the External DMA Request operations.

Table 33. External DMA Request Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{DR}	DMARx Asserted to CLKOUT High Setup	6.0		ns
t_{DH}	CLKOUT High to DMARx Deasserted Hold Time	0.0		ns
$t_{DMARACT}$	DMARx Active Pulse Width	$1.0 \times t_{SCLK}$		ns
$t_{DMARINACT}$	DMARx Inactive Pulse Width	$1.75 \times t_{SCLK}$		ns

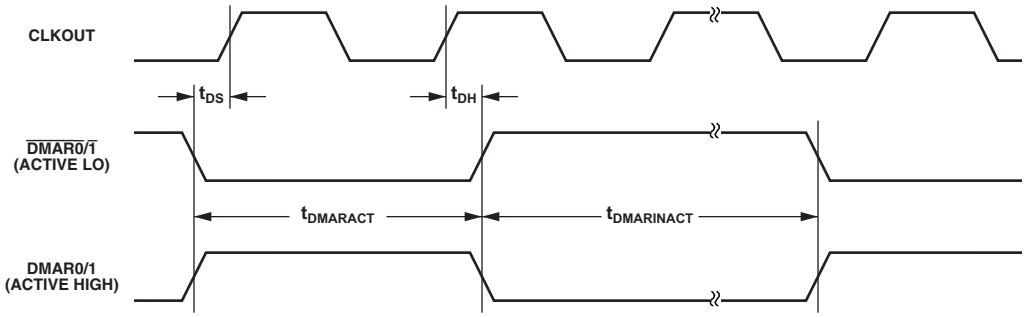


Figure 14. External DMA Request Timing

Parallel Peripheral Interface Timing

Table 34 and Figure 15 on Page 37, Figure 21 on Page 43, and Figure 22 on Page 44 describe parallel peripheral interface operations.

Table 34. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width[1]	6.4		ns
t_{PCLK}	PPI_CLK Period[1]	16.0		ns
Timing Requirements - GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		ns
Switching Characteristics - GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.8	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$

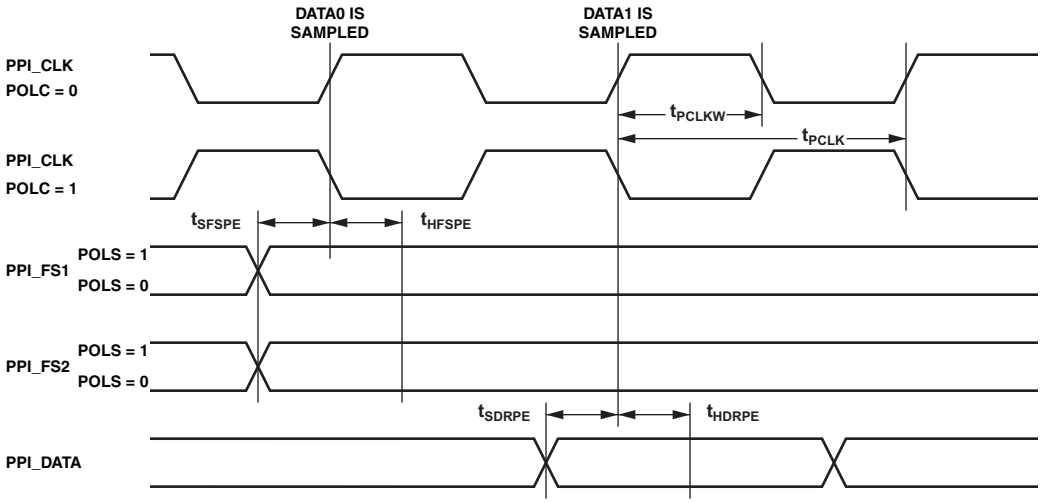


Figure 15. PPI GP Rx Mode with External Frame Sync Timing

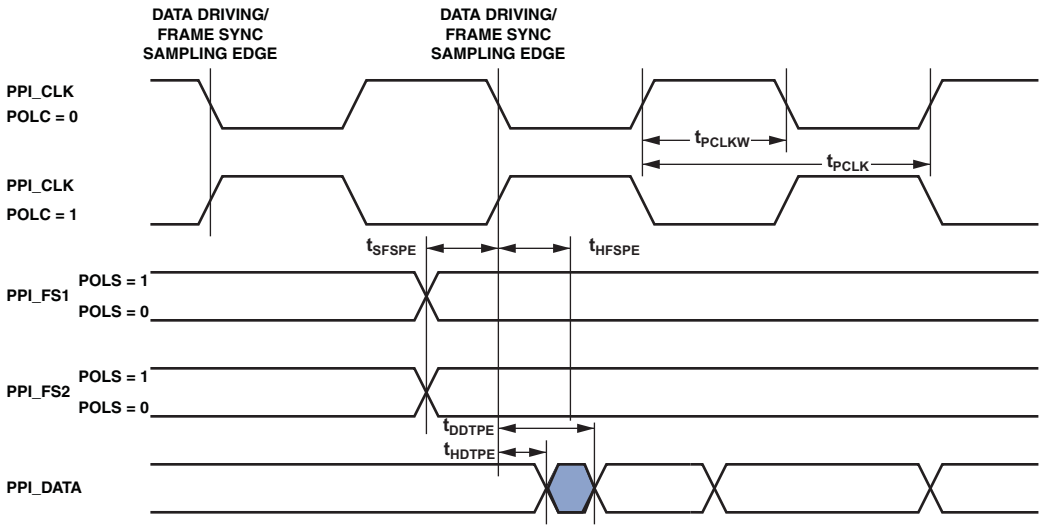


Figure 16. PPI GP Tx Mode with External Frame Sync Timing

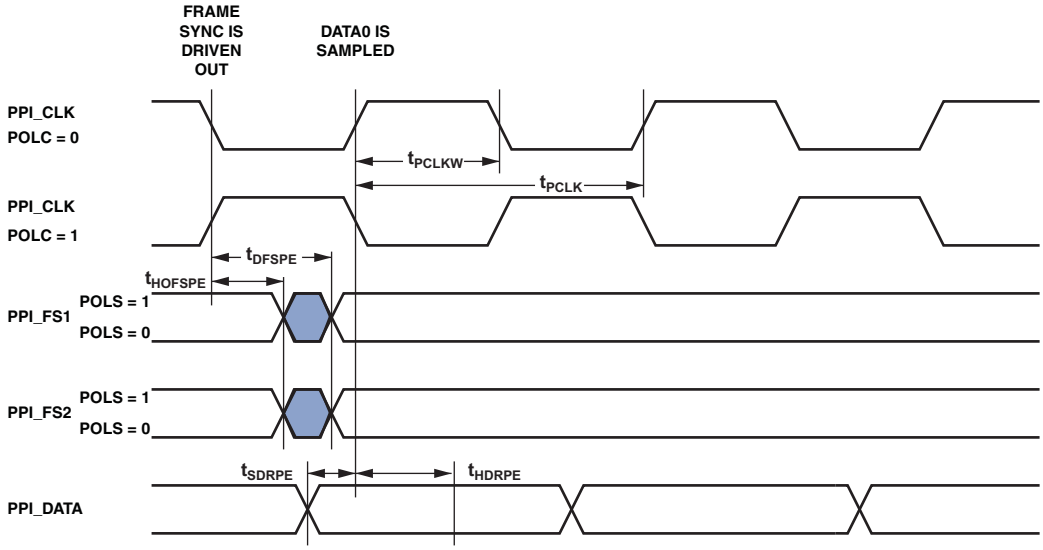


Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

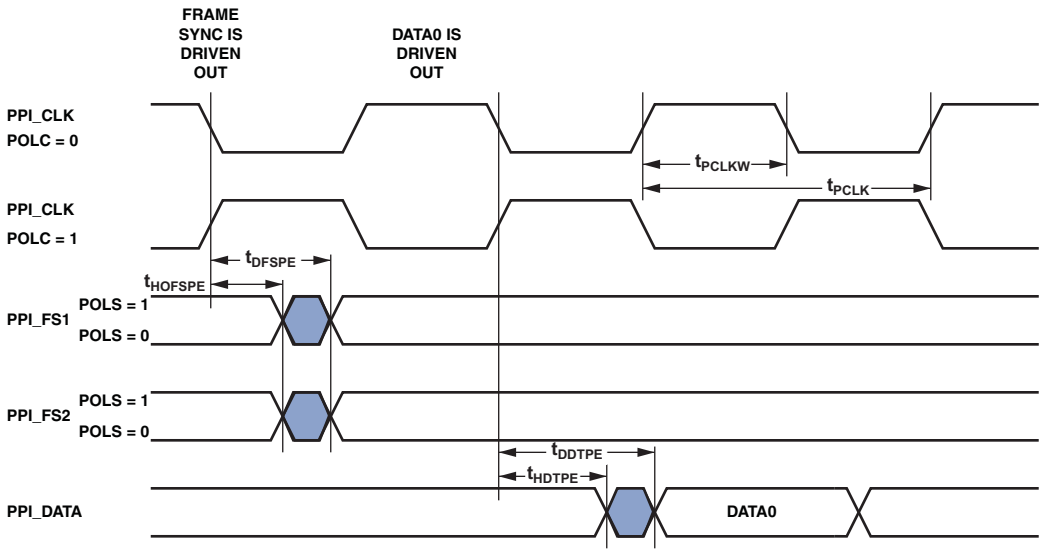


Figure 18. PPI GP Tx Mode with Internal Frame Sync Timing

RSI Controller Timing

Table 35 and Figure 19 describe RSI controller timing. Table 36 and Figure 20 describe RSI controller (high speed) timing.

Table 35. RSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	25	MHz
f_{OD}	Clock Frequency Identification Mode	100[2]	400	kHz
t_{WL}	Clock Low Time	15		ns
t_{WH}	Clock High Time	15		ns
t_{TLH}	Clock Rise Time		10	ns
t_{THL}	Clock Fall Time		10	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		14	ns
t_{ODLY}	Output Delay Time During Identification Mode		50	ns

[1] $t_{PP} = 1/f_{PP}$
[2] Specification can be 0 kHz, which means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

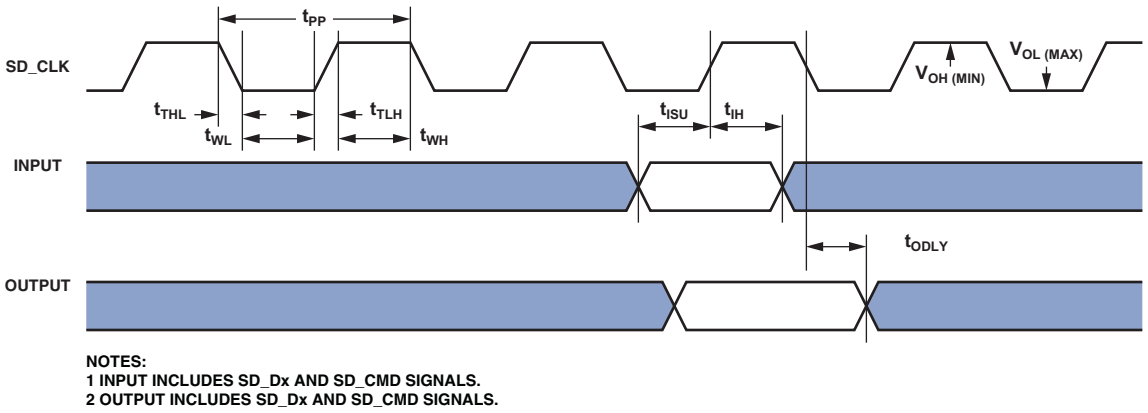


Figure 19. RSI Controller Timing

Table 36. RSI Controller Timing (High Speed Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	50	MHz
t_{WL}	Clock Low Time	9.5		ns
t_{WH}	Clock High Time	9.5		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		TBD	ns
t_{OH}	Output Hold Time	2.5		ns

[1] $t_{PP} = 1/f_{PP}$

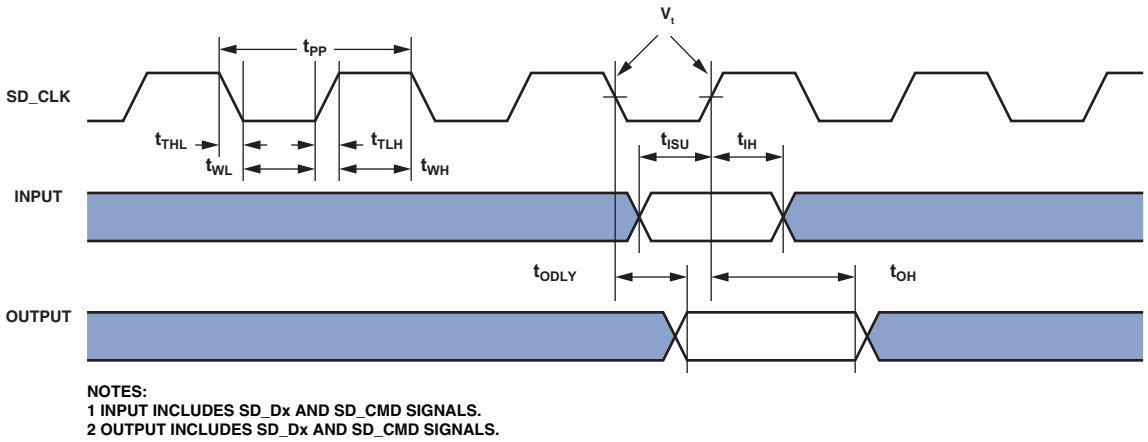


Figure 20. RSI Controller Timing (High-Speed Mode)

Serial Ports

Table 37 through Table 40 on Page 43 and Figure 21 on Page 43 through Figure 22 on Page 44 describe serial port operations.

Table 37. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.6		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	5.4		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	8.0		ns
Switching Characteristics				
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		12.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[1]		12.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[1]	0.0		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 38. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	11.3		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	11.3		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	–1.5		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	5.4		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	18.0		ns
Switching Characteristics				
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	–4.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[1]		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[1]	–1.8		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	5.4		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 39. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0.0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1]		3.0	ns

[1] Referenced to drive edge.

Table 40. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx with MCE = 1, MFD = 0[1, 2]		10.0	ns
$t_{DTENLFSE}$	Data Enable from Late FS or MCE = 1, MFD = 0[1, 2]	0.0		ns

[1] MCE = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

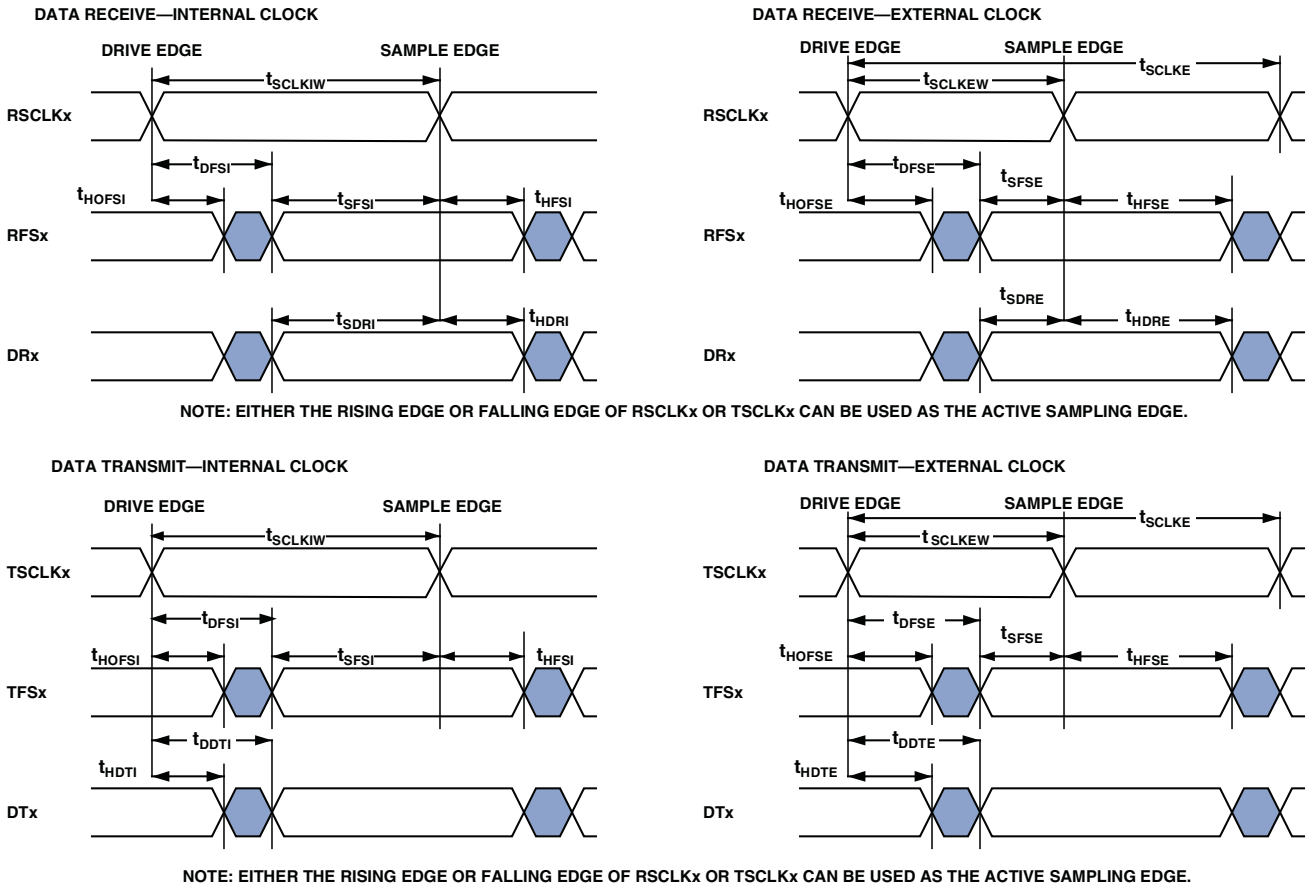


Figure 21. Serial Ports

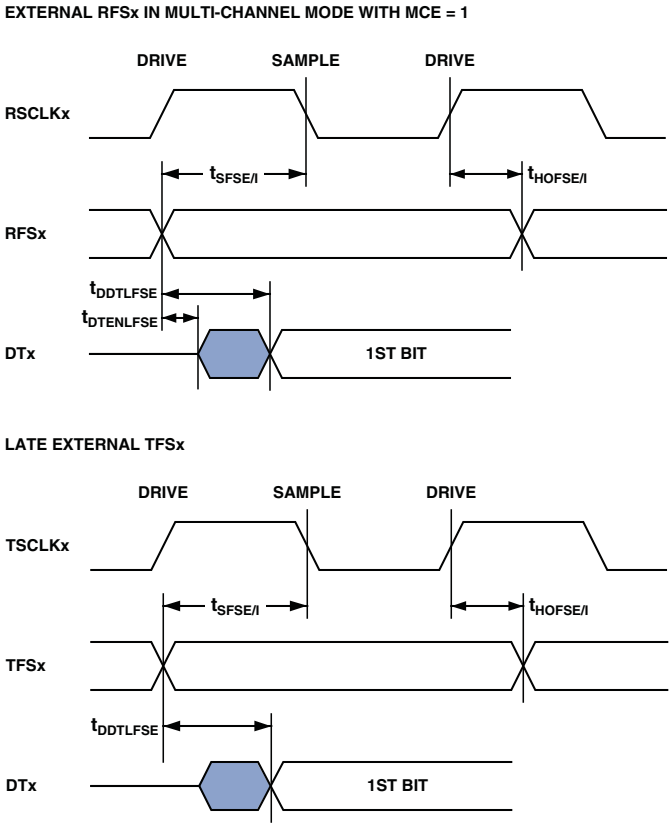


Figure 22. External Late Frame Sync

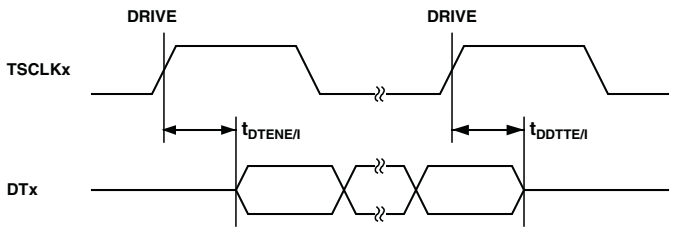


Figure 23. Enable and Three-State

Serial Peripheral Interface (SPI) Port—Master Timing

Table 41 and Figure 24 describe SPI port master operations.

Table 41. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	11.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPISELx}}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDSM}	Last SCK Edge to $\overline{\text{SPISELx}}$ High	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK}$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0	4.0	ns

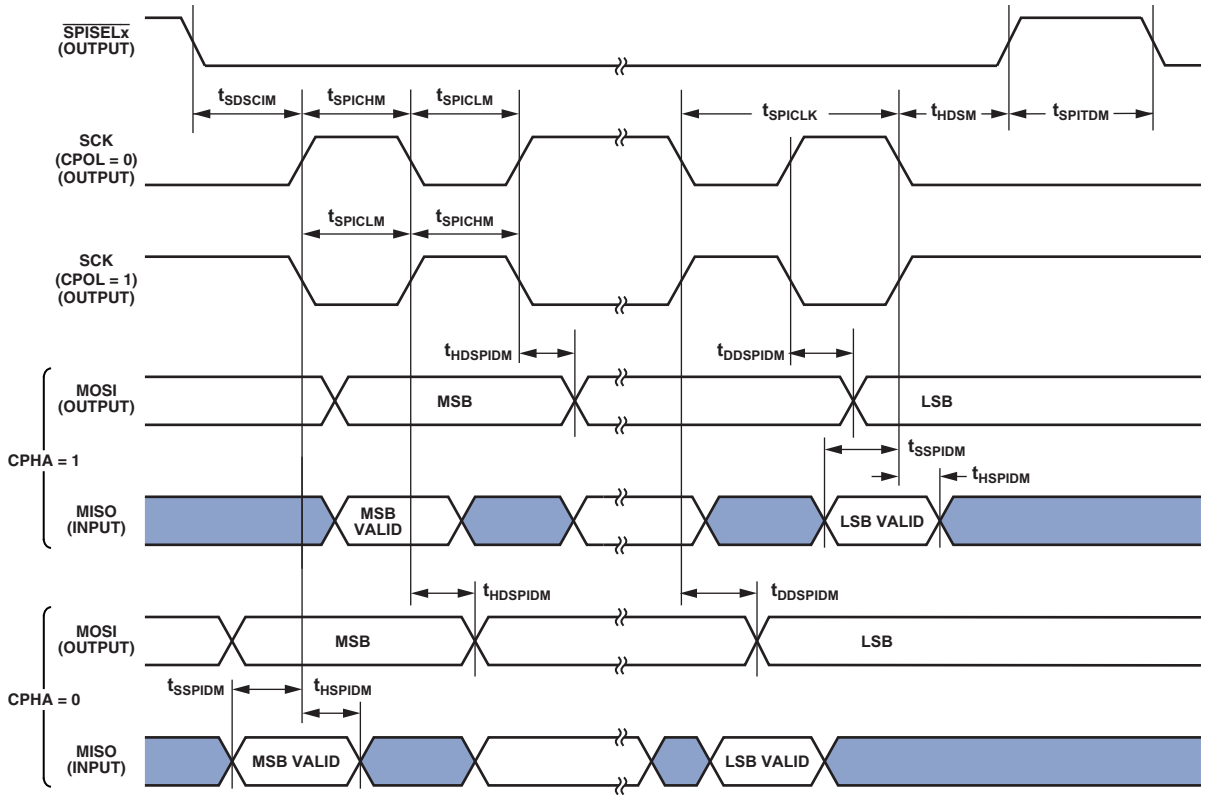


Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 42 and Figure 25 describe SPI port slave operations.

Table 42. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK}$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	9.0	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	9.0	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		ns

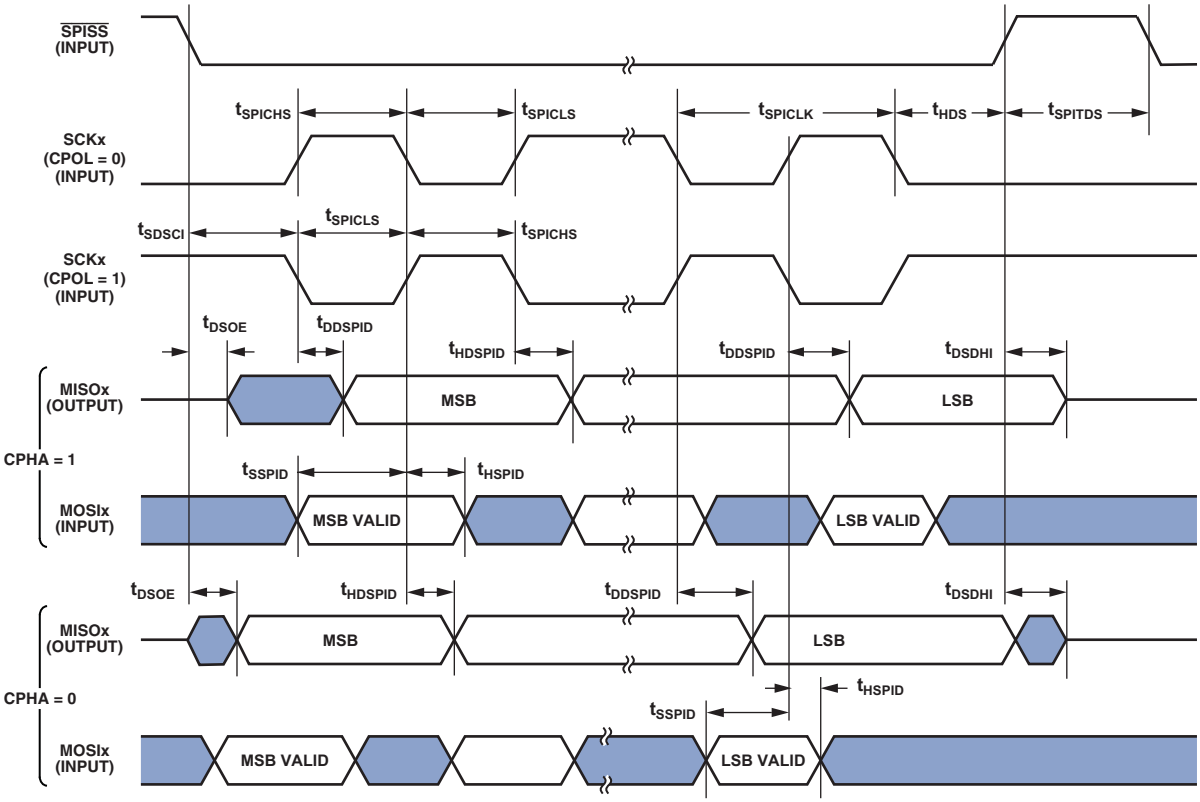


Figure 25. Serial Peripheral Interface (SPI) Port—Slave Timing

General-Purpose Port Timing

Table 43 and Figure 26 describe general-purpose port operations.

Table 43. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Signal Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristics				
t_{GPOD}	General-Purpose Port Signal Output Delay from CLKOUT Low	0	9.66	ns

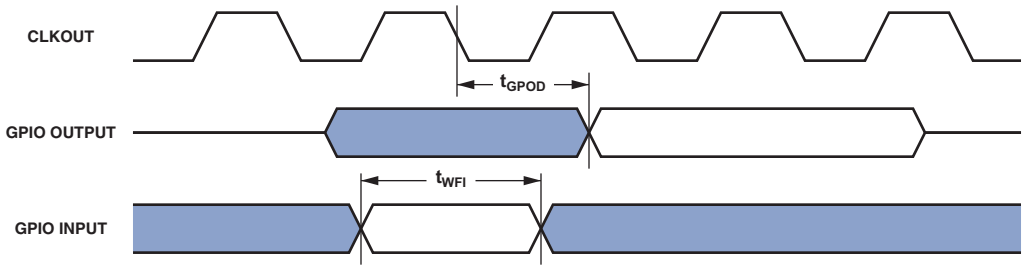


Figure 26. General-Purpose Port Timing

Timer Clock Timing

Table 44 and Figure 27 describe timer clock timing.

Table 44. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPICLK High		12.64	ns

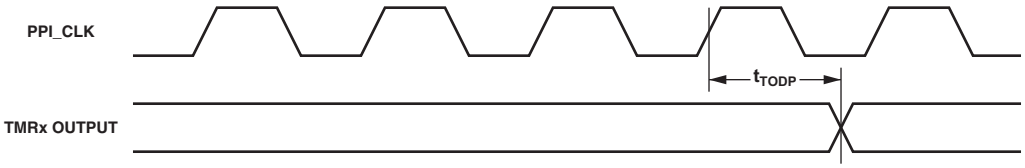


Figure 27. Timer Clock Timing

Timer Cycle Timing

Table 45 and Figure 28 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 45. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$1 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$1 \times t_{SCLK}$		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–2		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	$1 \times t_{SCLK}$	$(2^{32}–1)t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		8.1	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PF15 or PPI_CLK signals in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

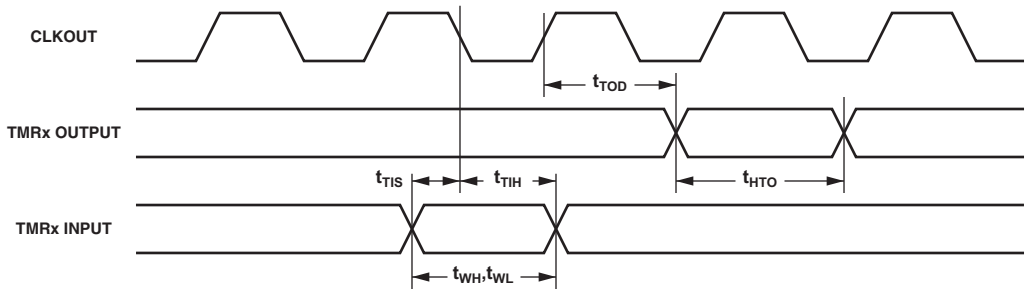


Figure 28. Timer Cycle Timing

Up/Down Counter/Rotary Encoder Timing

Table 46. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
t_{CIS}	Counter Input Setup Time Before CLKOUT Low[1]	4.0		4.0		ns
t_{CIH}	Counter Input Hold Time After CLKOUT Low1	4.0		4.0		ns

[1] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize counter inputs.

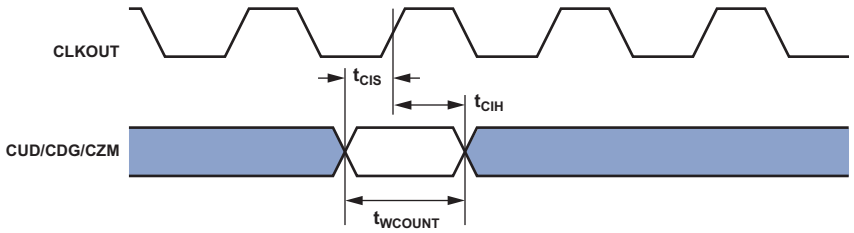


Figure 29. Up/Down Counter/Rotary Encoder Timing

10/100 Ethernet MAC Controller Timing

Table 47 through Table 52 and Figure 30 through Figure 35 describe the 10/100 Ethernet MAC Controller operations.

Table 47. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Parameter[1]		Min	Max	Unit
$t_{ERXCLKF}$	ERxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 MHz + 1% f_{SCLK} + 1%	ns
$t_{ERXCLKW}$	ERxCLK Width (t_{ERxCLK} = ERxCLK Period)	t_{ERxCLK} x 35%	t_{ERxCLK} x 65%	ns
$t_{ERXCLKIS}$	Rx Input Valid to ERxCLK Rising Edge (Data In Setup)	7.5		ns
$t_{ERXCLKIH}$	ERxCLK Rising Edge to Rx Input Invalid (Data In Hold)	7.5		ns

[1] MII inputs synchronous to ERxCLK are ERxD3–0, ERxDV, and ERxER.

Table 48. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

Parameter[1]		Min	Max	Unit
t_{ETF}	ETxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 MHz + 1% f_{SCLK} + 1%	ns
$t_{ETXCLKW}$	ETxCLK Width (t_{ETxCLK} = ETxCLK Period)	t_{ETxCLK} x 35%	t_{ETxCLK} x 65%	ns
$t_{ETXCLKOV}$	ETxCLK Rising Edge to Tx Output Valid (Data Out Valid)		20	ns
$t_{ETXCLKOH}$	ETxCLK Rising Edge to Tx Output Invalid (Data Out Hold)	0		ns

[1] MII outputs synchronous to ETxCLK are ETxD3–0.

Table 49. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Parameter[1]		Min	Max	Unit
$t_{EREFCLKF}$	REF_CLK Frequency (f_{SCLK} = SCLK Frequency)	None	50 MHz + 1% 2 x f_{SCLK} + 1%	ns
$t_{EREFCLKW}$	EREF_CLK Width ($t_{EREFCLK}$ = EREFCLK Period)	$t_{EREFCLK}$ x 35%	$t_{EREFCLK}$ x 65%	ns
$t_{EREFCLKIS}$	Rx Input Valid to RMII REF_CLK Rising Edge (Data In Setup)	4		ns
$t_{EREFCLKIH}$	RMII REF_CLK Rising Edge to Rx Input Invalid (Data In Hold)	2		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxD1–0, RMII CRS_DV, and ERxER.

Table 50. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
$t_{EREFCLKOV}$	RMII REF_CLK Rising Edge to Tx Output Valid (Data Out Valid)		8.1	ns
$t_{EREFCLKOH}$	RMII REF_CLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxD1–0.

Table 51. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter[1, 2]		Min	Max	Unit
t_{ECOLH}	COL Pulse Width High	t_{ETxCLK} x 1.5 t_{ERxCLK} x 1.5		ns
t_{ECOLL}	COL Pulse Width Low	t_{ETxCLK} x 1.5 t_{ERxCLK} x 1.5		ns
t_{ECRSH}	CRS Pulse Width High	t_{ETxCLK} x 1.5		ns
t_{ECRSL}	CRS Pulse Width Low	t_{ETxCLK} x 1.5		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

Table 52. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	11.5		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	11.5		ns
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid	25		ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

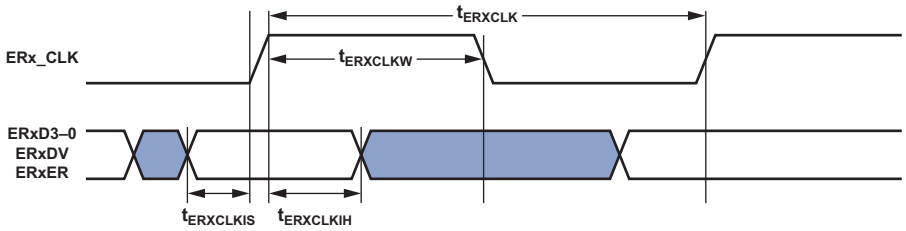


Figure 30. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

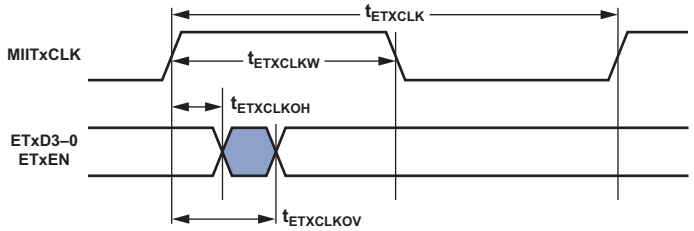


Figure 31. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

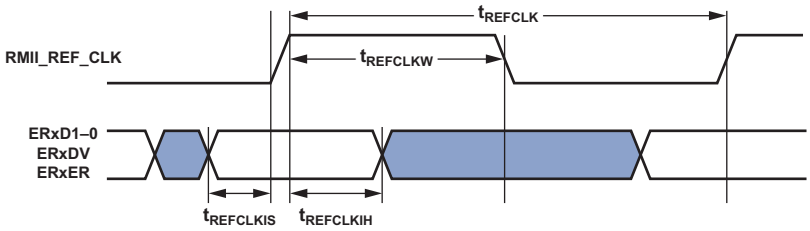


Figure 32. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

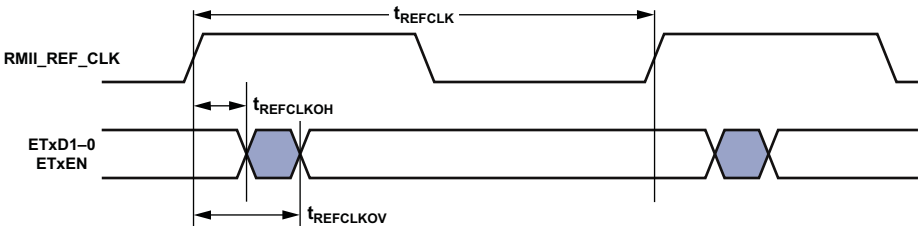


Figure 33. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

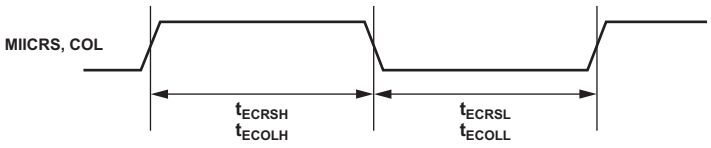


Figure 34. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

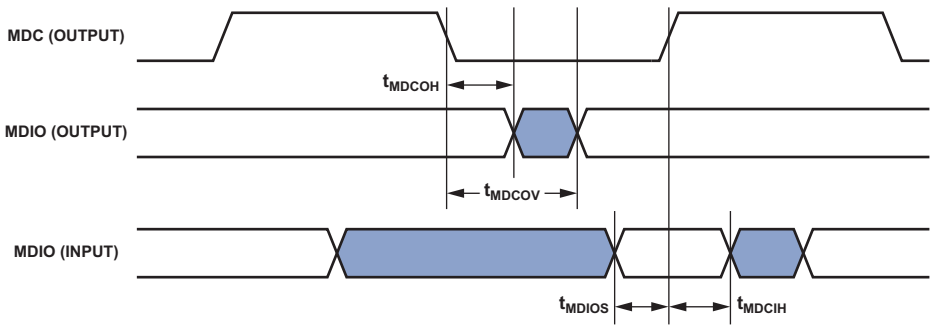


Figure 35. 10/100 Ethernet MAC Controller Timing: MII Station Management

JTAG Test And Emulation Port Timing

Table 53 and Figure 36 describe JTAG port operations.

Table 53. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	13	ns

[1] System Inputs = DATA15–0, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH7–0, MDIO, TCK, TD1, TMS, $\overline{TRST}$, $\overline{RESET}$, $\overline{NMI}$, BMODE2–0.

[2] 50 MHz Maximum

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS1–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, SCL, SDA, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH7–0, MDC, MDIO, TD0, $\overline{EMU}$.

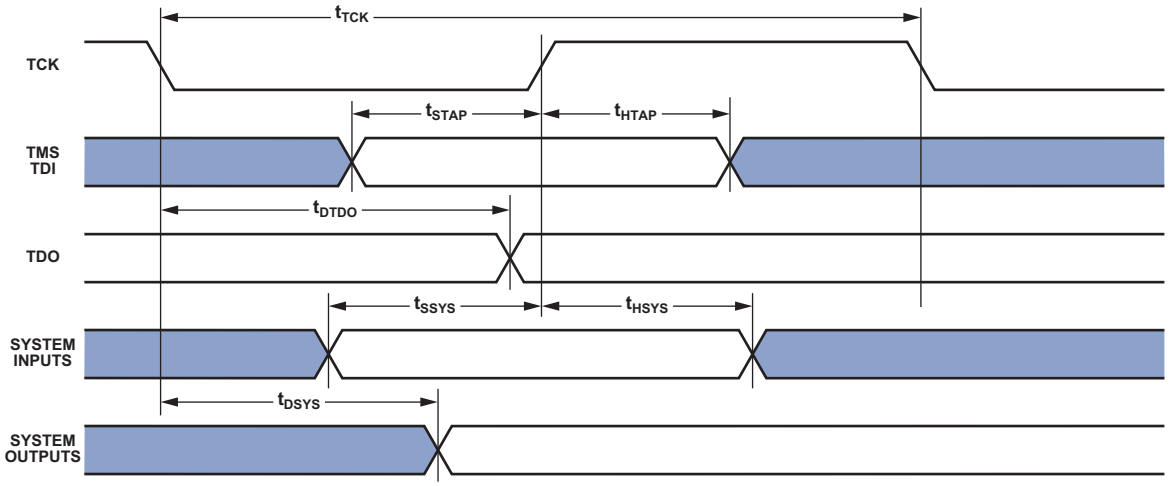


Figure 36. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 37 through Figure 51 show typical current-voltage characteristics for the output drivers of the ADSP-BF51xF processors.

The curves represent the current drive capability of the output drivers. See Table 10 on Page 21 for information about which driver type corresponds to a particular ball.

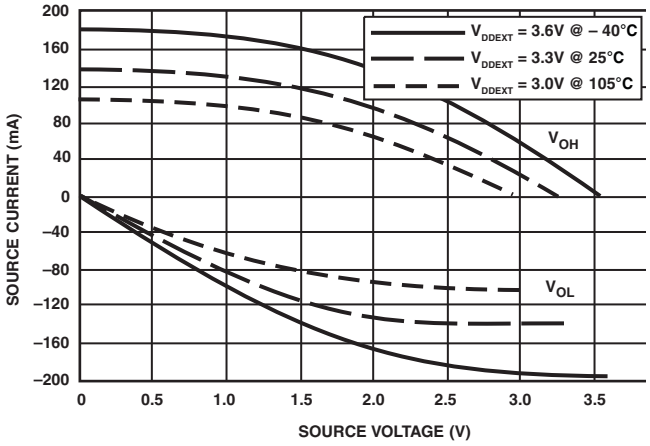


Figure 37. Driver Type A Current (3.3V V_{DDEXT}/V_{DDMEM})

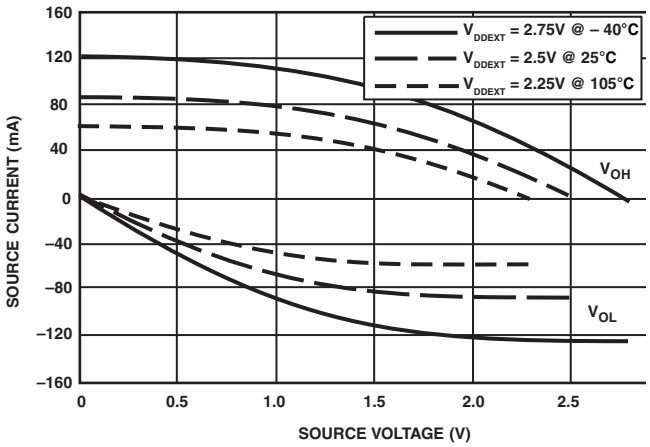


Figure 38. Driver Type A Current (2.5V V_{DDEXT}/V_{DDMEM})

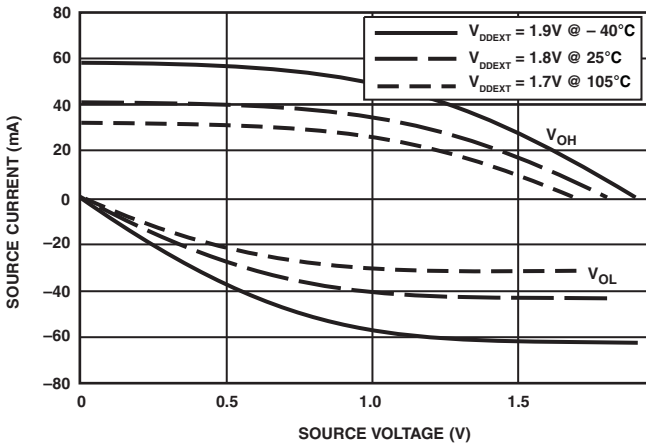


Figure 39. Driver Type A Current (1.8V V_{DDEXT}/V_{DDMEM})

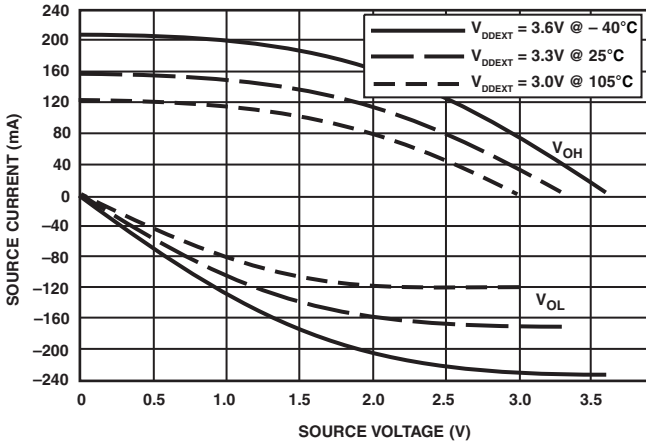


Figure 40. Driver Type B Current (3.3V V_{DDEXT}/V_{DDMEM})

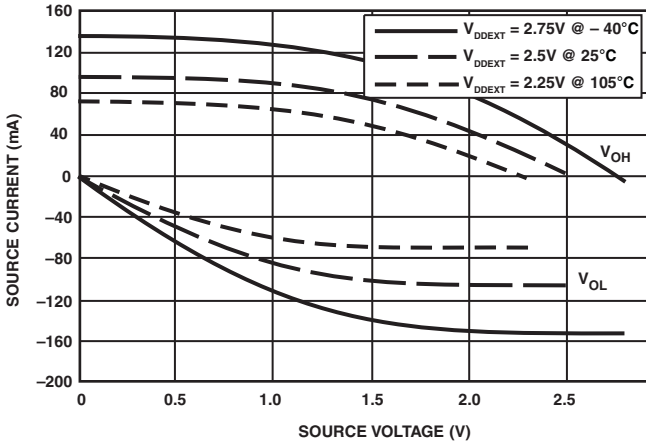


Figure 41. Driver Type B Current (2.5V V_{DDEXT}/V_{DDMEM})

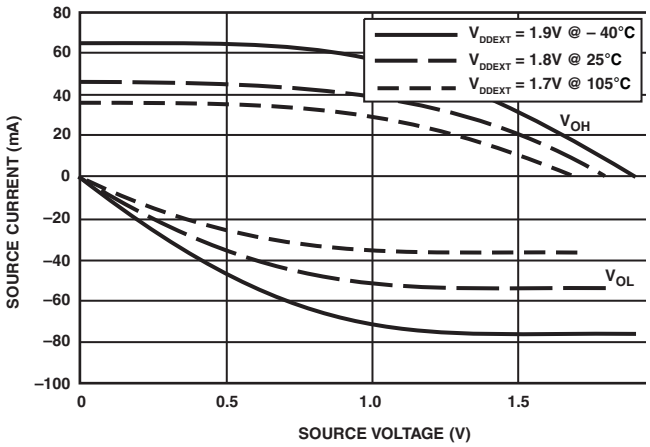


Figure 42. Driver Type B Current (1.8V V_{DDEXT}/V_{DDMEM})

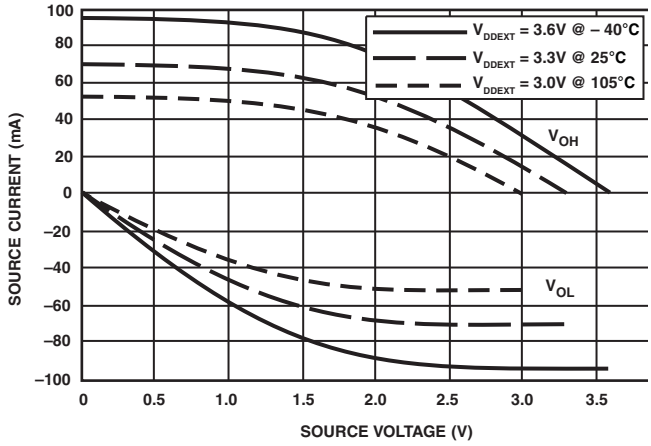


Figure 43. Driver Type C Current (3.3V V_{DDEXT}/V_{DDMEM})

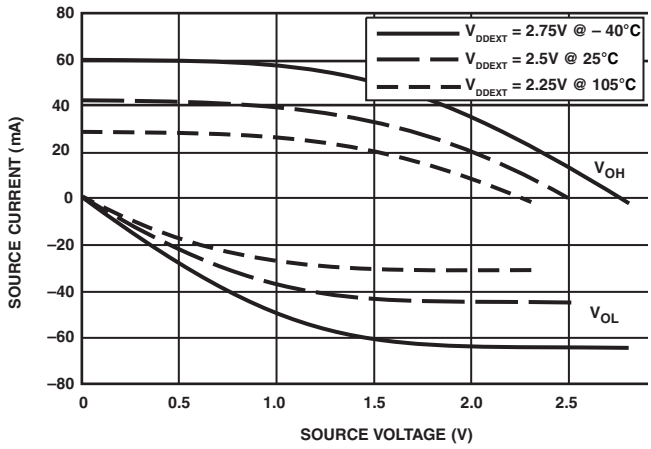


Figure 44. Drive Type C Current (2.5V V_{DDEXT}/V_{DDMEM})

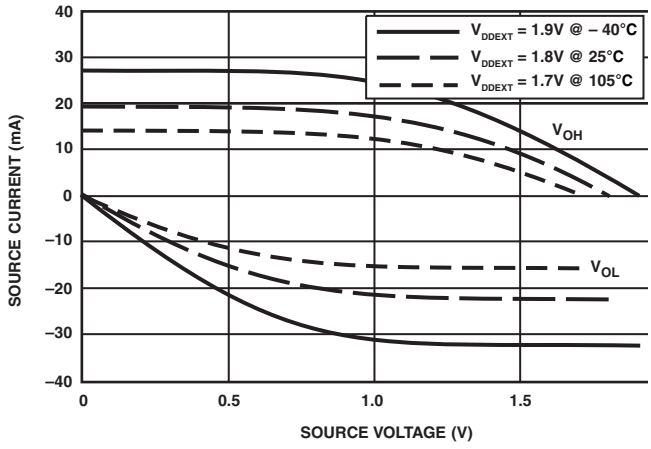


Figure 45. Driver Type C Current (1.8V V_{DDEXT}/V_{DDMEM})

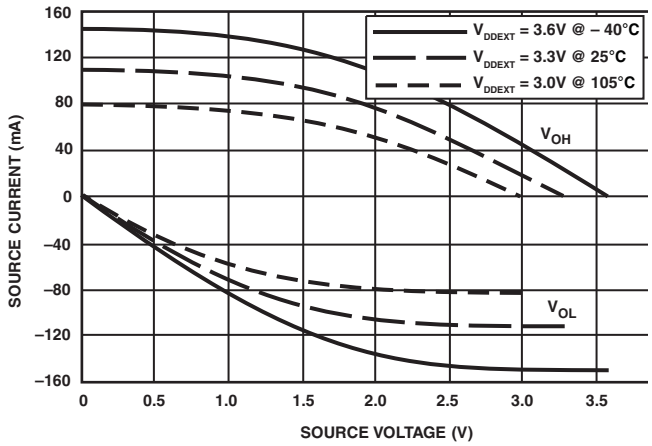


Figure 46. Driver Type D Current (3.3V V_{DDEXT}/V_{DDMEM})

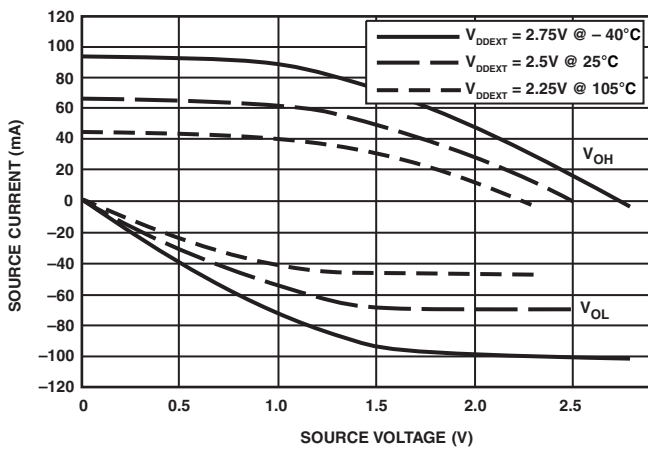


Figure 47. Driver Type D Current (2.5V V_{DDEXT}/V_{DDMEM})

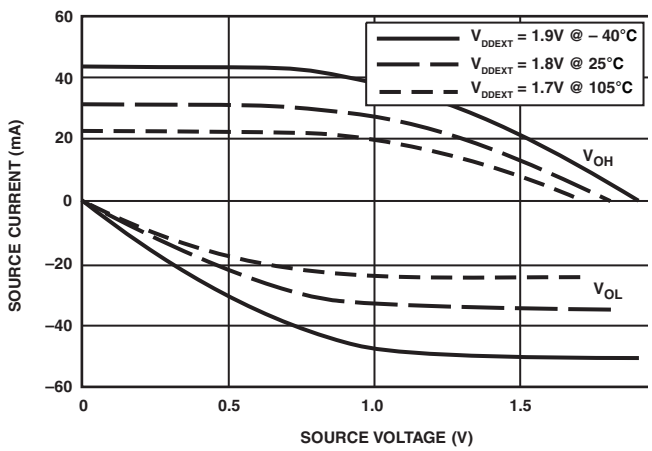


Figure 48. Driver Type D Current (1.8V V_{DDEXT}/V_{DDMEM})

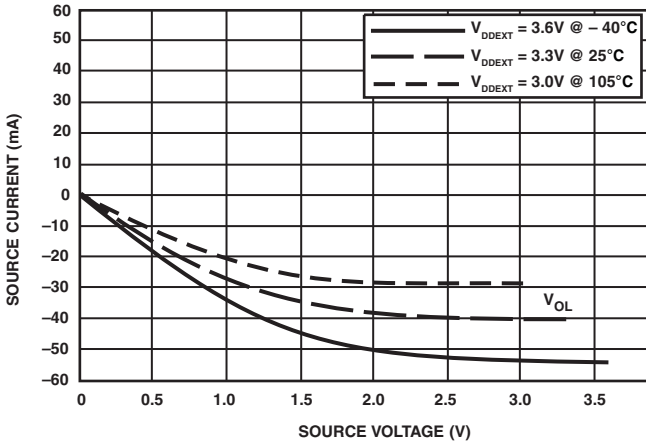


Figure 49. Driver Type E Current (3.3V V_{DDEXT}/V_{DDMEM})

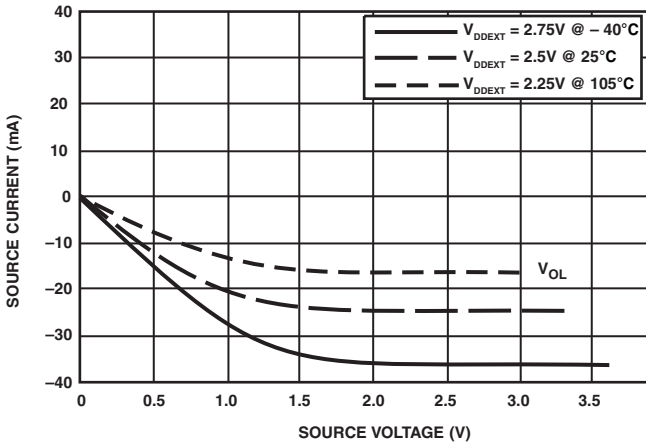


Figure 50. Driver Type E Current (2.5V V_{DDEXT}/V_{DDMEM})

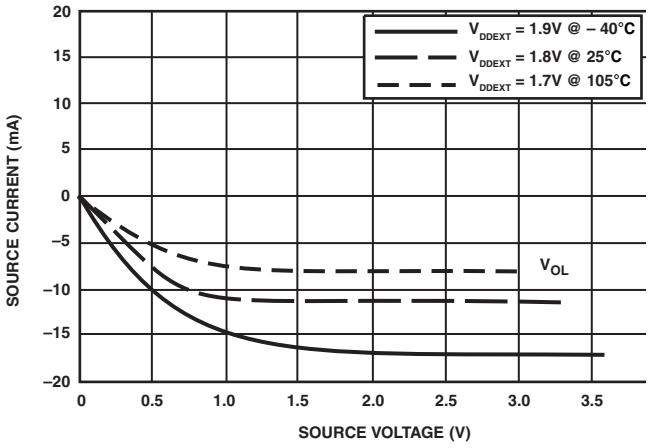


Figure 51. Driver Type E Current (1.8V V_{DDEXT}/V_{DDMEM})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 52 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is V_{DDEXT}/2 or V_{DDMEM}/2 for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V.

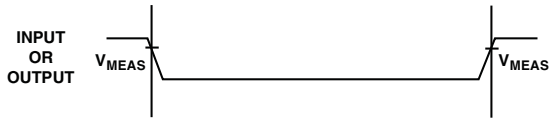


Figure 52. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output signals are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 53.

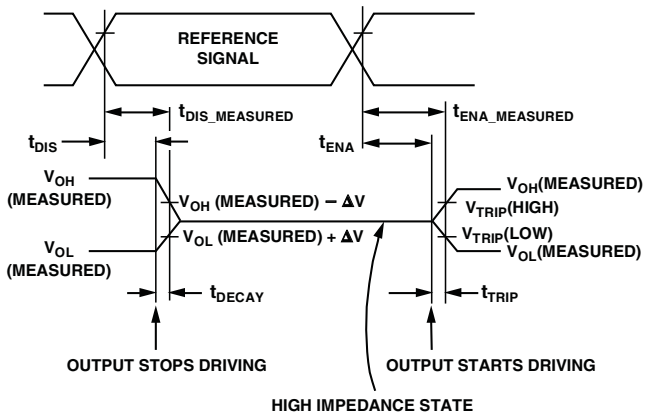


Figure 53. Output Enable/Disable

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). V_{TRIP}(high) is 2.0 V and V_{TRIP}(low) is 1.0 V for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple signals (such as the data bus) are enabled, the measurement value is that of the first signal to start driving.

Output Disable Time Measurement

Output signals are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 53.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V for V_{DDEXT}/V_{DDMEM} (nominal) = 2.5 V/3.3 V.

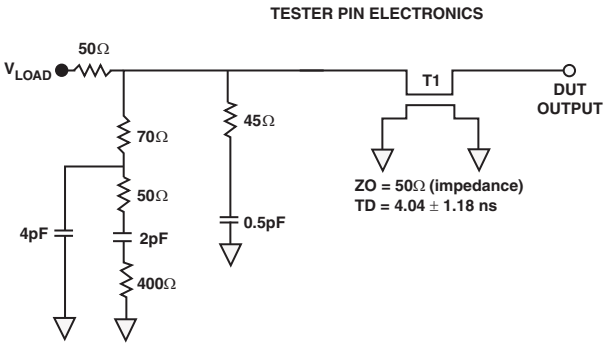
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF51x processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 31 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 35).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 54). V_{LOAD} is equal to (V_{DDEXT}/V_{DDMEM}) /2. The graphs of Figure 55 through Figure 66 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 54. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

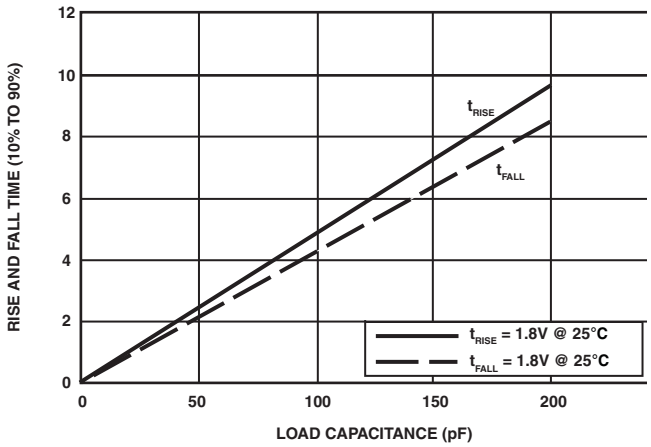


Figure 55. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

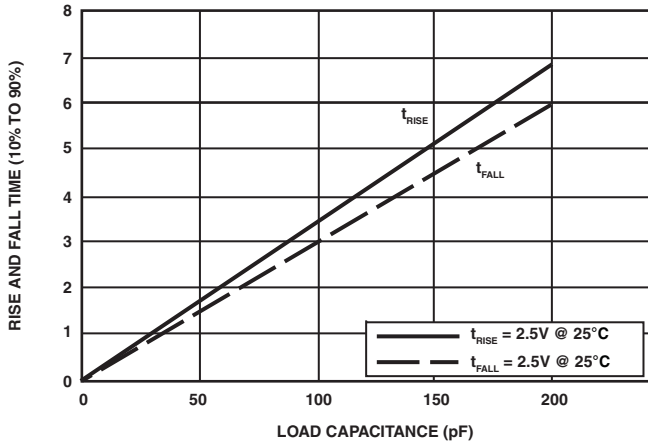


Figure 56. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

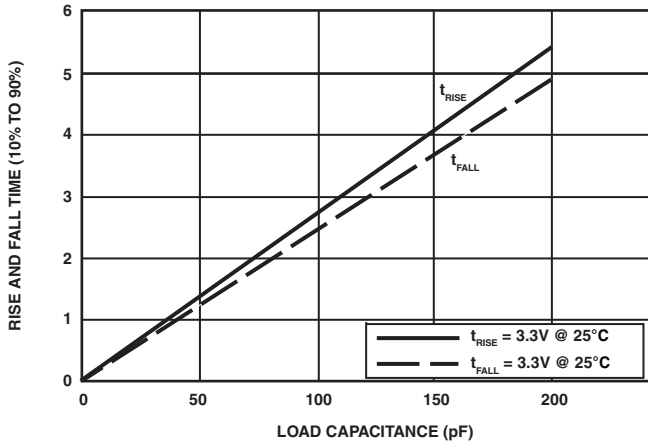


Figure 57. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

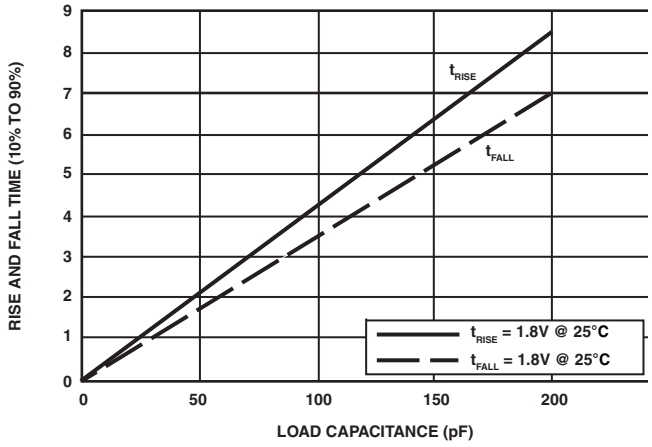


Figure 58. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

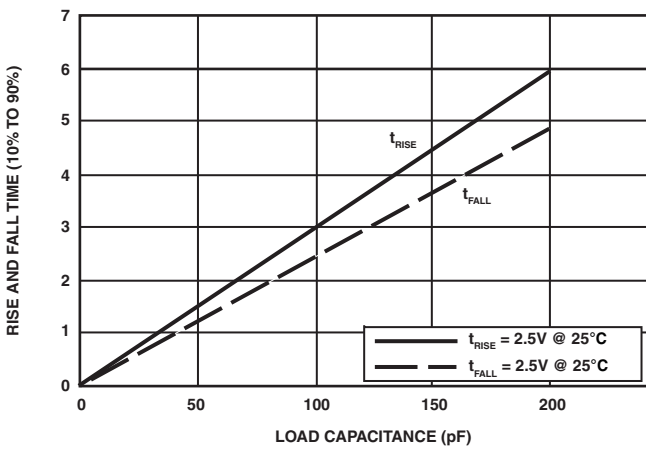


Figure 59. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

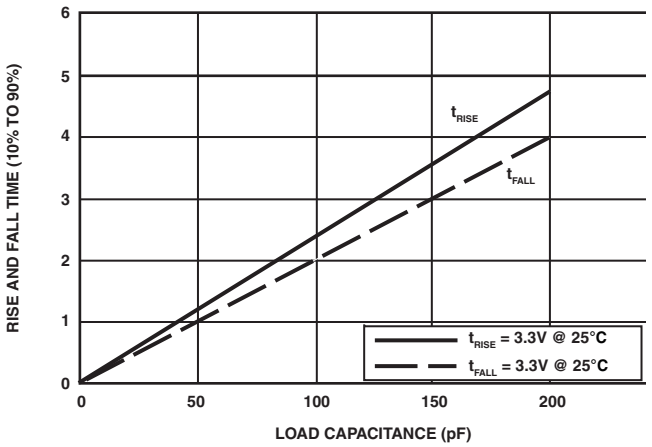


Figure 60. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

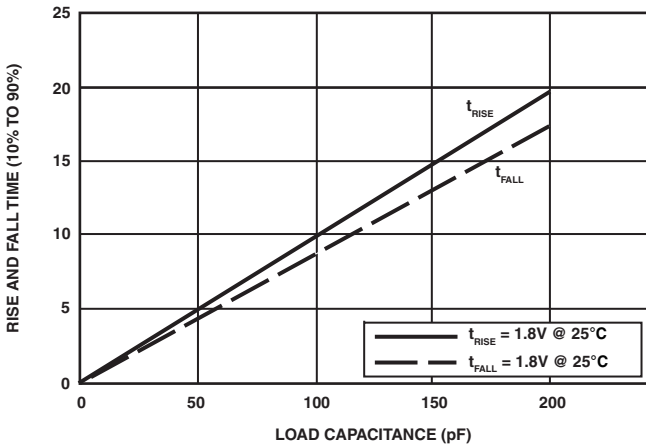


Figure 61. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

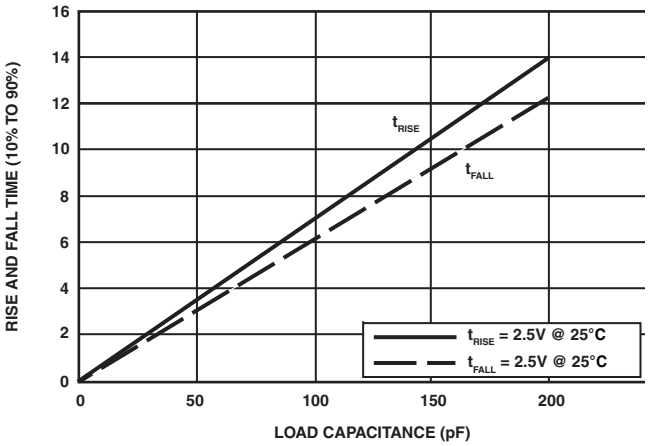


Figure 62. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

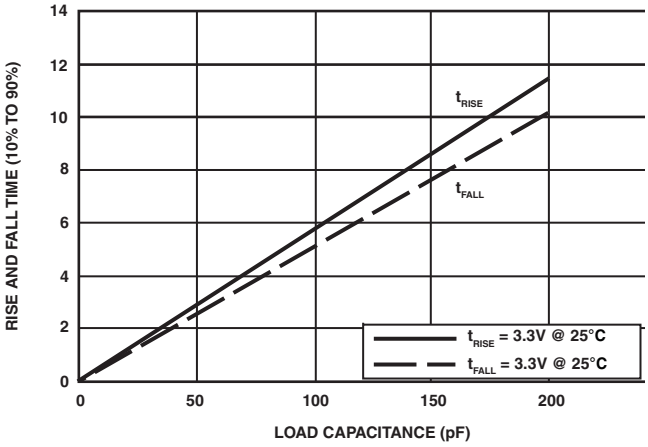


Figure 63. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

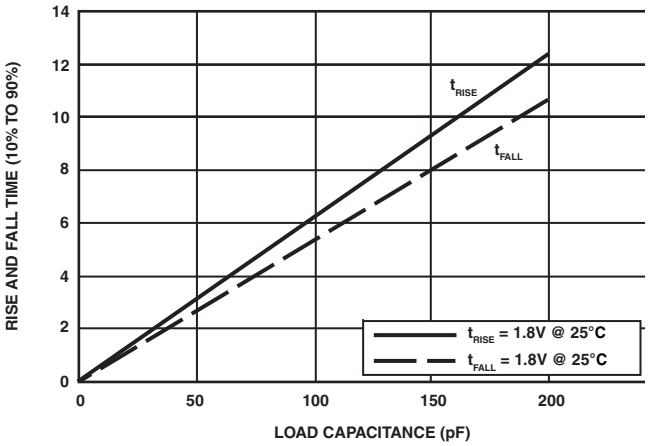


Figure 64. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

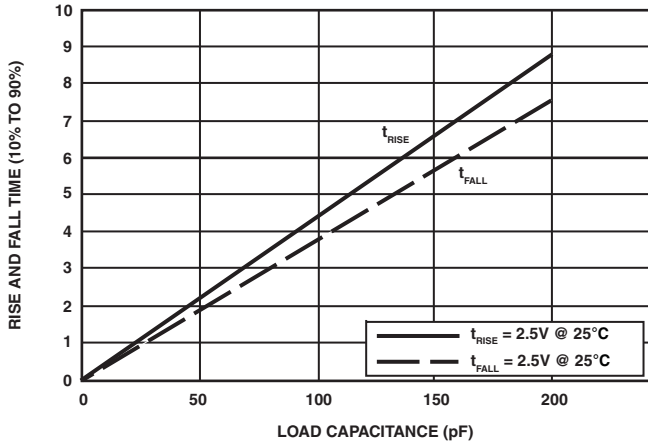


Figure 65. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

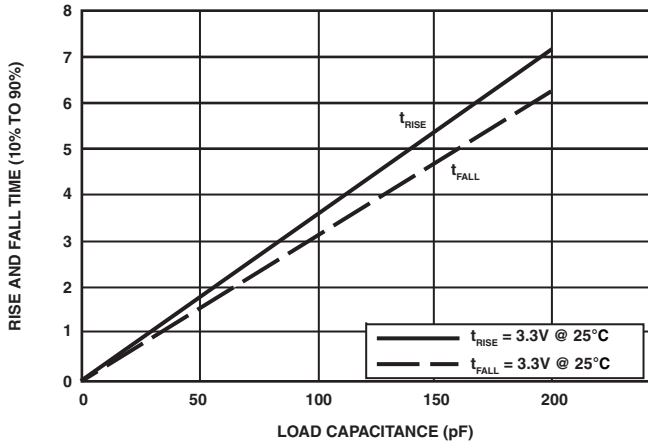


Figure 66. Driver Type D Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 55

P_D = Power dissipation (see Total Power Dissipation on Page 28 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 55, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

The LQFP-EP package requires thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. The paddle must be connected to ground for proper operation to data sheet specifications. Refer to JEDEC standard JESD51-5 for more information.

Table 54. Thermal Characteristics for SQ-176-2 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	17.4	°C/W
θ_{JMA}	1 Linear m/s Airflow	14.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	14.0	°C/W
θ_{JC}	Not Applicable	7.8	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.28	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.39	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.48	°C/W

Table 55. Thermal Characteristics for BC-168-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	30.5	°C/W
θ_{JMA}	1 Linear m/s Airflow	27.6	°C/W
θ_{JMA}	2 Linear m/s Airflow	26.3	°C/W
θ_{JC}	Not Applicable	11.1	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.20	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.35	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.45	°C/W

176-LEAD LQFP LEAD ASSIGNMENT

Table 56 lists the LQFP leads by lead number. Table 57 on Page 62 lists the LQFP by signal mnemonic.

Table 56. 176-Lead LQFP Pin Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	45	GND	89	GND	133	GND
2	GND	46	GND	90	GND	134	GND
3	PF9	47	PG1	91	A12	135	$\overline{PG}$
4	PF8	48	PG0	92	A11	136	V_{DDEXT}
5	PF7	49	V_{DDEXT}	93	A10	137	GND
6	PF6	50	TDO	94	A9	138	V_{DDINT}
7	V_{DDEXT}	51	$\overline{EMU}$	95	V_{DDMEM}	139	GND
8	V_{PPOTP}	52	TDI	96	A8	140	RTXO
9	V_{DDOTP}	53	TCK	97	A7	141	RTXI
10	PF5	54	$\overline{TRST}$	98	V_{DDINT}	142	V_{DDRTC}
11	PF4	55	TMS	99	GND	143	CLKIN
12	PF3	56	D15	100	V_{DDINT}	144	XTAL
13	PF2	57	D14	101	A6	145	V_{DDEXT}
14	V_{DDINT}	58	D13	102	A5	146	$\overline{RESET}$
15	GND	59	V_{DDMEM}	103	A4	147	$\overline{NMI}$
16	$V_{DDFLASH}$	60	D12	104	V_{DDMEM}	148	V_{DDEXT}
17	$V_{DDFLASH}$	61	D11	105	A3	149	GND
18	PF1	62	D10	106	A2	150	CLKBUF
19	PF0	63	V_{DDINT}	107	A1	151	GND
20	PG15	64	D9	108	$\overline{ABE}$1	152	V_{DDINT}
21	PG14	65	D8	109	$\overline{ABE}$0	153	PH7
22	GND	66	D7	110	SA10	154	PH6
23	V_{DDINT}	67	GND	111	GND	155	PH5
24	V_{DDEXT}	68	V_{DDMEM}	112	V_{DDMEM}	156	PH4
25	PG13	69	D6	113	$\overline{SWE}$	157	GND
26	PG12	70	D5	114	$\overline{SCAS}$	158	V_{DDEXT}
27	PG11	71	D4	115	$\overline{SRAS}$	159	PH3
28	PG10	72	D3	116	V_{DDINT}	160	PH2
29	$V_{DDFLASH}$	73	D2	117	GND	161	PH1
30	V_{DDINT}	74	D1	118	$\overline{SMS}$	162	PH0
31	PG9	75	V_{DDMEM}	119	SCKE	163	GND
32	PG8	76	D0	120	$\overline{AMS}$1	164	V_{DDINT}
33	PG7	77	A19	121	$\overline{ARE}$	165	PF15
34	PG6	78	A18	122	$\overline{AWE}$	166	PF14
35	V_{DDEXT}	79	V_{DDINT}	123	$\overline{AMS}$0	167	PF13
36	PG5	80	A17	124	V_{DDMEM}	168	PF12
37	PG4	81	A16	125	CLKOUT	169	GND
38	PG3	82	V_{DDMEM}	126	$V_{DDFLASH}$	170	V_{DDEXT}
39	PG2	83	GND	127	NC[1]	171	PF11
40	BMODE2	84	A15	128	V_{DDEXT}	172	SDA
41	BMODE1	85	A14	129	V_{DDEXT}	173	SCL
42	BMODE0	86	A13	130	EXT_WAKE	174	PF10
43	GND	87	GND	131	GND	175	GND
44	GND	88	GND	132	GND	176	GND

[1] This pin must not be connected.

Table 57. 176-Lead LQFP Pin Assignment (Alphabetically by Signal Mnemonic)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
107	A1	58	D13	5	PF7	113	$\overline{SWE}$
106	A2	57	D14	4	PF8	53	TCK
105	A3	56	D15	3	PF9	52	TDI
103	A4	51	$\overline{EMU}$	174	PF10	50	TDO
102	A5	130	EXT_WAKE	171	PF11	55	TMS
101	A6	1	GND	168	PF12	54	$\overline{TRST}$
97	A7	2	GND	167	PF13	7	V_{DDEXT}
96	A8	15	GND	166	PF14	24	V_{DDEXT}
94	A9	22	GND	165	PF15	35	V_{DDEXT}
93	A10	43	GND	135	$\overline{PG}$	49	V_{DDEXT}
92	A11	44	GND	48	PG0	128	V_{DDEXT}
91	A12	45	GND	47	PG1	129	V_{DDEXT}
86	A13	46	GND	39	PG2	136	V_{DDEXT}
85	A14	67	GND	38	PG3	145	V_{DDEXT}
84	A15	83	GND	37	PG4	148	V_{DDEXT}
81	A16	87	GND	36	PG5	158	V_{DDEXT}
80	A17	88	GND	34	PG6	170	V_{DDEXT}
78	A18	89	GND	33	PG7	16	$V_{DDFLASH}$
77	A19	90	GND	32	PG8	17	$V_{DDFLASH}$
109	$\overline{ABE}$0	99	GND	31	PG9	29	$V_{DDFLASH}$
108	$\overline{ABE}$1	111	GND	28	PG10	126	$V_{DDFLASH}$
123	$\overline{AMS}$0	131	GND	27	PG11	14	V_{DDINT}
120	$\overline{AMS}$1	132	GND	26	PG12	23	V_{DDINT}
121	$\overline{ARE}$	133	GND	25	PG13	30	V_{DDINT}
122	$\overline{AWE}$	134	GND	21	PG14	63	V_{DDINT}
42	BMODE0	137	GND	20	PG15	79	V_{DDINT}
41	BMODE1	139	GND	162	PH0	98	V_{DDINT}
40	BMODE2	149	GND	161	PH1	100	V_{DDINT}
150	CLKBUF	151	GND	160	PH2	116	V_{DDINT}
143	CLKIN	157	GND	159	PH3	138	V_{DDINT}
125	CLKOUT	163	GND	156	PH4	152	V_{DDINT}
76	D0	169	GND	155	PH5	164	V_{DDINT}
74	D1	175	GND	154	PH6	59	V_{DDMEM}
73	D2	176	GND	153	PH7	68	V_{DDMEM}
72	D3	117	GND	146	$\overline{RESET}$	75	V_{DDMEM}
71	D4	127	NC[1]	141	RTXI	82	V_{DDMEM}
70	D5	147	$\overline{NMI}$	140	RTXO	95	V_{DDMEM}
69	D6	19	PF0	110	SA10	104	V_{DDMEM}
66	D7	18	PF1	114	$\overline{SCAS}$	112	V_{DDMEM}
65	D8	13	PF2	119	SCKE	124	V_{DDMEM}
64	D9	12	PF3	173	SCL	9	V_{DDOTP}
62	D10	11	PF4	172	SDA	142	V_{DDRTC}
61	D11	10	PF5	118	$\overline{SMS}$	8	V_{PPOTP}
60	D12	6	PF6	115	$\overline{SRAS}$	144	XTAL

[1] This pin must not be connected.

168-BALL CSP_BGA BALL ASSIGNMENT

Table 58 lists the CSP_BGA by ball number. Table 59 on Page 64 lists the CSP_BGA balls by signal mnemonic.

Table 58. 168-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	GND	C1	PF4	E10	V_{DDINT}	H1	PG12	K6	V_{DDMEM}	N1	BMODE1
A2	SCL	C2	PF7	E12	V_{DDMEM}	H2	PG13	K7	V_{DDMEM}	N2	PG1
A3	SDA	C3	PF8	E13	$\overline{ARE}$	H3	PG11	K8	V_{DDMEM}	N3	TDO
A4	PF13	C4	PF10	E14	$\overline{AWE}$	H5	V_{DDEXT}	K9	V_{DDMEM}	N4	$\overline{TRST}$
A5	PF15	C5	V_{DDEXT}	F1	PF0	H6	GND	K10	V_{DDMEM}	N5	TMS
A6	PH2	C6	V_{DDEXT}	F2	PF1	H7	GND	K12	A8	N6	D13
A7	PH1	C7	PF11	F3	V_{DDINT}	H8	GND	K13	A2	N7	D9
A8	PH5	C8	V_{DDEXT}	F5	V_{DDEXT}	H9	GND	K14	A1	N8	D5
A9	PH6	C9	V_{DDINT}	F6	GND	H10	V_{DDINT}	L1	PG5	N9	D1
A10	PH7	C10	V_{DDEXT}	F7	GND	H12	A3	L2	PG3	N10	A18
A11	CLKBUF	C11	RTXI	F8	GND	H13	$\overline{ABE0}$	L3	PG2	N11	A16
A12	XTAL	C12	RTXO	F9	GND	H14	$\overline{SCAS}$	L12	A9	N12	A14
A13	CLKIN	C13	$\overline{PG}$	F10	V_{DDINT}	J1	PG10	L13	A6	N13	A11
A14	GND	C14	NC[1]	F12	$\overline{SMS}$	J2	$V_{DDFLASH}$	L14	A4	N14	A7
B1	V_{DDOTP}	D1	PF3	F13	SCKE	J3	PG9	M1	PG4	P1	GND
B2	GND	D2	PF5	F14	$\overline{AMS1}$	J5	V_{DDMEM}	M2	BMODE2	P2	TDI
B3	PF9	D3	VPPOTP	G1	PG15	J6	GND	M3	BMODE0	P3	TCK
B4	PF12	D12	$V_{DDFLASH}$	G2	PG14	J7	GND	M4	PG0	P4	D15
B5	PF14	D13	CLKOUT	G3	V_{DDINT}	J8	GND	M5	$\overline{EMU}$	P5	D14
B6	PH0	D14	$\overline{AMS0}$	G5	V_{DDEXT}	J9	GND	M6	D12	P6	D11
B7	PH3	E1	$V_{DDFLASH}$	G6	GND	J10	V_{DDINT}	M7	D10	P7	D8
B8	PH4	E2	PF2	G7	GND	J12	A15	M8	D2	P8	D7
B9	V_{DDEXT}	E3	PF6	G8	GND	J13	$\overline{ABE1}$	M9	D0	P9	D6
B10	$\overline{RESET}$	E5	V_{DDEXT}	G9	GND	J14	SA10	M10	A17	P10	D4
B11	$\overline{NMI}$	E6	V_{DDEXT}	G10	V_{DDINT}	K1	PG6	M11	A13	P11	D3
B12	V_{DDRTC}	E7	V_{DDINT}	G12	$\overline{SWE}$	K2	PG8	M12	A12	P12	A19
B13	V_{DDEXT}	E8	V_{DDINT}	G13	$\overline{SRAS}$	K3	PG7	M13	A10	P13	GND
B14	EXT_WAKE	E9	V_{DDINT}	G14	GND	K5	V_{DDMEM}	M14	A5	P14	GND

[1] This pin must not be connected.

Table 59. 168-Ball CSP_BGA Ball Assignment (Alphabetically by Signal Mnemonic)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
K14	A1	A11	CLKBUF	G6	GND	C4	PF10	A8	PH5	G5	V_{DDEXT}
K13	A2	A13	CLKIN	G7	GND	C7	PF11	A9	PH6	H5	V_{DDEXT}
H12	A3	D13	CLKOUT	G8	GND	B4	PF12	A10	PH7	D12	$V_{DDFLASH}$
L14	A4	M9	D0	G9	GND	A4	PF13	B10	$\overline{RESET}$	E1	$V_{DDFLASH}$
M14	A5	N9	D1	H6	GND	B5	PF14	C11	RTXI	J2	$V_{DDFLASH}$
L13	A6	M8	D2	H7	GND	A5	PF15	C12	RTXO	C9	V_{DDINT}
N14	A7	P11	D3	H8	GND	C13	$\overline{PG}$	J14	SA10	E7	V_{DDINT}
K12	A8	P10	D4	H9	GND	M4	PG0	H14	$\overline{SCAS}$	E8	V_{DDINT}
L12	A9	N8	D5	J6	GND	N2	PG1	F13	SCKE	E9	V_{DDINT}
M13	A10	P9	D6	J7	GND	L3	PG2	A2	SCL	E10	V_{DDINT}
N13	A11	P8	D7	J8	GND	L2	PG3	A3	SDA	F3	V_{DDINT}
M12	A12	P7	D8	J9	GND	M1	PG4	F12	$\overline{SMS}$	F10	V_{DDINT}
M11	A13	N7	D9	P1	GND	L1	PG5	G13	$\overline{SRAS}$	G3	V_{DDINT}
N12	A14	M7	D10	P13	GND	K1	PG6	G12	$\overline{SWE}$	G10	V_{DDINT}
J12	A15	P6	D11	P14	GND	K3	PG7	P3	TCK	H10	V_{DDINT}
N11	A16	M6	D12	G14	GND	K2	PG8	P2	TDI	J10	V_{DDINT}
M10	A17	N6	D13	C14	NC[1]	J3	PG9	N3	TDO	E12	V_{DDMEM}
N10	A18	P5	D14	B11	$\overline{NMI}$	J1	PG10	N5	TMS	J5	V_{DDMEM}
P12	A19	P4	D15	F1	PF0	H3	PG11	N4	$\overline{TRST}$	K5	V_{DDMEM}
H13	$\overline{ABE}$0	M5	$\overline{EMU}$	F2	PF1	H1	PG12	B9	V_{DDEXT}	K6	V_{DDMEM}
J13	$\overline{ABE}$1	B14	EXT_WAKE	E2	PF2	H2	PG13	B13	V_{DDEXT}	K7	V_{DDMEM}
D14	$\overline{AMS}$0	A1	GND	D1	PF3	G2	PG14	C5	V_{DDEXT}	K8	V_{DDMEM}
F14	$\overline{AMS}$1	A14	GND	C1	PF4	G1	PG15	C6	V_{DDEXT}	K9	V_{DDMEM}
E13	$\overline{ARE}$	B2	GND	D2	PF5	B6	PH0	C8	V_{DDEXT}	K10	V_{DDMEM}
E14	$\overline{AWE}$	F6	GND	E3	PF6	A7	PH1	C10	V_{DDEXT}	B1	V_{DDOTP}
M3	BMODE0	F7	GND	C2	PF7	A6	PH2	E5	V_{DDEXT}	B12	V_{DDRTC}
N1	BMODE1	F8	GND	C3	PF8	B7	PH3	E6	V_{DDEXT}	D3	V_{PPOTP}
M2	BMODE2	F9	GND	B3	PF9	B8	PH4	F5	V_{DDEXT}	A12	XTAL

[1] This pin must not be connected.

Figure 67 shows the top view of the CSP_BGA ball configuration. Figure 68 shows the bottom view of the CSP_BGA ball configuration.

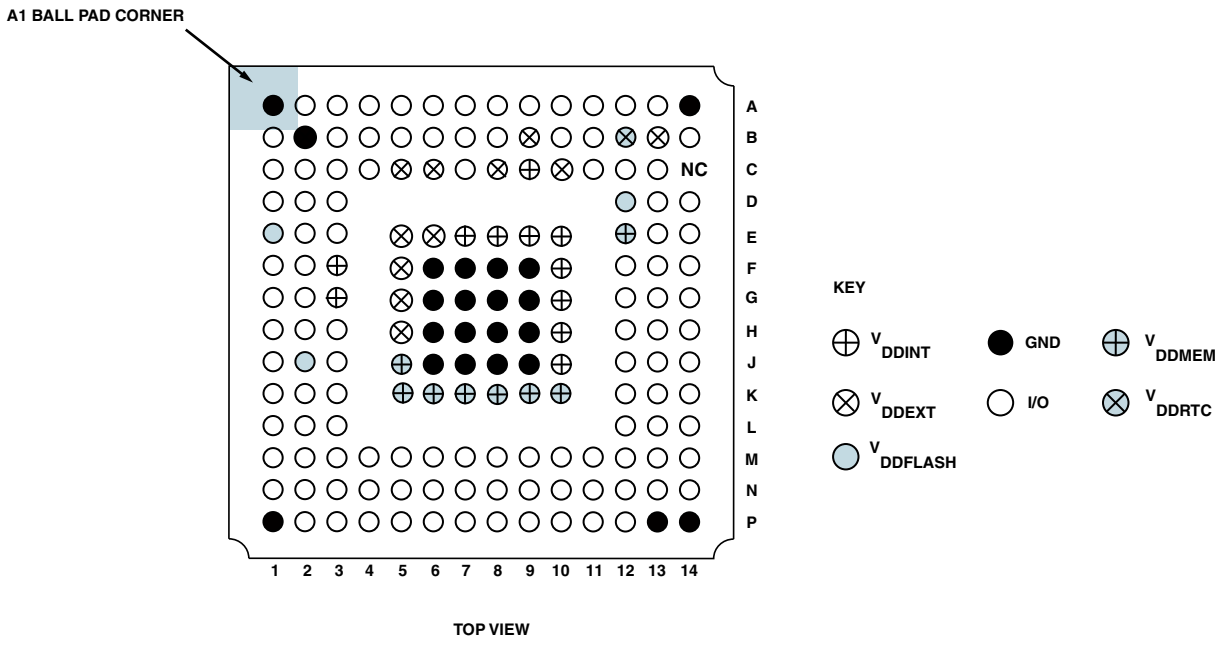


Figure 67. 168-Ball CSP_BGA Ball Configuration (Top View)

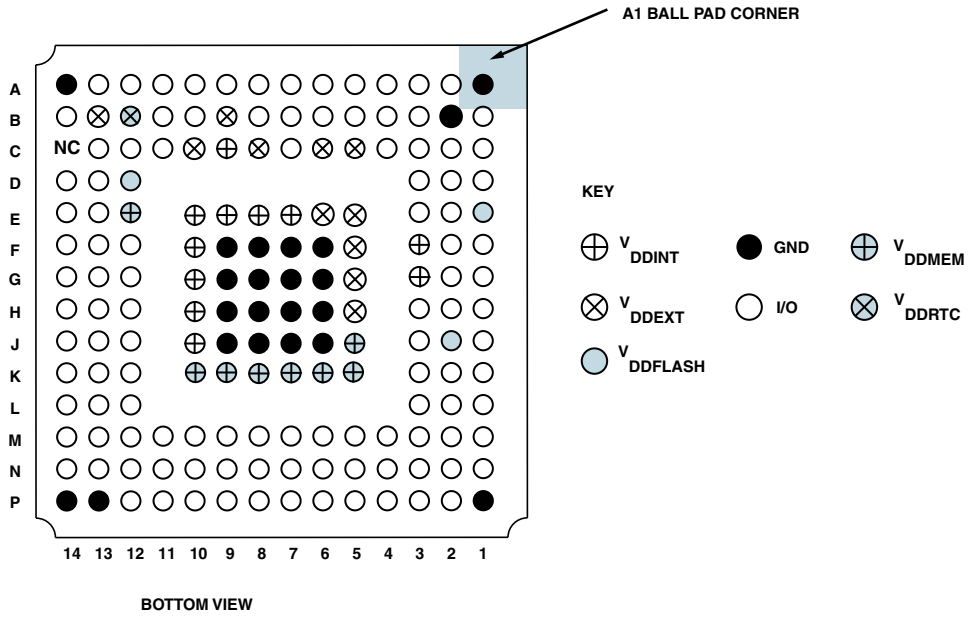


Figure 68. 168-Ball CSP_BGA Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 69 are shown in millimeters.

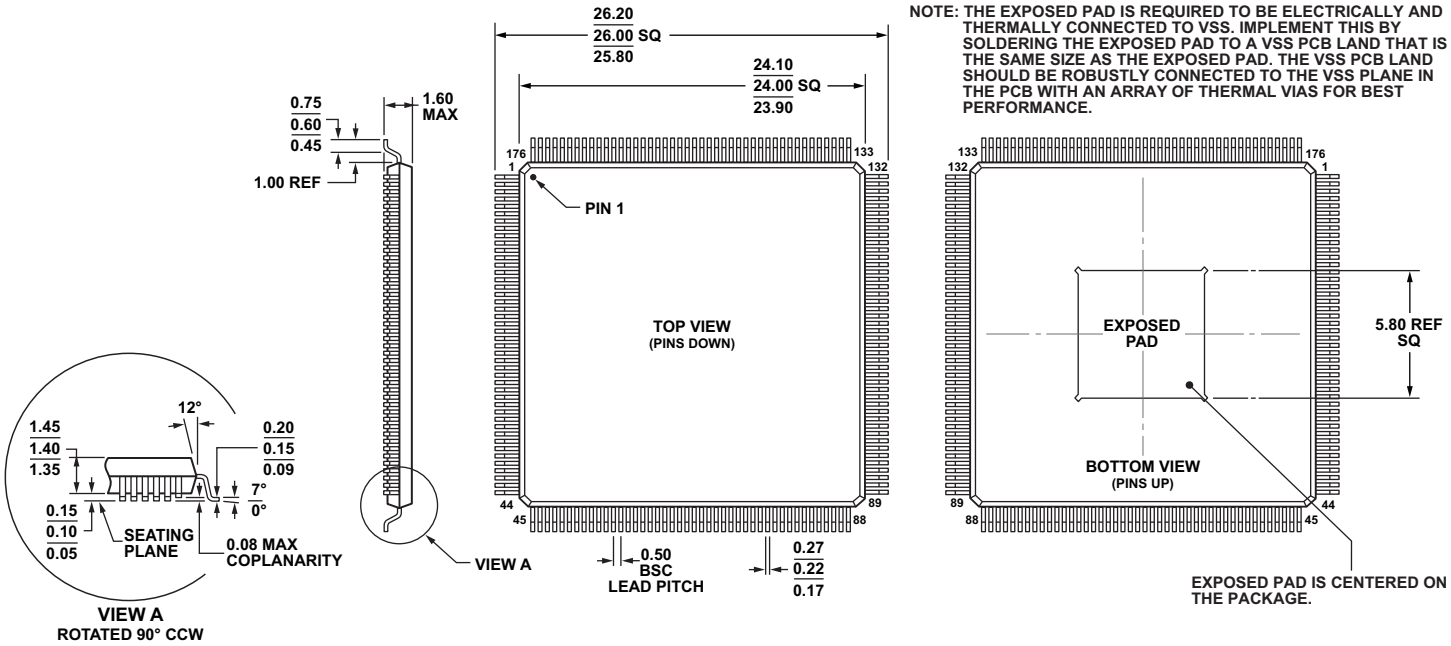


Figure 69. 176-Lead Low Profile Quad Flat Package [LQFP_EP]
(SQ-176-2)
Dimensions shown in millimeters

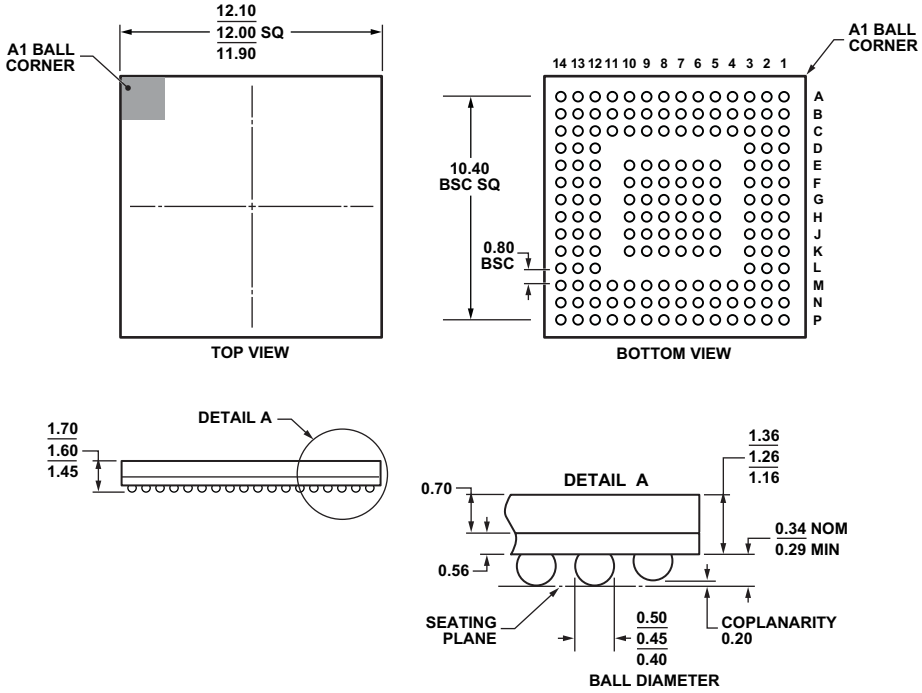


Figure 70. 168-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-168-1)
Dimensions shown in millimeters

SURFACE MOUNT DESIGN

Table 60 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 60. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
168-Ball CSP_BGA	Solder Mask Defined	TBD mm diameter	TBD mm diameter

ORDERING GUIDE

Model[1]	Temperature Range[2]	Processor Instruction Rate (Max)	Flash Memory	Package Description	Package Option
ADSP-BF518BSWZ-4FX	–40°C to +85°C	400 MHz	4M Bit	176-Lead LQFP_EP	SQ-176-2
ADSP-BF518BSWZ-4X	–40°C to +85°C	400 MHz	n/a	176-Lead LQFP_EP	SQ-176-2
ADSP-BF518KBCZ-4FX	0°C to +70°C	400 MHz	4M Bit	168-Ball CSP-BGA	BC-168-1
ADSP-BF518KBCZ-4X	0°C to +70°C	400 MHz	n/a	168-Ball CSP-BGA	BC-168-1

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is ambient temperature.

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