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## REVISION HISTORY

### 7/13—Revision I to Revision J

|                                                                                                           |    |
|-----------------------------------------------------------------------------------------------------------|----|
| Updated <a href="#">Development Tools</a> .....                                                           | 9  |
| Added Nominal Value column in <a href="#">Operating Conditions</a> ..                                     | 14 |
| Changed Max values in <a href="#">Table 30</a> in <a href="#">Pulse-Width Modulation Generators</a> ..... | 35 |
| Updated <a href="#">Ordering Guide</a> .....                                                              | 56 |

## GENERAL DESCRIPTION

The ADSP-2136x SHARC® processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices, Inc., Super Harvard Architecture. The processor is source code-compatible with the ADSP-2126x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2136x are 32-/40-bit floating-point processors optimized for high performance automotive audio applications. They contain a large on-chip SRAM and ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital audio interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-2136x uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of signal processing algorithms. With its SIMD computational hardware, the ADSP-2136x can perform two GFLOPS running at 333 MHz.

Table 1 shows performance benchmarks for these devices. Table 2 shows the features of the individual product offerings.

**Table 1. Benchmarks (at 333 MHz)**

| Benchmark Algorithm                             | Speed (at 333 MHz) |
|-------------------------------------------------|--------------------|
| 1024 Point Complex FFT (Radix 4, with reversal) | 27.9 $\mu$ s       |
| FIR Filter (per tap) <sup>1</sup>               | 1.5 ns             |
| IIR Filter (per biquad) <sup>1</sup>            | 6.0 ns             |
| Matrix Multiply (pipelined)                     |                    |
| $[3 \times 3] \times [3 \times 1]$              | 13.5 ns            |
| $[4 \times 4] \times [4 \times 1]$              | 23.9 ns            |
| Divide (y/x)                                    | 10.5 ns            |
| Inverse Square Root                             | 16.3 ns            |

<sup>1</sup> Assumes two files in multichannel SIMD mode.

**Table 2. ADSP-2136x Family Features**

| Feature                            | ADSP-21362 | ADSP-21363 | ADSP-21364 | ADSP-21365 | ADSP-21366 |
|------------------------------------|------------|------------|------------|------------|------------|
| RAM                                | 3M bit     | 3M bit     | 3M bit     | 3M bit     | 3M bit     |
| ROM                                | 4M bit     | 4M bit     | 4M bit     | 4M bit     | 4M bit     |
| Audio Decoders in ROM <sup>1</sup> | No         | No         | No         | Yes        | Yes        |
| Pulse-Width Modulation             | Yes        | Yes        | Yes        | Yes        | Yes        |
| S/PDIF                             | Yes        | No         | Yes        | Yes        | Yes        |
| DTCP <sup>2</sup>                  | Yes        | No         | No         | Yes        | No         |
| SRC SNR Performance                | -128 dB    | No SRC     | -140 dB    | -128 dB    | -128 dB    |

<sup>1</sup> Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Pro Logic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit [www.analog.com](http://www.analog.com) for complete information.

<sup>2</sup> The ADSP-21362 and ADSP-21365 processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2136x processors. The core clock domain contains the following features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (3M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints, which allow flexible exception handling.

The diagram on Page 1 also shows the following architectural features:

- I/O processor that handles 32-bit DMA for the peripherals
- Six full duplex serial ports
- Two SPI-compatible interface ports—primary on dedicated pins, secondary on DAI pins
- 8-bit or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- Digital audio interface that includes two precision clock generators (PCG), an input data port with eight serial interfaces (IDP), an S/PDIF receiver/transmitter, 8-channel asynchronous sample rate converter (ASRC), DTCP cipher, six serial ports, a 20-bit parallel input data port (PDAP), 10 interrupts, six flag outputs, six flag inputs, three timers, and a flexible signal routing unit (SRU)

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## SHARC FAMILY CORE ARCHITECTURE

The ADSP-2136x is code-compatible at the assembly level with the ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2136x shares architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC processors, as shown in [Figure 2](#) and detailed in the following sections.

### SIMD Computational Engine

The processor contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY can be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive signal processing algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

### Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit, single-precision floating-point, 40-bit extended-precision floating-point, and 32-bit fixed-point data formats.

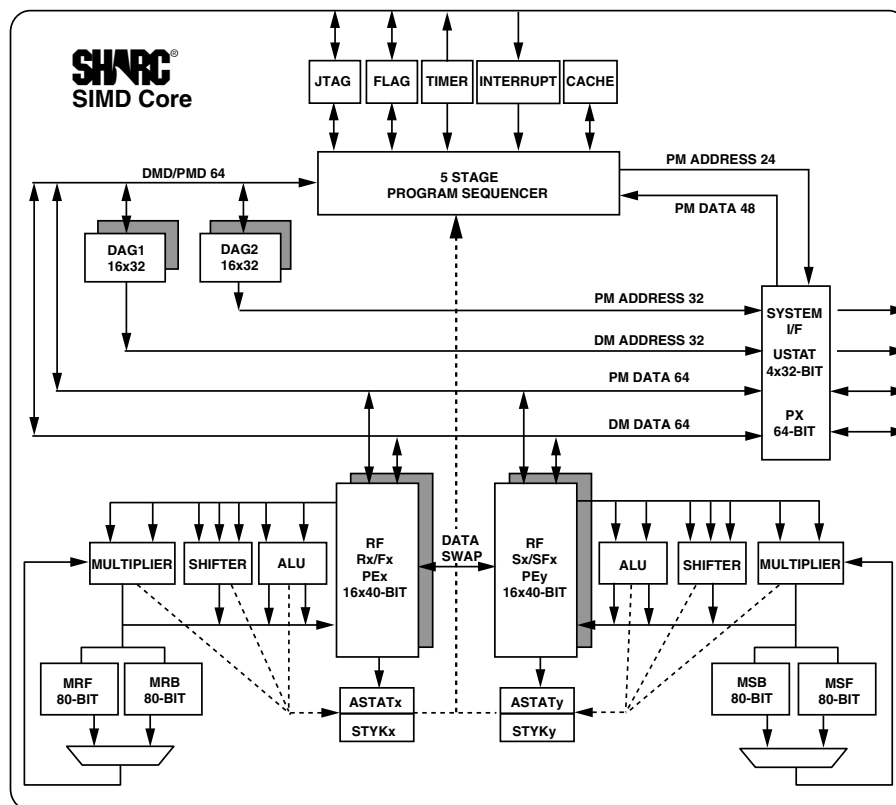


Figure 2. SHARC Core Block Diagram

**Data Register File**

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

**Context Switch**

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result register all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

**Universal Registers**

The universal registers are general purpose registers. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

**Timer**

A core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

**Single-Cycle Fetch of Instruction and Four Operands**

The processor features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

**Instruction Cache**

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

**Data Address Generators with Zero-Overhead Hardware Circular Buffer Support**

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal

processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

**Flexible Instruction Set**

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the processor can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

**On-Chip Memory**

The processor contains 3M bits of internal SRAM and 4M bits of internal ROM. Each block can be configured for different combinations of code and data storage (see Table 3). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The processor's memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The SRAM can be configured as a maximum of 96K words of 32-bit data, 192K words of 16-bit data, 64K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 3M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

**On-Chip Memory Bandwidth**

The internal memory architecture allows three accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is gained with DMD and PMD buses ( $2 \times 64$ -bits, core CLK) and the IOD bus (32-bit, PCLK).

**ROM-Based Security**

The processor has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG

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Table 3. ADSP-2136x Internal Memory Space

| IOP Registers 0x0000 0000–0003 FFFF     |                                                         |                                         |                                         |
|-----------------------------------------|---------------------------------------------------------|-----------------------------------------|-----------------------------------------|
| Long Word (64 Bits)                     | Extended Precision Normal or Instruction Word (48 Bits) | Normal Word (32 Bits)                   | Short Word (16 Bits)                    |
| Block 0 ROM<br>0x0004 0000–0x0004 7FFF  | Block 0 ROM<br>0x0008 0000–0x0008 AAA9                  | Block 0 ROM<br>0x0008 0000–0x0008 FFFF  | Block 0 ROM<br>0x0010 0000–0x0011 FFFF  |
| Reserved<br>0x0004 8000–0x0004 BFFF     |                                                         | Reserved<br>0x0009 0000–0x0009 7FFF     | Reserved<br>0x0012 0000–0x0012 FFFF     |
| Block 0 SRAM<br>0x0004 C000–0x0004 FFFF | Block 0 SRAM<br>0x0009 0000–0x0009 5554                 | Block 0 SRAM<br>0x0009 8000–0x0009 FFFF | Block 0 SRAM<br>0x0013 0000–0x0013 FFFF |
| Block 1 ROM<br>0x0005 0000–0x0005 7FFF  | Block 1 ROM<br>0x000A 0000–0x000A AAA9                  | Block 1 ROM<br>0x000A 0000–0x000A FFFF  | Block 1 ROM<br>0x0014 0000–0x0015 FFFF  |
| Reserved<br>0x0005 8000–0x0005 BFFF     |                                                         | Reserved<br>0x000B 0000–0x000B 7FFF     | Reserved<br>0x0016 0000–0x0016 FFFF     |
| Block 1 SRAM<br>0x0005 C000–0x0005 FFFF | Block 1 SRAM<br>0x000B 0000–0x000B 5554                 | Block 1 SRAM<br>0x000B 8000–0x000B FFFF | Block 1 SRAM<br>0x0017 0000–0x0017 FFFF |
| Block 2 SRAM<br>0x0006 0000–0x0006 1FFF | Block 2 SRAM<br>0x000C 0000–0x000C 2AA9                 | Block 2 SRAM<br>0x000C 0000–0x000C 3FFF | Block 2 SRAM<br>0x0018 0000–0x0018 7FFF |
| Reserved<br>0x0006 2000–0x0006 FFFF     |                                                         | Reserved<br>0x000C 4000–0x000D FFFF     | Reserved<br>0x0018 8000–0x001B FFFF     |
| Block 3 SRAM<br>0x0007 0000–0x0007 1FFF | Block 3 SRAM<br>0x000E 0000–0x000E 2AA9                 | Block 3 SRAM<br>0x000E 0000–0x000E 3FFF | Block 3 SRAM<br>0x001C 0000–0x001C 7FFF |
| Reserved<br>0x0007 2000–0x0007 FFFF     |                                                         | Reserved<br>0x000E 4000–0x000F FFFF     | Reserved<br>0x001C 8000–0x001F FFFF     |
|                                         |                                                         |                                         | Reserved<br>0x0020 0000–0xFFFF FFFF     |

or test access port, is assigned to each customer. The device ignores a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

## FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2136x family contains a rich set of peripherals that support a wide variety of applications, including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, monitor control, imaging, and other applications.

### Parallel Port

The parallel port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15–0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8-bit or 16-bit, the maximum data transfer rate is  $f_{PCLK}/4$ .

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The  $\overline{RD}$ ,  $\overline{WR}$ , and ALE (address latch enable) pins are the control pins for the parallel port.

### Serial Peripheral (Compatible) Interface

The processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the processor's SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes and can operate at a maximum baud rate of  $f_{PCLK}/4$ .

The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-2136x SPI-compatible peripheral implementation also features programmable baud rate, clock phase, and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

### Pulse-Width Modulation

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can

generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

### **Digital Audio Interface (DAI)**

The digital audio interface (DAI) provides the ability to connect various peripherals to any of the DSP's DAI pins (DAI\_P20–1). Programs make these connections using the signal routing unit (SRU, shown in [Figure 1](#)).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI-associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes six serial ports, an S/PDIF receiver/transmitter, a DTCP cipher, a precision clock generator (PCG), eight channels of asynchronous sample rate converters, an input data port (IDP), an SPI port, six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2136x core, configurable as either eight channels of I<sup>2</sup>S serial data or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

### **Serial Ports**

The processor features six synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and a frame sync and they can operate at maximum  $f_{CLK}/4$ . The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I<sup>2</sup>S mode
- Left-justified sample pair mode

### **S/PDIF-Compatible Digital Audio Receiver/Transmitter**

The S/PDIF transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphasic encoded signal. The serial data input to the transmitter can be formatted as left-justified, I<sup>2</sup>S, or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), or the sample rate converters (SRC) and are controlled by the SRU control registers.

### **Digital Transmission Content Protection (DTCP)**

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system. This feature is available on the ADSP-21362 and ADSP-21365 processors only. Licensing through DTLA is required for these products. Visit [www.dtcp.com](http://www.dtcp.com) for more information.

### **Memory-to-Memory (MTM)**

If the DTCP module is not used, the memory-to-memory DMA module allows internal memory copies for a standard DMA.

### **Synchronous/Asynchronous Sample Rate Converter (SRC)**

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 140 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

The S/PDIF and SRC are not available on the ADSP-21363 models.

### **Input Data Port (IDP)**

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive

audio channels in I2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I<sup>2</sup>S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

## Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of two units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A and B, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

## Peripheral Timers

The following three general-purpose timers can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

Each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

## I/O PROCESSOR FEATURES

The processor's I/O provides many channels of DMA and controls the extensive set of peripherals described in the previous sections.

## DMA Controller

The processor's on-chip DMA controllers allow data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP), or the parallel port (PP). See [Table 4](#).

**Table 4. DMA Channels**

| Peripheral         | ADSP-2136x |
|--------------------|------------|
| SPORTs             | 12         |
| IDP/PDAP           | 8          |
| SPI                | 2          |
| MTM/DTCP           | 2          |
| Parallel Port      | 1          |
| Total DMA Channels | 25         |

## SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

## Program Booting

The internal memory of the processor boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT\_CFG1–0) pins in [Table 5](#). Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

**Table 5. Boot Mode Selection**

| BOOT_CFG1–0 | Booting Mode                                                         |
|-------------|----------------------------------------------------------------------|
| 00          | SPI Slave Boot                                                       |
| 01          | SPI Master Boot                                                      |
| 10          | Parallel Port Boot via EPROM                                         |
| 11          | No booting occurs. Processor executes from internal ROM after reset. |

## Phase-Locked Loop

The processors use an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK\_CFG1–0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

## Power Supplies

The processor has a separate power supply connection for the internal (V<sub>DDINT</sub>), external (V<sub>DDEXT</sub>), and analog (A<sub>VDD</sub>/A<sub>VSS</sub>) power supplies. The internal and analog supplies must meet the 1.2 V requirement for K, B, and Y grade models, and the 1.0 V requirement for Y models. (For information on the temperature ranges offered for this product, see [Operating Conditions on Page 14](#), [Package Information on Page 16](#), and [Ordering Guide on Page 56](#).) The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A<sub>VDD</sub>) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A<sub>VDD</sub> pin. Place the filter components as close as possible to the A<sub>VDD</sub>/A<sub>VSS</sub> pins. For an example circuit, see [Figure 3](#). (A recommended ferrite chip is the muRata BLM18AG102SN1D.) To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V<sub>DDINT</sub> and GND. Use wide traces to connect the bypass capacitors to the analog power (A<sub>VDD</sub>) and ground (A<sub>VSS</sub>) pins. Note that the A<sub>VDD</sub> and A<sub>VSS</sub> pins specified in [Figure 3](#) are inputs to the processor and not the analog ground plane on the board—the A<sub>VSS</sub> pin should connect directly to digital ground (GND) at the chip.

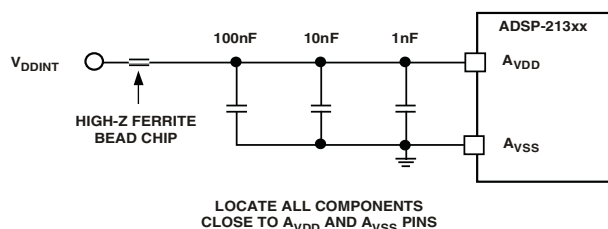


Figure 3. Analog Power ( $A_{VDD}$ ) Filter Circuit

## Target Board JTAG Emulator Connector

Analog Devices' DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processor to monitor and control the target board processor during emulation. Analog Devices' DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator does not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, refer to the appropriate emulator user's guide.

## DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

### Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit [www.analog.com/cces](http://www.analog.com/cces).

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit [www.analog.com/visualdsp](http://www.analog.com/visualdsp). Note that VisualDSP++ will not support future Analog Devices processors.

### EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development

features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit [www.analog.com](http://www.analog.com) and search on "ezkit" or "ezextender".

### EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

### Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

### Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

### Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- [www.analog.com/ucos3](http://www.analog.com/ucos3)
- [www.analog.com/ucfs](http://www.analog.com/ucfs)
- [www.analog.com/ucusb](http://www.analog.com/ucusb)
- [www.analog.com/lwip](http://www.analog.com/lwip)

### Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and

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VisualDSP++. For more information visit [www.analog.com](http://www.analog.com) and search on “Blackfin software modules” or “SHARC software modules”.

## **Designing an Emulator-Compatible DSP Board (Target)**

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note “*Analog Devices JTAG Emulation Technical Reference*” (EE-68) on the Analog Devices website ([www.analog.com](http://www.analog.com))—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

## **ADDITIONAL INFORMATION**

This data sheet provides a general overview of the processor’s architecture and functionality. For detailed information on the ADSP-2136x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Hardware Reference* and the *ADSP-2136x SHARC Processor Programming Reference*.

## **RELATED SIGNAL CHAINS**

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the “signal chain” entry in the [Glossary of EE Terms](#) on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the [www.analog.com](http://www.analog.com) website.

The Circuits from the Lab™ site (<http://www.analog.com/signalchains>) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

## PIN FUNCTION DESCRIPTIONS

The processor's pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS and TDI).

Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for  $\overline{\text{TRST}}$ ). Tie or pull unused inputs to  $V_{\text{DDEXT}}$  or GND, except for the following:

DAI\_Px, SPICLK, MISO, MOSI,  $\overline{\text{EMU}}$ , TMS,  $\overline{\text{TRST}}$ , TDI, and AD15–0. **Note:** These pins have pull-up resistors.

**Table 6. Pin Descriptions**

| Pin                                           | Type       | State During and After Reset          | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------|------------|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AD15–0                                        | I/O/T (pu) | Three-state with pull-up enabled      | <b>Parallel Port Address/Data.</b> The ADSP-2136x parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 k $\Omega$ internal pull-up resistor. For details about the AD pin operation, refer to the <i>ADSP-2136x SHARC Processor Hardware Reference</i> .<br>For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, ADDR23–8; ALE is used in conjunction with an external latch to retain the values of the ADDR23–8.<br>For detailed information on I/O operations and pin multiplexing, refer to the <i>ADSP-2136x SHARC Processor Hardware Reference</i> . |
| $\overline{\text{RD}}$                        | O (pu)     | Three-state, driven high <sup>1</sup> | <b>Parallel Port Read Enable.</b> $\overline{\text{RD}}$ is asserted low whenever the processor reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{RD}}$ has a 22.5 k $\Omega$ internal pull-up resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| $\overline{\text{WR}}$                        | O (pu)     | Three-state, driven high <sup>1</sup> | <b>Parallel Port Write Enable.</b> $\overline{\text{WR}}$ is asserted low whenever the processor writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted. $\overline{\text{WR}}$ has a 22.5 k $\Omega$ internal pull-up resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| ALE                                           | O (pd)     | Three-state, driven low <sup>1</sup>  | <b>Parallel Port Address Latch Enable.</b> ALE is asserted whenever the processor drives a new address on the parallel port address pins. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted. ALE has a 20 k $\Omega$ internal pull-down resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| FLAG[0]/ $\overline{\text{IRQ0}}$ /SPI FLG[0] | I/O        | FLAG[0] INPUT                         | <b>FLAG0/Interrupt Request0/SPI0 Slave Select.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| FLAG[1]/ $\overline{\text{IRQ1}}$ /SPI FLG[1] | I/O        | FLAG[1] INPUT                         | <b>FLAG1/Interrupt Request1/SPI1 Slave Select.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| FLAG[2]/ $\overline{\text{IRQ2}}$ /SPI FLG[2] | I/O        | FLAG[2] INPUT                         | <b>FLAG2/Interrupt Request 2/SPI2 Slave Select.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| FLAG[3]/TMREXP/SPIFLG[3]                      | I/O        | FLAG[3] INPUT                         | <b>FLAG3/Timer Expired/SPI3 Slave Select.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DAI_P20–1                                     | I/O/T (pu) | Three-state with programmable pull-up | <b>Digital Audio Interface Pins.</b> These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators and timers, sample rate converters and SPI to the DAI_P20–1 pins. These pins have internal 22.5 k $\Omega$ pull-up resistors that are enabled on reset. These pull-ups can be disabled using the DAI_PIN_PULLUP register.                                                            |

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, **(A/D)** = active drive, **(O/D)** = open drain, and **T** = three-state, **(pd)** = pull-down resistor, **(pu)** = pull-up resistor.

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Table 6. Pin Descriptions (Continued)

| Pin                       | Type           | State During and After Reset                                          | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------|----------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPICLK                    | I/O (pu)       | Three-state with pull-up enabled, driven high in SPI-master boot mode | <b>Serial Peripheral Interface Clock Signal.</b> Driven by the master, this signal controls the rate at which data is transferred. The master can transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (high). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 kΩ internal pull-up resistor.                                                                                                     |
| $\overline{\text{SPIDS}}$ | I              | Input only                                                            | <b>Serial Peripheral Interface Slave Device Select.</b> An active low signal used to select the processor as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode the processor's $\overline{\text{SPIDS}}$ signal can be driven by a slave device to signal to the processor (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to $V_{\text{DDEXT}}$ on the master device. For processor to processor SPI interaction, any of the master processor's flag pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the SPI slave device. |
| MOSI                      | I/O (O/D) (pu) | Three-state with pull-up enabled, driven low in SPI-master boot mode  | <b>SPI Master Out Slave In.</b> If the ADSP-2136x is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the processor is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 kΩ internal pull-up resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| MISO                      | I/O (O/D) (pu) | Three-state with pull-up enabled                                      | <b>SPI Master In Slave Out.</b> If the ADSP-2136x is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the processor is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 kΩ internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register.<br><b>Note:</b> Only one slave is allowed to transmit data at any given time. To enable broadcast transmission to multiple SPI slaves, the processor's MISO pin can be disabled by setting Bit 5 (DMISO) of the SPICTL register equal to 1.                                                                                                                    |
| CLKIN                     | I              | Input only                                                            | <b>Local Clock In.</b> Used in conjunction with XTAL. CLKIN is the ADSP-2136x clock input. It configures the ADSP-2136x to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLK_CFG1–0 pin settings. CLKIN should not be halted, changed, or operated below the specified frequency.                                                                                                                                                                                                                                                     |
| XTAL                      | O              | Output only <sup>2</sup>                                              | <b>Crystal Oscillator Terminal.</b> Used in conjunction with CLKIN to drive an external crystal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| CLK_CFG1–0                | I              | Input only                                                            | <b>Core to CLKIN Ratio Control.</b> These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are:<br>00 = 6:1<br>01 = 32:1<br>10 = 16:1<br>11 = reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

The following symbols appear in the Type column of Table 6: **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, (**A/D**) = active drive, (**O/D**) = open drain, and **T** = three-state, (**pd**) = pull-down resistor, (**pu**) = pull-up resistor.

**Table 6. Pin Descriptions (Continued)**

| Pin                                                          | Type            | State During and After Reset     | Function                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------------------------------------------------|-----------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BOOT_CFG1–0                                                  | I               | Input only                       | <b>Boot Configuration Select.</b> This pin is used to select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. For a description of the boot mode, refer to <a href="#">Table 5</a> , Boot Mode Selection.                                                                                                                                        |
| $\overline{\text{RESETOUT}}$<br>$\overline{\text{RESET}}$    | O<br>I/A        | Output only<br>Input only        | <b>Reset Out.</b> Drives out the core reset signal to an external device.<br><b>Processor Reset.</b> Resets the ADSP-2136x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up. |
| TCK                                                          | I               | Input only <sup>3</sup>          | <b>Test Clock (JTAG).</b> Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processors.                                                                                                                                                                                                                    |
| TMS                                                          | I/S<br>(pu)     | Three-state with pull-up enabled | <b>Test Mode Select (JTAG).</b> Used to control the test state machine. TMS has a 22.5 k $\Omega$ internal pull-up resistor.                                                                                                                                                                                                                                                               |
| TDI                                                          | I/S<br>(pu)     | Three-state with pull-up enabled | <b>Test Data Input (JTAG).</b> Provides serial data for the boundary scan logic. TDI has a 22.5 k $\Omega$ internal pull-up resistor.                                                                                                                                                                                                                                                      |
| TDO                                                          | O               | Three-state <sup>4</sup>         | <b>Test Data Output (JTAG).</b> Serial scan output of the boundary scan path.                                                                                                                                                                                                                                                                                                              |
| $\overline{\text{TRST}}$                                     | I/A<br>(pu)     | Three-state with pull-up enabled | <b>Test Reset (JTAG).</b> Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2136x. $\overline{\text{TRST}}$ has a 22.5 k $\Omega$ internal pull-up resistor.                                                                                                                               |
| $\overline{\text{EMU}}$                                      | O (O/D)<br>(pu) | Three-state with pull-up enabled | <b>Emulation Status.</b> Must be connected to the processor's JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 k $\Omega$ internal pull-up resistor.                                                                                                                                                                                                         |
| V <sub>DDINT</sub><br>V <sub>DDEXT</sub><br>A <sub>VDD</sub> | P<br>P<br>P     |                                  | <b>Core Power Supply.</b> Supplies the processor's core.<br><b>I/O Power Supply.</b><br><b>Analog Power Supply.</b> Supplies the processor's internal PLL (clock generator). This pin has the same specifications as V <sub>DDINT</sub> , except that added filtering circuitry is required. <a href="#">For more information, see Power Supplies on Page 8.</a>                           |
| A <sub>VSS</sub><br>GND                                      | G<br>G          |                                  | <b>Analog Power Supply Return.</b><br><b>Power Supply Return.</b>                                                                                                                                                                                                                                                                                                                          |

The following symbols appear in the Type column of [Table 6](#): **A** = asynchronous, **G** = ground, **I** = input, **O** = output, **P** = power supply, **S** = synchronous, **(A/D)** = active drive, **(O/D)** = open drain, and **T** = three-state, **(pd)** = pull-down resistor, **(pu)** = pull-up resistor.

<sup>1</sup>  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ , and ALE are three-stated (and not driven) only when  $\overline{\text{RESET}}$  is active.

<sup>2</sup> Output only is a three-state driver with its output path always enabled.

<sup>3</sup> Input only is a three-state driver with both output path and pull-up disabled.

<sup>4</sup> Three-state is a three-state driver with pull-up disabled.

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## SPECIFICATIONS

Specifications are subject to change without notice.

### OPERATING CONDITIONS

| Parameter                          | Description                                         | K Grade |     |                          | B Grade |     |                          | Y Grade |     |                          | Unit |
|------------------------------------|-----------------------------------------------------|---------|-----|--------------------------|---------|-----|--------------------------|---------|-----|--------------------------|------|
|                                    |                                                     | Min     | Nom | Max                      | Min     | Nom | Max                      | Min     | Nom | Max                      |      |
| V <sub>DDINT</sub>                 | Internal (Core) Supply Voltage                      | 1.14    | 1.2 | 1.26                     | 1.14    | 1.2 | 1.26                     | 0.95    | 1.0 | 1.05                     | V    |
| A <sub>VDD</sub>                   | Analog (PLL) Supply Voltage                         | 1.14    | 1.2 | 1.26                     | 1.14    | 1.2 | 1.26                     | 0.95    | 1.0 | 1.05                     | V    |
| V <sub>DDEXT</sub>                 | External (I/O) Supply Voltage                       | 3.13    | 3.3 | 3.47                     | 3.13    | 3.3 | 3.47                     | 3.13    | 3.3 | 3.47                     | V    |
| V <sub>IH</sub> <sup>1</sup>       | High Level Input Voltage @ V <sub>DDEXT</sub> = Max | 2.0     |     | V <sub>DDEXT</sub> + 0.5 | 2.0     |     | V <sub>DDEXT</sub> + 0.5 | 2.0     |     | V <sub>DDEXT</sub> + 0.5 | V    |
| V <sub>IL</sub> <sup>1</sup>       | Low Level Input Voltage @ V <sub>DDEXT</sub> = Min  | −0.5    |     | +0.8                     | −0.5    |     | +0.8                     | −0.5    |     | +0.8                     | V    |
| V <sub>IH_CLKIN</sub> <sup>2</sup> | High Level Input Voltage @ V <sub>DDEXT</sub> = Max | 1.74    |     | V <sub>DDEXT</sub> + 0.5 | 1.74    |     | V <sub>DDEXT</sub> + 0.5 | 1.74    |     | V <sub>DDEXT</sub> + 0.5 | V    |
| V <sub>IL_CLKIN</sub>              | Low Level Input Voltage @ V <sub>DDEXT</sub> = Min  | −0.5    |     | +1.19                    | −0.5    |     | +1.19                    | −0.5    |     | +1.19                    | V    |
| T <sub>J</sub> <sup>3, 4</sup>     | Junction Temperature 136-Ball CSP_BGA               | 0       |     | +110                     | −40     |     | +125                     | −40     |     | +125                     | °C   |
| T <sub>J</sub> <sup>3, 4</sup>     | Junction Temperature 144-Lead LQFP_EP               | 0       |     | +110                     | −40     |     | +125                     | −40     |     | +125                     | °C   |

<sup>1</sup>Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI\_Px, SPICLK, MOSI, MISO, SPIDS, BOOT\_CFGx, CLK\_CFGx, RESET, TCK, TMS, TDI, and TRST.

<sup>2</sup>Applies to input pin CLKIN.

<sup>3</sup>See [Thermal Characteristics on Page 47](#) for information on thermal specifications.

<sup>4</sup>See the Engineer-to-Engineer Note “*Estimating Power for the ADSP-21362 SHARC Processors*” (EE-277) for further information.

## ELECTRICAL CHARACTERISTICS

| Parameter            | Description                         | Test Conditions                                                                     | Min | Max | Unit          |
|----------------------|-------------------------------------|-------------------------------------------------------------------------------------|-----|-----|---------------|
| $V_{OH}^1$           | High Level Output Voltage           | @ $V_{DDEXT} = \text{Min}$ , $I_{OH} = -1.0 \text{ mA}^2$                           | 2.4 |     | V             |
| $V_{OL}^1$           | Low Level Output Voltage            | @ $V_{DDEXT} = \text{Min}$ , $I_{OL} = 1.0 \text{ mA}^2$                            |     | 0.4 | V             |
| $I_{IH}^{3,4}$       | High Level Input Current            | @ $V_{DDEXT} = \text{Max}$ , $V_{IN} = V_{DDEXT} \text{ Max}$                       |     | 10  | $\mu\text{A}$ |
| $I_{IL}^3$           | Low Level Input Current             | @ $V_{DDEXT} = \text{Max}$ , $V_{IN} = 0 \text{ V}$                                 |     | 10  | $\mu\text{A}$ |
| $I_{ILPU}^4$         | Low Level Input Current Pull-Up     | @ $V_{DDEXT} = \text{Max}$ , $V_{IN} = 0 \text{ V}$                                 |     | 200 | $\mu\text{A}$ |
| $I_{OZH}^{5,6}$      | Three-State Leakage Current         | @ $V_{DDEXT} = \text{Max}$ , $V_{IN} = V_{DDEXT} \text{ Max}$                       |     | 10  | $\mu\text{A}$ |
| $I_{OZL}^5$          | Three-State Leakage Current         | @ $V_{DDEXT} = \text{Max}$ , $V_{IN} = 0 \text{ V}$                                 |     | 10  | $\mu\text{A}$ |
| $I_{OZLPU}^6$        | Three-State Leakage Current Pull-Up | @ $V_{DDEXT} = \text{Max}$ , $V_{IN} = 0 \text{ V}$                                 |     | 200 | $\mu\text{A}$ |
| $I_{DD-INTYP}^{7,8}$ | Supply Current (Internal)           | $t_{CLK} = \text{Min}$ , $V_{DDINT} = \text{Nom}$                                   |     | 800 | mA            |
| $I_{AVDD}^9$         | Supply Current (Analog)             | $A_{VDD} = \text{Max}$                                                              |     | 10  | mA            |
| $C_{IN}^{10,11}$     | Input Capacitance                   | $f_{IN} = 1 \text{ MHz}$ , $T_{CASE} = 25^\circ\text{C}$ , $V_{IN} = 1.2 \text{ V}$ |     | 4.7 | pF            |

<sup>1</sup> Applies to output and bidirectional pins: AD15–0,  $\overline{RD}$ ,  $\overline{WR}$ , ALE, FLAG3–0, DAI\_Px, SPICLK, MOSI, MISO,  $\overline{EMU}$ , TDO, and XTAL.

<sup>2</sup> See [Output Drive Currents on Page 46](#) for typical drive current capabilities.

<sup>3</sup> Applies to input pins: SPIDS, BOOT\_CFGx, CLK\_CFGx, TCK, RESET, and CLKIN.

<sup>4</sup> Applies to input pins with 22.5 k $\Omega$  internal pull-ups:  $\overline{TRST}$ , TMS, TDI.

<sup>5</sup> Applies to three-stateable pins: FLAG3–0.

<sup>6</sup> Applies to three-stateable pins with 22.5 k $\Omega$  pull-ups: AD15–0, DAI\_Px, SPICLK,  $\overline{EMU}$ , MISO, and MOSI.

<sup>7</sup> Typical internal current data reflects nominal operating conditions.

<sup>8</sup> See the Engineer-to-Engineer Note “*Estimating Power for the ADSP-21362 SHARC Processors*” (EE-277) for further information.

<sup>9</sup> Characterized, but not tested.

<sup>10</sup> Applies to all signal pins.

<sup>11</sup> Guaranteed, but not tested.

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## PACKAGE INFORMATION

The information presented in [Figure 4](#) provides details about the package branding for the ADSP-2136x processor. For a complete listing of product availability, see [Ordering Guide on Page 56](#).



Figure 4. Typical Package Brand

Table 7. Package Brand Information

| Brand Key | Field Description          |
|-----------|----------------------------|
| t         | Temperature Range          |
| pp        | Package Type               |
| Z         | RoHS Compliant Designation |
| cc        | See Ordering Guide         |
| vvvvvv.x  | Assembly Lot Code          |
| n.n       | Silicon Revision           |
| #         | RoHS Compliant Designation |
| yyww      | Date Code                  |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## MAXIMUM POWER DISSIPATION

See the Engineer-to-Engineer Note “*Estimating Power for the ADSP-21362 SHARC Processors*” (EE-277) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see [Thermal Characteristics on Page 47](#).

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in [Table 8](#) may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of

this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

| Parameter                                      | Rating                        |
|------------------------------------------------|-------------------------------|
| Internal (Core) Supply Voltage ( $V_{DDINT}$ ) | –0.3 V to +1.5 V              |
| Analog (PLL) Supply Voltage ( $A_{VDD}$ )      | –0.3 V to +1.5 V              |
| External (I/O) Supply Voltage ( $V_{DDEXT}$ )  | –0.3 V to +4.6 V              |
| Input Voltage                                  | –0.5 V to +3.8 V              |
| Output Voltage Swing                           | –0.5 V to $V_{DDEXT} + 0.5$ V |
| Load Capacitance                               | 200 pF                        |
| Storage Temperature Range                      | –65°C to +150°C               |
| Junction Temperature While Biased              | 125°C                         |

## TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. For voltage reference levels, see [Figure 39 on Page 46](#) under [Test Conditions](#).

*Switching Characteristics* specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

*Timing Requirements* apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

## Core Clock Requirements

The processor’s internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor’s internal clock frequency and external (CLKIN) clock frequency with the CLK\_CFG1–0 pins.

The processor’s internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see [Figure 5](#)). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor’s internal clock.

## Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds  $f_{VCO}$  specified in [Table 11](#).

- The product of CLKIN and PLLM must never exceed  $\frac{1}{2} f_{VCO}(\text{max})$  in Table 11 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed  $f_{VCO}(\text{max})$  in Table 11 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$

$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLN)$$

where:

$f_{VCO}$  = VCO output

$PLLM$  = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK\_CFG pins in hardware.

$PLLN$  = 1, 2, 4, 8 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

$f_{INPUT}$  = Input frequency to the PLL.

$f_{INPUT}$  = CLKIN when the input divider is disabled or

$f_{INPUT} = \text{CLKIN} \div 2$  when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 9. All of the timing specifications for the ADSP-2136x peripherals are defined in relation to  $t_{PCLK}$ . Refer to the peripheral specific section for each peripheral's timing information.

**Table 9. Clock Periods**

| Timing Requirements | Description                                   |
|---------------------|-----------------------------------------------|
| $t_{CK}$            | CLKIN Clock Period                            |
| $t_{CCLK}$          | Processor Core Clock Period                   |
| $t_{PCLK}$          | Peripheral Clock Period = $2 \times t_{CCLK}$ |

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, refer to the ADSP-2136x SHARC Processor Hardware Reference.

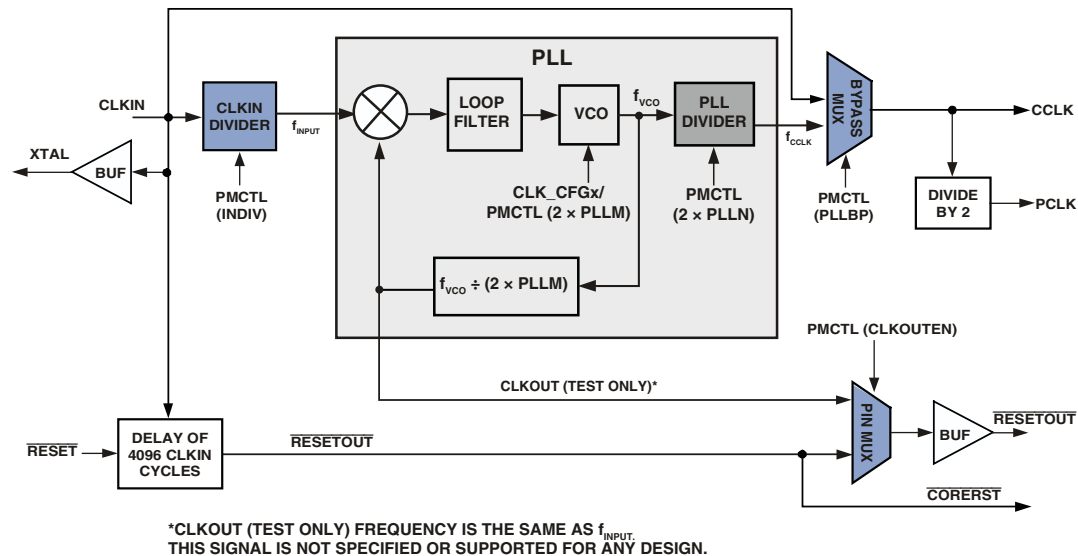


Figure 5. Core Clock and System Clock Relationship to CLKIN

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## Power-Up Sequencing

The timing requirements for processor startup are given in Table 10. Note that during power-up, when the  $V_{DDINT}$  power supply comes up after  $V_{DDEXT}$ , a leakage current of the order of

three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example the  $\overline{RESET}$  pin) until the  $V_{DDINT}$  rail has powered up.

**Table 10. Power-Up Sequencing Timing Requirements (Processor Startup)**

| Parameter                       |                                                           | Min                            | Max  | Unit    |
|---------------------------------|-----------------------------------------------------------|--------------------------------|------|---------|
| <i>Timing Requirements</i>      |                                                           |                                |      |         |
| $t_{RSTVDD}$                    | $\overline{RESET}$ Low Before $V_{DDINT}/V_{DDEXT}$ On    | 0                              |      | ns      |
| $t_{IVDDEVDD}$                  | $V_{DDINT}$ On Before $V_{DDEXT}$                         | -50                            | +200 | ms      |
| $t_{CLKVDD}^1$                  | CLKIN Valid After $V_{DDINT}/V_{DDEXT}$ Valid             | 0                              | 200  | ms      |
| $t_{CLKRST}$                    | CLKIN Valid Before $\overline{RESET}$ Deasserted          | $10^2$                         |      | $\mu s$ |
| $t_{PLLRST}$                    | PLL Control Setup Before $\overline{RESET}$ Deasserted    | 20                             |      | $\mu s$ |
| <i>Switching Characteristic</i> |                                                           |                                |      |         |
| $t_{CORERST}$                   | Core Reset Deasserted After $\overline{RESET}$ Deasserted | $4096t_{CK} + 2t_{CCLK}^{3,4}$ |      |         |

<sup>1</sup> Valid  $V_{DDINT}/V_{DDEXT}$  assumes that the supplies are fully ramped to their 1.2 V rails and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds, depending on the design of the power supply subsystem.

<sup>2</sup> Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

<sup>3</sup> Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for  $\overline{RESET}$  to be held low to properly initialize and propagate default states at all I/O pins.

<sup>4</sup> The 4096 cycle count depends on  $t_{SRST}$  specification in Table 12. If setup time is not met, 1 additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

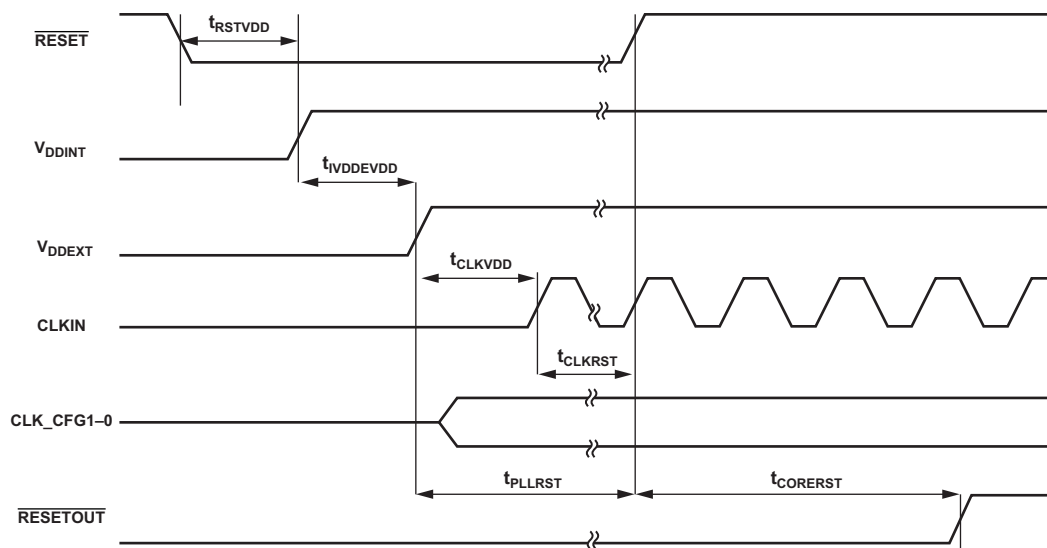


Figure 6. Power-Up Sequencing

## Clock Input

Table 11. Clock Input

| Parameter                       |                                  | 200 MHz <sup>1</sup> |      | 333 MHz <sup>2</sup> |      | Unit |
|---------------------------------|----------------------------------|----------------------|------|----------------------|------|------|
|                                 |                                  | Min                  | Max  | Min                  | Max  |      |
| Timing Requirements             |                                  |                      |      |                      |      |      |
| t <sub>CK</sub>                 | CLKIN Period                     | 30 <sup>3</sup>      | 100  | 18                   | 100  | ns   |
| t <sub>CKL</sub>                | CLKIN Width Low                  | 12.5                 |      | 7.5                  |      | ns   |
| t <sub>CKH</sub>                | CLKIN Width High                 | 12.5                 |      | 7.5                  |      | ns   |
| t <sub>CKRF</sub>               | CLKIN Rise/Fall (0.4 V to 2.0 V) |                      | 3    |                      | 3    | ns   |
| t <sub>CCLK</sub> <sup>4</sup>  | CCLK Period                      | 5.0                  | 10   | 3.0                  | 10   | ns   |
| t <sub>VCO</sub> <sup>5</sup>   | VCO Frequency                    | 200                  | 600  | 200                  | 800  | MHz  |
| t <sub>CKJ</sub> <sup>6,7</sup> | CLKIN Jitter Tolerance           | −250                 | +250 | −250                 | +250 | ps   |

<sup>1</sup> Applies to all 200 MHz models. See [Ordering Guide on Page 56](#).

<sup>2</sup> Applies to all 333 MHz models. See [Ordering Guide on Page 56](#).

<sup>3</sup> Applies only for CLK\_CFG1-0 = 00 and default values for PLL control bits in the PMCTL register.

<sup>4</sup> Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t<sub>CCLK</sub>.

<sup>5</sup> See [Figure 5 on Page 17](#) for VCO diagram.

<sup>6</sup> Actual input jitter should be combined with AC specifications for accurate timing analysis.

<sup>7</sup> Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

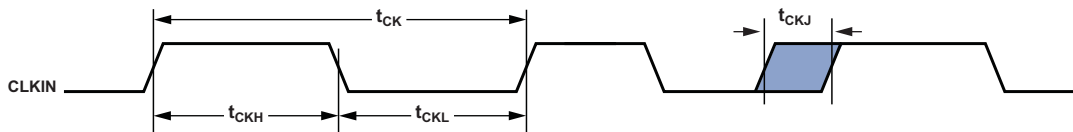


Figure 7. Clock Input

## Clock Signals

The processor can use an external clock or a crystal. Refer to the CLKIN pin description in [Table 6 on Page 11](#). The user application program can configure the processor to use its internal clock generator by connecting the necessary components to the CLKIN and XTAL pins. [Figure 8](#) shows the component connections used for a fundamental frequency crystal operating in parallel mode.

Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1. (CCLK:CLKIN achieves a clock speed of 266.72 MHz.) To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

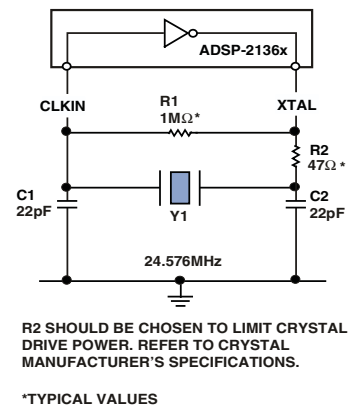


Figure 8. Recommended Circuit for Fundamental Mode Crystal Operation

Reset

Table 12. Reset

| Parameter           |                                           | Min               | Unit |
|---------------------|-------------------------------------------|-------------------|------|
| Timing Requirements |                                           |                   |      |
| $t_{WRST}^1$        | $\overline{RESET}$ Pulse Width Low        | $4 \times t_{CK}$ | ns   |
| $t_{SRST}$          | $\overline{RESET}$ Setup Before CLKIN Low | 8                 | ns   |

<sup>1</sup> Applies after the power-up sequence is complete. At power-up, the processor’s internal phase-locked loop requires no more than 100  $\mu$ s while  $\overline{RESET}$  is low, assuming stable  $V_{DD}$  and CLKIN (not including start-up time of external clock oscillator).

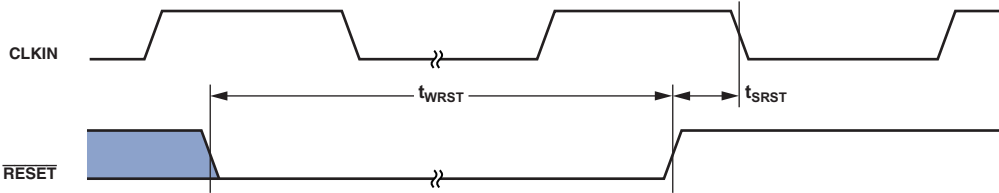


Figure 9. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as  $\overline{IRQ0}$ ,  $\overline{IRQ1}$ , and  $\overline{IRQ2}$  interrupts.

Table 13. Interrupts

| Parameter          |                               | Min                     | Unit |
|--------------------|-------------------------------|-------------------------|------|
| Timing Requirement |                               |                         |      |
| $t_{IPW}$          | $\overline{IRQx}$ Pulse Width | $2 \times t_{PCLK} + 2$ | ns   |

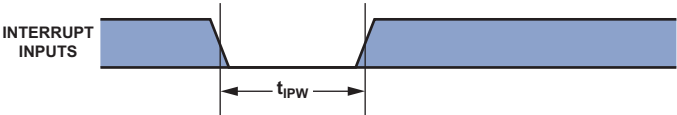


Figure 10. Interrupts

## Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP pin).

**Table 14. Core Timer**

| Parameter                       | Min                     | Unit |
|---------------------------------|-------------------------|------|
| <i>Switching Characteristic</i> |                         |      |
| $t_{WCTIM}$ TMREXP Pulse Width  | $2 \times t_{PCLK} - 1$ | ns   |

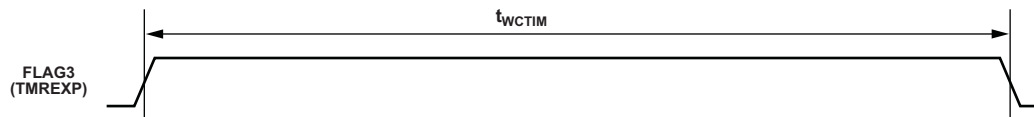


Figure 11. Core Timer

## Timer PWM\_OUT Cycle Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in PWM\_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI\_P20-1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI\_P20-1 pins.

**Table 15. Timer PWM\_OUT Timing**

| Parameter                           | Min                     | Max                                     | Unit |
|-------------------------------------|-------------------------|-----------------------------------------|------|
| <i>Switching Characteristic</i>     |                         |                                         |      |
| $t_{PWMO}$ Timer Pulse Width Output | $2 \times t_{PCLK} - 1$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns   |

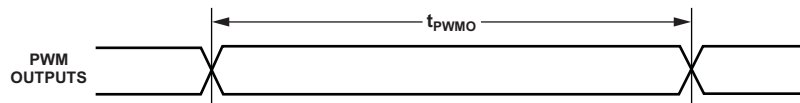


Figure 12. Timer PWM\_OUT Timing

Timer WDT<sub>H</sub>\_CAP Timing

The following timing specification applies to Timer0, Timer1, and Timer2 in WDT<sub>H</sub>\_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI\_P20-1 pins through the SRU. Therefore, the timing specification provided below are valid at the DAI\_P20-1 pins.

Table 16. Timer Width Capture Timing

| Parameter                          | Min                   | Max                                           | Unit |
|------------------------------------|-----------------------|-----------------------------------------------|------|
| Timing Requirement                 |                       |                                               |      |
| t <sub>PWI</sub> Timer Pulse Width | 2 × t <sub>PCLK</sub> | 2 × (2 <sup>31</sup> – 1) × t <sub>PCLK</sub> | ns   |

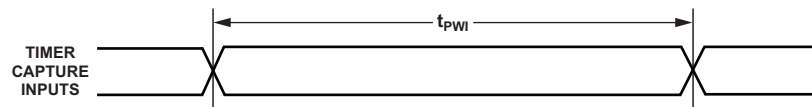


Figure 13. Timer Width Capture Timing

DAI Pin to Pin Direct Routing

For direct pin connections only (for example, DAI\_PB01\_I to DAI\_PB02\_O).

Table 17. DAI Pin to Pin Routing

| Parameter                                                       | Min | Max | Unit |
|-----------------------------------------------------------------|-----|-----|------|
| Timing Requirement                                              |     |     |      |
| t <sub>DPIO</sub> Delay DAI Pin Input Valid to DAI Output Valid | 1.5 | 10  | ns   |

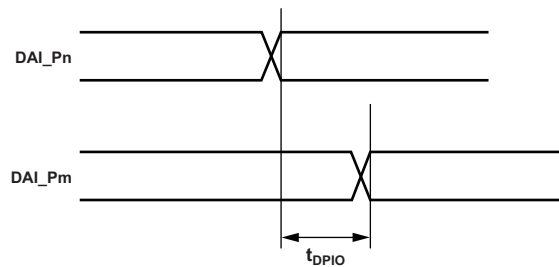


Figure 14. DAI Pin to Pin Direct Routing

## Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's

inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI\_P01 through DAI\_P20).

**Table 18. Precision Clock Generator (Direct Pin Routing)**

| Parameter                       |                                                                         | K and B Grade                                |                                             | Y Grade                                     | Unit |
|---------------------------------|-------------------------------------------------------------------------|----------------------------------------------|---------------------------------------------|---------------------------------------------|------|
|                                 |                                                                         | Min                                          | Max                                         | Max                                         |      |
| Timing Requirements             |                                                                         |                                              |                                             |                                             |      |
| t <sub>PCGIP</sub>              | Input Clock Period                                                      | t <sub>PCLK</sub> × 4                        |                                             |                                             | ns   |
| t <sub>STRIG</sub>              | PCG Trigger Setup Before Falling Edge of PCG Input Clock                | 4.5                                          |                                             |                                             | ns   |
| t <sub>HTRIG</sub>              | PCG Trigger Hold After Falling Edge of PCG Input Clock                  | 3                                            |                                             |                                             | ns   |
| Switching Characteristics       |                                                                         |                                              |                                             |                                             |      |
| t <sub>DPCGIO</sub>             | PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock | 2.5                                          | 10                                          | 10                                          | ns   |
| t <sub>DTRIGCLK</sub>           | PCG Output Clock Delay After PCG Trigger                                | 2.5 + (2.5 × t <sub>PCGIP</sub> )            | 10 + (2.5 × t <sub>PCGIP</sub> )            | 12 + (2.5 × t <sub>PCGIP</sub> )            | ns   |
| t <sub>DTRIGFS</sub>            | PCG Frame Sync Delay After PCG Trigger                                  | 2.5 + ((2.5 + D – PH) × t <sub>PCGIP</sub> ) | 10 + ((2.5 + D – PH) × t <sub>PCGIP</sub> ) | 12 + ((2.5 + D – PH) × t <sub>PCGIP</sub> ) | ns   |
| t <sub>PCGOP</sub> <sup>1</sup> | Output Clock Period                                                     | 2 × t <sub>PCGIP</sub> – 1                   |                                             |                                             | ns   |

D = FSxDIV, PH = FSxPHASE. For more information, refer to the ADSP-2136x SHARC Processor Hardware Reference, "Precision Clock Generators" chapter.

<sup>1</sup>In normal mode,  $t_{PCGOP}(\text{min}) = 2 \times t_{PCGIP}$ .

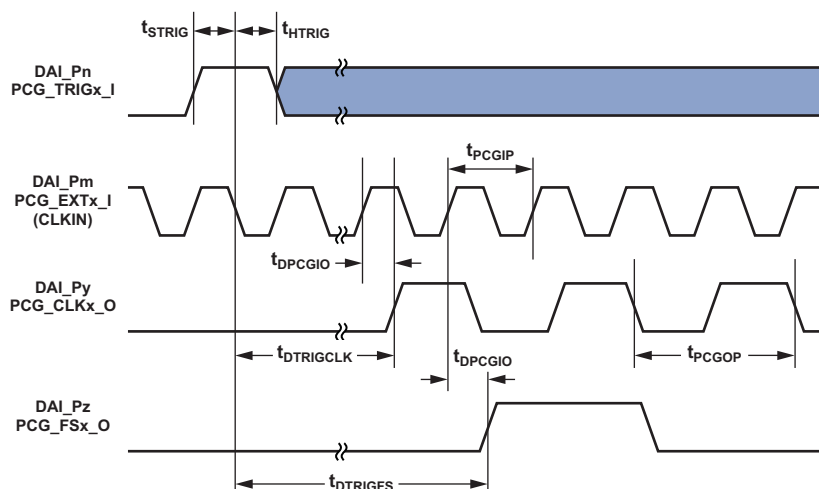


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3-0 and DAI\_P20-1 pins, the parallel port, and the serial peripheral interface (SPI). See Table 6 on Page 11 for more information on flag use.

Table 19. Flags

| Parameter                                           | Min            | Unit |
|-----------------------------------------------------|----------------|------|
| Timing Requirement                                  |                |      |
| t_FIPW                      FLAG3-0 IN Pulse Width  | 2 × t_PCLK + 3 | ns   |
| Switching Characteristic                            |                |      |
| t_FOPW                      FLAG3-0 OUT Pulse Width | 2 × t_PCLK - 1 | ns   |

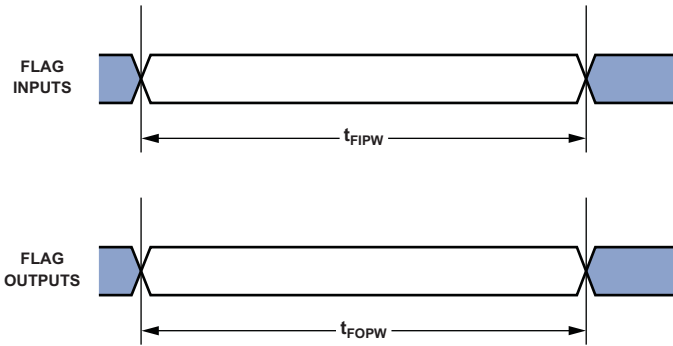


Figure 16. Flags

## Memory Read—Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

**Table 20. 8-Bit Memory Read Cycle**

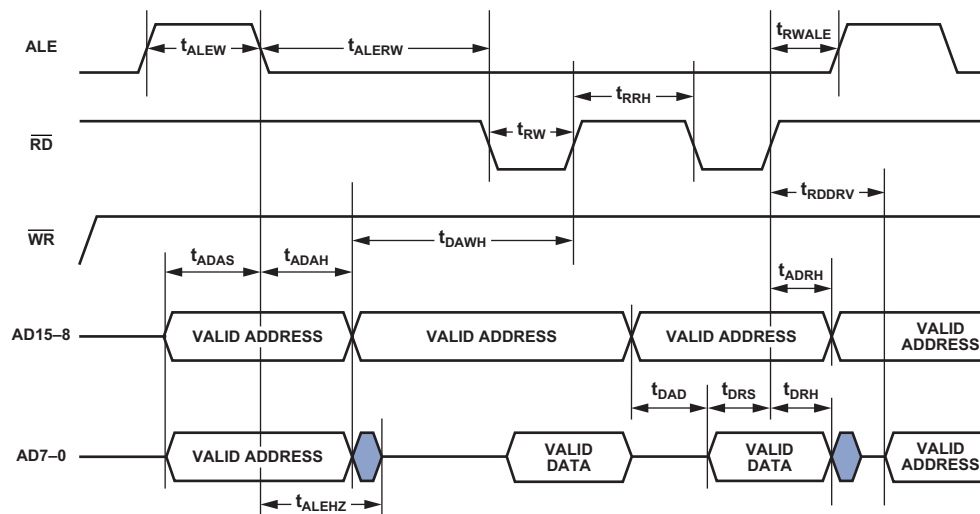
| Parameter                       |                                                                | K and B Grade                   |                             | Y Grade                         |                             | Unit |
|---------------------------------|----------------------------------------------------------------|---------------------------------|-----------------------------|---------------------------------|-----------------------------|------|
|                                 |                                                                | Min                             | Max                         | Min                             | Max                         |      |
| Timing Requirements             |                                                                |                                 |                             |                                 |                             |      |
| t <sub>DRS</sub>                | AD7–0 Data Setup Before $\overline{RD}$ High                   | 3.3                             |                             | 4.5                             |                             | ns   |
| t <sub>DRH</sub>                | AD7–0 Data Hold After $\overline{RD}$ High                     | 0                               |                             | 0                               |                             | ns   |
| t <sub>DAD</sub>                | AD15–8 Address to AD7–0 Data Valid                             |                                 | D + t <sub>PCLK</sub> – 5.0 |                                 | D + t <sub>PCLK</sub> – 5.0 | ns   |
| Switching Characteristics       |                                                                |                                 |                             |                                 |                             |      |
| t <sub>ALEW</sub>               | ALE Pulse Width                                                | 2 × t <sub>PCLK</sub> – 2.0     |                             | 2 × t <sub>PCLK</sub> – 2.0     |                             | ns   |
| t <sub>ADAS</sub> <sup>1</sup>  | AD15–0 Address Setup Before ALE Deasserted                     | t <sub>PCLK</sub> – 2.5         |                             | t <sub>PCLK</sub> – 2.5         |                             | ns   |
| t <sub>RRH</sub>                | Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge | H + t <sub>PCLK</sub> – 1.4     |                             | H + t <sub>PCLK</sub> – 1.4     |                             | ns   |
| t <sub>ALERW</sub>              | ALE Deasserted to Read Asserted                                | 2 × t <sub>PCLK</sub> – 3.8     |                             | 2 × t <sub>PCLK</sub> – 3.8     |                             | ns   |
| t <sub>RWALE</sub>              | Read Deasserted to ALE Asserted                                | F + H + 0.5                     |                             | F + H + 0.5                     |                             | ns   |
| t <sub>ADAH</sub> <sup>1</sup>  | AD15–0 Address Hold After ALE Deasserted                       | t <sub>PCLK</sub> – 2.3         |                             | t <sub>PCLK</sub> – 2.3         |                             | ns   |
| t <sub>ALEHZ</sub> <sup>1</sup> | ALE Deasserted to AD7–0 Address in High-Z                      | t <sub>PCLK</sub>               | t <sub>PCLK</sub> + 3.0     | t <sub>PCLK</sub>               | t <sub>PCLK</sub> + 3.8     | ns   |
| t <sub>RW</sub>                 | $\overline{RD}$ Pulse Width                                    | D – 2.0                         |                             | D – 2.0                         |                             | ns   |
| t <sub>RDDRV</sub>              | AD7–0 ALE Address Drive After Read High                        | F + H + t <sub>PCLK</sub> – 2.3 |                             | F + H + t <sub>PCLK</sub> – 2.3 |                             | ns   |
| t <sub>ADRH</sub>               | AD15–8 Address Hold After $\overline{RD}$ High                 | H                               |                             | H                               |                             | ns   |
| t <sub>DAWH</sub>               | AD15–8 Address to $\overline{RD}$ High                         | D + t <sub>PCLK</sub> – 4.0     |                             | D + t <sub>PCLK</sub> – 4.0     |                             | ns   |

$D = (\text{The value set by the PPDUR Bits (5–1) in the PPCTL register}) \times t_{PCLK}$

$H = t_{PCLK}$  (if a hold cycle is specified, else  $H = 0$ )

$F = 7 \times t_{PCLK}$  (if FLASH\_MODE is set, else  $F = 0$ )

<sup>1</sup> On reset, ALE is an active high cycle. However, it can be configured by software to be active low.



NOTE: MEMORY READS ALWAYS OCCUR IN GROUPS OF FOUR BETWEEN ALE CYCLES. THIS FIGURE SHOWS ONLY TWO MEMORY READS TO PROVIDE THE NECESSARY TIMING INFORMATION.

Figure 17. Read Cycle for 8-Bit Memory Timing

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

Table 21. 16-Bit Memory Read Cycle

| Parameter                      |                                                                | K and B Grade                   |                         | Y Grade                         |                         | Unit |
|--------------------------------|----------------------------------------------------------------|---------------------------------|-------------------------|---------------------------------|-------------------------|------|
|                                |                                                                | Min                             | Max                     | Min                             | Max                     |      |
| Timing Requirements            |                                                                |                                 |                         |                                 |                         |      |
| t <sub>DRS</sub>               | AD15–0 Data Setup Before $\overline{RD}$ High                  | 3.3                             |                         | 4.5                             |                         | ns   |
| t <sub>DRH</sub>               | AD15–0 Data Hold After $\overline{RD}$ High                    | 0                               |                         | 0                               |                         | ns   |
| Switching Characteristics      |                                                                |                                 |                         |                                 |                         |      |
| t <sub>ALEW</sub>              | ALE Pulse Width                                                | 2 × t <sub>PCLK</sub> – 2.0     |                         | 2 × t <sub>PCLK</sub> – 2.0     |                         | ns   |
| t <sub>ADAS</sub> <sup>1</sup> | AD15–0 Address Setup Before ALE Deasserted                     | t <sub>PCLK</sub> – 2.5         |                         | t <sub>PCLK</sub> – 2.5         |                         | ns   |
| t <sub>ALERW</sub>             | ALE Deasserted to Read Asserted                                | 2 × t <sub>PCLK</sub> – 3.8     |                         | 2 × t <sub>PCLK</sub> – 3.8     |                         | ns   |
| t <sub>RRH</sub> <sup>2</sup>  | Delay Between $\overline{RD}$ Rising Edge to Next Falling Edge | H + t <sub>PCLK</sub> – 1.4     |                         | H + t <sub>PCLK</sub> – 1.4     |                         | ns   |
| t <sub>RWALE</sub>             | Read Deasserted to ALE Asserted                                | F + H + 0.5                     |                         | F + H + 0.5                     |                         | ns   |
| t <sub>RDDRV</sub>             | ALE Address Drive After Read High                              | F + H + t <sub>PCLK</sub> – 2.3 |                         | F + H + t <sub>PCLK</sub> – 2.3 |                         | ns   |
| t <sub>ADAH</sub> <sup>1</sup> | AD15–0 Address Hold After ALE Deasserted                       | t <sub>PCLK</sub> – 2.3         |                         | t <sub>PCLK</sub> – 2.3         |                         | ns   |
| t <sub>ALEHZ1</sub>            | ALE Deasserted to Address/Data15–0 in High-Z                   | t <sub>PCLK</sub>               | t <sub>PCLK</sub> + 3.0 | t <sub>PCLK</sub>               | t <sub>PCLK</sub> + 3.8 | ns   |
| t <sub>RW</sub>                | $\overline{RD}$ Pulse Width                                    | D – 2.0                         |                         | D – 2.0                         |                         | ns   |

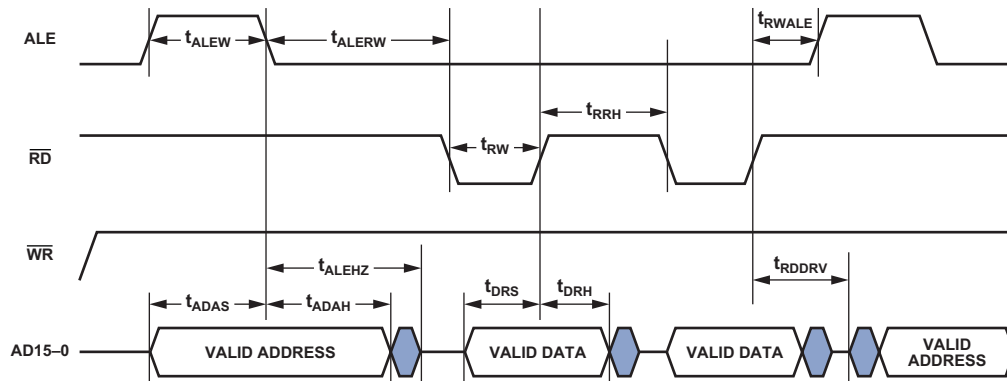
$D = (\text{The value set by the PPDUR Bits (5–1) in the PPCTL register}) \times t_{PCLK}$

$H = t_{PCLK}$  (if a hold cycle is specified, else  $H = 0$ )

$F = 7 \times t_{PCLK}$  (if FLASH\_MODE is set, else  $F = 0$ )

<sup>1</sup> On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

<sup>2</sup> This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY READS, WHEN EMPP  $\neq$  0, ONLY ONE  $\overline{RD}$  PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE  $\overline{RD}$  PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 18. Read Cycle for 16-Bit Memory Timing

## Memory Write—Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the processor is accessing external memory space.

**Table 22. 8-Bit Memory Write Cycle**

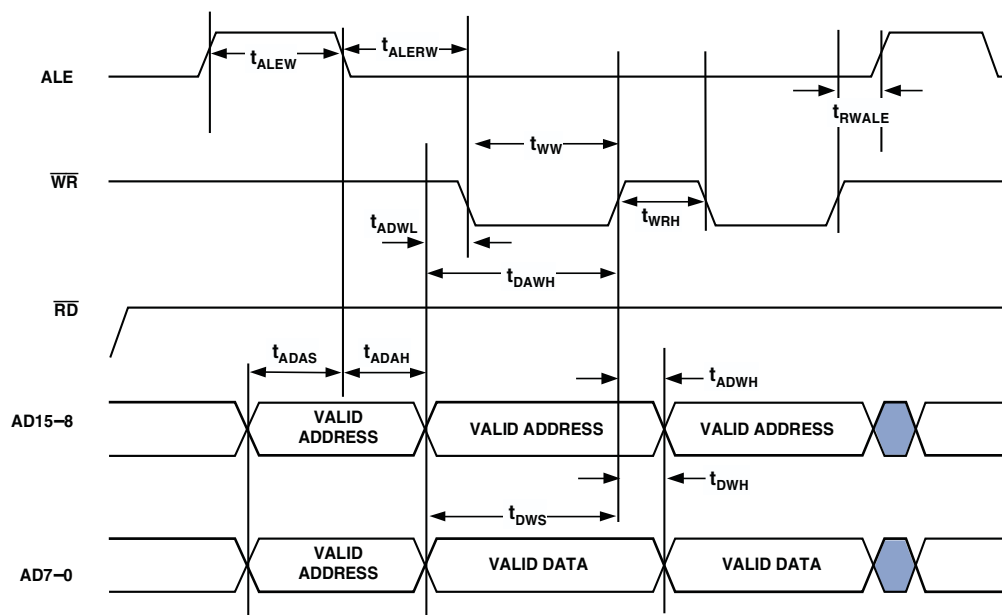
| Parameter                        |                                                                                | K and B Grade<br>Min      | Y Grade<br>Min            | Unit |
|----------------------------------|--------------------------------------------------------------------------------|---------------------------|---------------------------|------|
| <i>Switching Characteristics</i> |                                                                                |                           |                           |      |
| $t_{ALEW}$                       | ALE Pulse Width                                                                | $2 \times t_{PCLK} - 2.0$ | $2 \times t_{PCLK} - 2.0$ | ns   |
| $t_{ADAS}^1$                     | AD15–0 Address Setup Before ALE Deasserted                                     | $t_{PCLK} - 2.8$          | $t_{PCLK} - 2.8$          | ns   |
| $t_{ALERW}$                      | ALE Deasserted to Write Asserted                                               | $2 \times t_{PCLK} - 3.8$ | $2 \times t_{PCLK} - 3.8$ | ns   |
| $t_{RWALE}$                      | Write Deasserted to ALE Asserted                                               | H + 0.5                   | H + 0.5                   | ns   |
| $t_{WRH}$                        | Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge | $F + H + t_{PCLK} - 2.3$  | $F + H + t_{PCLK} - 2.3$  | ns   |
| $t_{ADAH}^1$                     | AD15–0 Address Hold After ALE Deasserted                                       | $t_{PCLK} - 0.5$          | $t_{PCLK} - 0.5$          | ns   |
| $t_{WW}$                         | $\overline{WR}$ Pulse Width                                                    | $D - F - 2.0$             | $D - F - 2.0$             | ns   |
| $t_{ADWL}$                       | AD15–8 Address to $\overline{WR}$ Low                                          | $t_{PCLK} - 2.8$          | $t_{PCLK} - 3.5$          | ns   |
| $t_{ADWH}$                       | AD15–8 Address Hold After $\overline{WR}$ High                                 | H                         | H                         | ns   |
| $t_{DWS}$                        | AD7–0 Data Setup Before $\overline{WR}$ High                                   | $D - F + t_{PCLK} - 4.0$  | $D - F + t_{PCLK} - 4.0$  | ns   |
| $t_{DWH}$                        | AD7–0 Data Hold After $\overline{WR}$ High                                     | H                         | H                         | ns   |
| $t_{DAWH}$                       | AD15–8 Address to $\overline{WR}$ High                                         | $D - F + t_{PCLK} - 4.0$  | $D - F + t_{PCLK} - 4.0$  | ns   |

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register)  $\times t_{PCLK}$ .

H =  $t_{PCLK}$  (if a hold cycle is specified, else H = 0)

F =  $7 \times t_{PCLK}$  (if FLASH\_MODE is set, else F = 0). If FLASH\_MODE is set, D must be  $\geq 9 \times t_{PCLK}$ .

<sup>1</sup> On reset, ALE is an active high cycle. However, it can be configured by software to be active low.



NOTE: MEMORY WRITES ALWAYS OCCUR IN GROUPS OF FOUR BETWEEN ALE CYCLES. THIS FIGURE SHOWS ONLY TWO MEMORY WRITES TO PROVIDE THE NECESSARY TIMING INFORMATION.

Figure 19. Write Cycle for 8-Bit Memory Timing

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

Table 23. 16-Bit Memory Write Cycle

| Parameter                      |                                                                                | K and B Grade                   | Y Grade                         | Unit |
|--------------------------------|--------------------------------------------------------------------------------|---------------------------------|---------------------------------|------|
|                                |                                                                                | Min                             | Min                             |      |
| Switching Characteristics      |                                                                                |                                 |                                 |      |
| t <sub>ALEW</sub>              | ALE Pulse Width                                                                | 2 × t <sub>PCLK</sub> – 2.0     | 2 × t <sub>PCLK</sub> – 2.0     | ns   |
| t <sub>ADAS</sub> <sup>1</sup> | AD15–0 Address Setup Before ALE Deasserted                                     | t <sub>PCLK</sub> – 2.5         | t <sub>PCLK</sub> – 2.5         | ns   |
| t <sub>ALERW</sub>             | ALE Deasserted to Write Asserted                                               | 2 × t <sub>PCLK</sub> – 3.8     | 2 × t <sub>PCLK</sub> – 3.8     | ns   |
| t <sub>RWALE</sub>             | Write Deasserted to ALE Asserted                                               | H + 0.5                         | H + 0.5                         | ns   |
| t <sub>WRH</sub> <sup>2</sup>  | Delay Between $\overline{WR}$ Rising Edge to Next $\overline{WR}$ Falling Edge | F + H + t <sub>PCLK</sub> – 2.3 | F + H + t <sub>PCLK</sub> – 2.3 | ns   |
| t <sub>ADAH</sub> <sup>1</sup> | AD15–0 Address Hold After ALE Deasserted                                       | t <sub>PCLK</sub> – 2.3         | t <sub>PCLK</sub> – 2.3         | ns   |
| t <sub>WW</sub>                | $\overline{WR}$ Pulse Width                                                    | D – F – 2.0                     | D – F – 2.0                     | ns   |
| t <sub>DWS</sub>               | AD15–0 Data Setup Before $\overline{WR}$ High                                  | D – F + t <sub>PCLK</sub> – 4.0 | D – F + t <sub>PCLK</sub> – 4.0 | ns   |
| t <sub>DWH</sub>               | AD15–0 Data Hold After $\overline{WR}$ High                                    | H                               | H                               | ns   |

$D = (\text{the value set by the PPDUR Bits (5–1) in the PPCTL register}) \times t_{PCLK}$ .

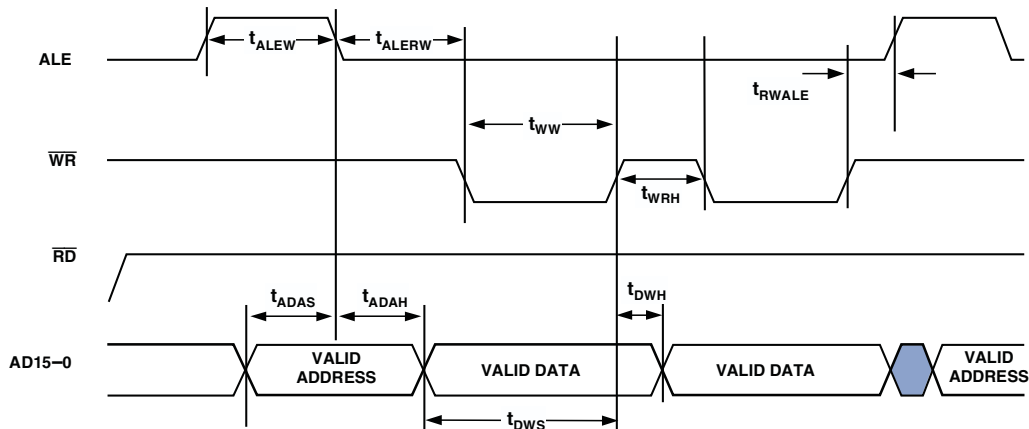
$H = t_{PCLK}$  (if a hold cycle is specified, else  $H = 0$ )

$F = 7 \times t_{PCLK}$  (if FLASH\_MODE is set, else  $F = 0$ ). If FLASH\_MODE is set, D must be  $\geq 9 \times t_{PCLK}$ .

$t_{PCLK} = (\text{peripheral}) \text{ clock period} = 2 \times t_{CCLK}$

<sup>1</sup>On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

<sup>2</sup>This parameter is only available when in EMPP = 0 mode.



NOTE: FOR 16-BIT MEMORY WRITES, WHEN EMPP  $\neq$  0, ONLY ONE  $\overline{WR}$  PULSE OCCURS BETWEEN ALE CYCLES. WHEN EMPP = 0, MULTIPLE  $\overline{WR}$  PULSES OCCUR BETWEEN ALE CYCLES. FOR COMPLETE INFORMATION, SEE THE ADSP-2136x SHARC PROCESSOR HARDWARE REFERENCE.

Figure 20. Write Cycle for 16-Bit Memory Timing

## Serial Ports

To determine whether communication is possible between two devices at clock speed  $n$ , the following specifications must be confirmed: 1) frame sync (FS) delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI\_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI\_P20–1 pins.

**Table 24. Serial Ports—External Clock**

| Parameter                       | K and B Grade                                                                                        |     | Y Grade                         | Unit |    |
|---------------------------------|------------------------------------------------------------------------------------------------------|-----|---------------------------------|------|----|
|                                 | Min                                                                                                  | Max | Max                             |      |    |
| Timing Requirements             |                                                                                                      |     |                                 |      |    |
| t <sub>SFSE</sub> <sup>1</sup>  | Frame Sync Setup Before SCLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode) |     | 2.5                             | ns   |    |
| t <sub>HFSE</sub> <sup>1</sup>  | Frame Sync Hold After SCLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode)   |     | 2.5                             | ns   |    |
| t <sub>SDRE</sub> <sup>1</sup>  | Receive Data Setup Before Receive SCLK                                                               |     | 2.5                             | ns   |    |
| t <sub>HDRE</sub> <sup>1</sup>  | Receive Data Hold After SCLK                                                                         |     | 2.5                             | ns   |    |
| t <sub>SCLKW</sub>              | SCLK Width                                                                                           |     | (t <sub>PCLK</sub> × 4) ÷ 2 – 2 | ns   |    |
| t <sub>SCLK</sub>               | SCLK Period                                                                                          |     | t <sub>PCLK</sub> × 4           | ns   |    |
| Switching Characteristics       |                                                                                                      |     |                                 |      |    |
| t <sub>DFSE</sub> <sup>2</sup>  | Frame Sync Delay After SCLK<br>(Internally Generated Frame Sync in Either Transmit or Receive Mode)  |     | 9.5                             | 11   | ns |
| t <sub>HOFSE</sub> <sup>2</sup> | Frame Sync Hold After SCLK<br>(Internally Generated Frame Sync in Either Transmit or Receive Mode)   |     | 2                               |      | ns |
| t <sub>DDTE</sub> <sup>2</sup>  | Transmit Data Delay After Transmit SCLK                                                              |     | 9.5                             | 11   | ns |
| t <sub>HDTE</sub> <sup>2</sup>  | Transmit Data Hold After Transmit SCLK                                                               |     | 2                               |      | ns |

<sup>1</sup>Referenced to sample edge.

<sup>2</sup>Referenced to drive edge.

**Table 25. Serial Ports—Internal Clock**

| Parameter                                                                                                                           | K and B Grade             |                           | Y Grade                   | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------|---------------------------|------|
|                                                                                                                                     | Min                       | Max                       | Max                       |      |
| Timing Requirements                                                                                                                 |                           |                           |                           |      |
| t <sub>SFSI</sub> <sup>1</sup> Frame Sync Setup Before SCLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode) | 7                         |                           |                           | ns   |
| t <sub>HFSI</sub> <sup>1</sup> Frame Sync Hold After SCLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode)   | 2.5                       |                           |                           | ns   |
| t <sub>SDRI</sub> <sup>1</sup> Receive Data Setup Before SCLK                                                                       | 7                         |                           |                           | ns   |
| t <sub>HDRI</sub> <sup>1</sup> Receive Data Hold After SCLK                                                                         | 2.5                       |                           |                           | ns   |
| Switching Characteristics                                                                                                           |                           |                           |                           |      |
| t <sub>DFSI</sub> <sup>2</sup> Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)                       |                           | 3                         | 3.5                       | ns   |
| t <sub>HOFSI</sub> <sup>2</sup> Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)                       | −1.0                      |                           |                           | ns   |
| t <sub>DFSIR</sub> <sup>2</sup> Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)                       |                           | 8                         | 9.5                       | ns   |
| t <sub>HOF SIR</sub> <sup>2</sup> Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)                      | −1.0                      |                           |                           | ns   |
| t <sub>DDTI</sub> <sup>2</sup> Transmit Data Delay After SCLK                                                                       |                           | 3                         | 4.0                       | ns   |
| t <sub>HDTI</sub> <sup>2</sup> Transmit Data Hold After SCLK                                                                        | −1.0                      |                           |                           | ns   |
| t <sub>SCLKIW</sub> Transmit or Receive SCLK Width                                                                                  | 2 × t <sub>PCLK</sub> − 2 | 2 × t <sub>PCLK</sub> + 2 | 2 × t <sub>PCLK</sub> + 2 | ns   |

<sup>1</sup>Referenced to the sample edge.

<sup>2</sup>Referenced to drive edge.

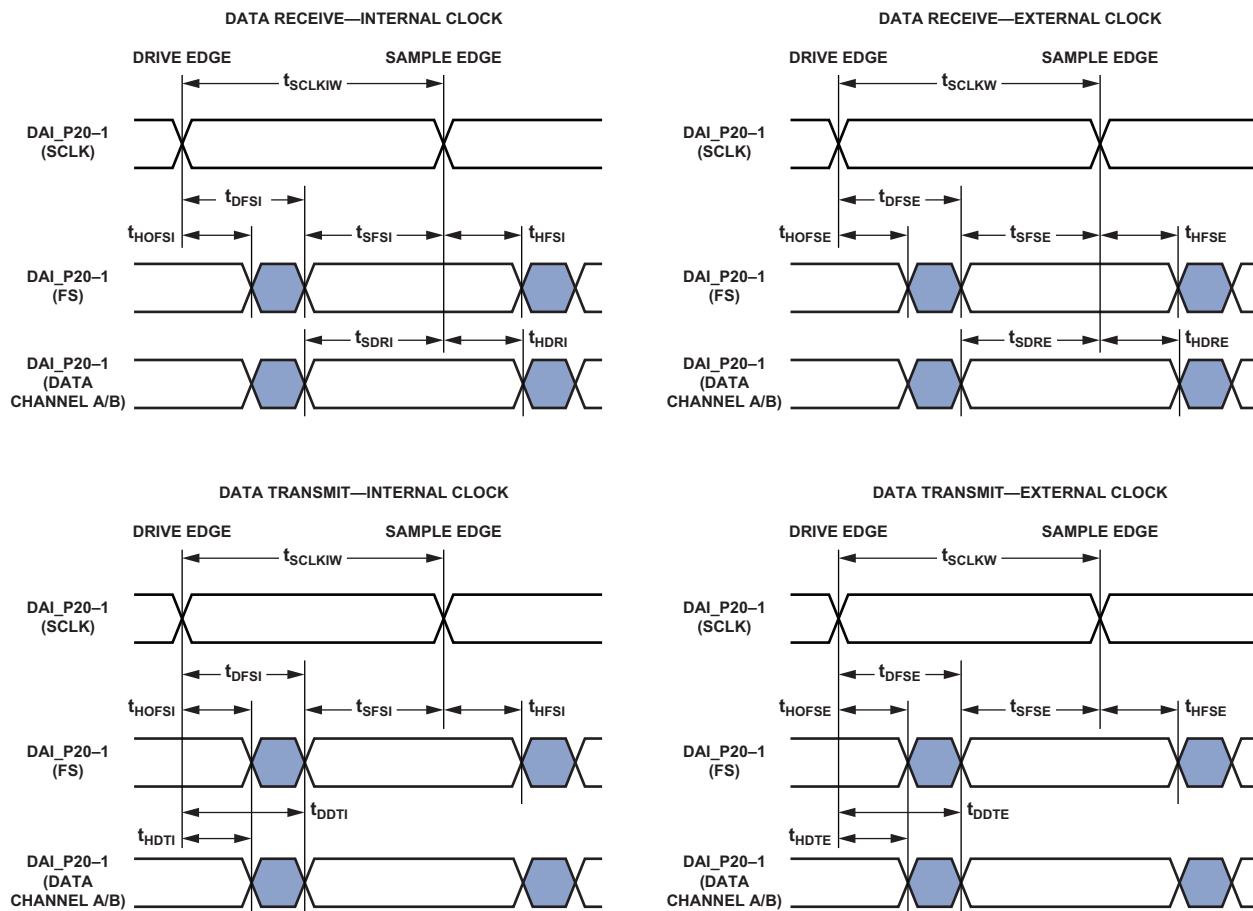


Figure 21. Serial Ports

**Table 26. Serial Ports—External Late Frame Sync**

| Parameter                                                                                                                        | Min | K and B Grade<br>Max | Y Grade<br>Max | Unit |
|----------------------------------------------------------------------------------------------------------------------------------|-----|----------------------|----------------|------|
| Switching Characteristics                                                                                                        |     |                      |                |      |
| t <sub>DDTLFSE</sub> <sup>1</sup> Data Delay from Late External Transmit Frame Sync or External Receive FS with MCE = 1, MFD = 0 |     | 9                    | 10.5           | ns   |
| t <sub>DDTENFS</sub> <sup>1</sup> Data Enable for MCE = 1, MFD = 0                                                               | 0.5 |                      |                | ns   |

<sup>1</sup>The  $t_{DDTLFSE}$  and  $t_{DDTENFS}$  parameters apply to left-justified sample pair as well as serial mode, and MCE = 1, MFD = 0.

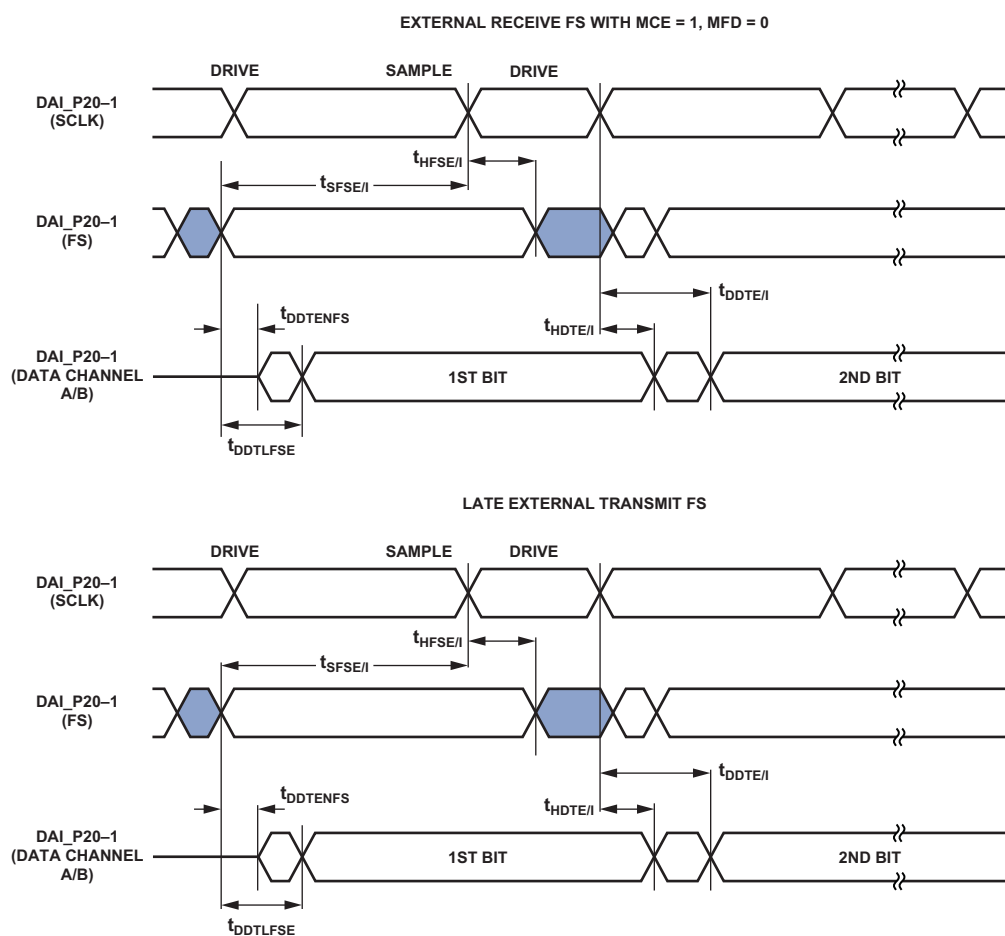


Figure 22. External Late Frame Sync

Table 27. Serial Ports—Enable and Three-State

| Parameter                       |                                          | K and B Grade |     | Y Grade | Unit |
|---------------------------------|------------------------------------------|---------------|-----|---------|------|
|                                 |                                          | Min           | Max | Max     |      |
| Switching Characteristics       |                                          |               |     |         |      |
| t <sub>DDTEN</sub> <sup>1</sup> | Data Enable from External Transmit SCLK  | 2             |     |         | ns   |
| t <sub>DDTTE</sub> <sup>1</sup> | Data Disable from External Transmit SCLK |               | 7   | 8.5     | ns   |
| t <sub>DDTIN</sub> <sup>1</sup> | Data Enable from Internal Transmit SCLK  | −1            |     |         | ns   |

<sup>1</sup>Referenced to drive edge.

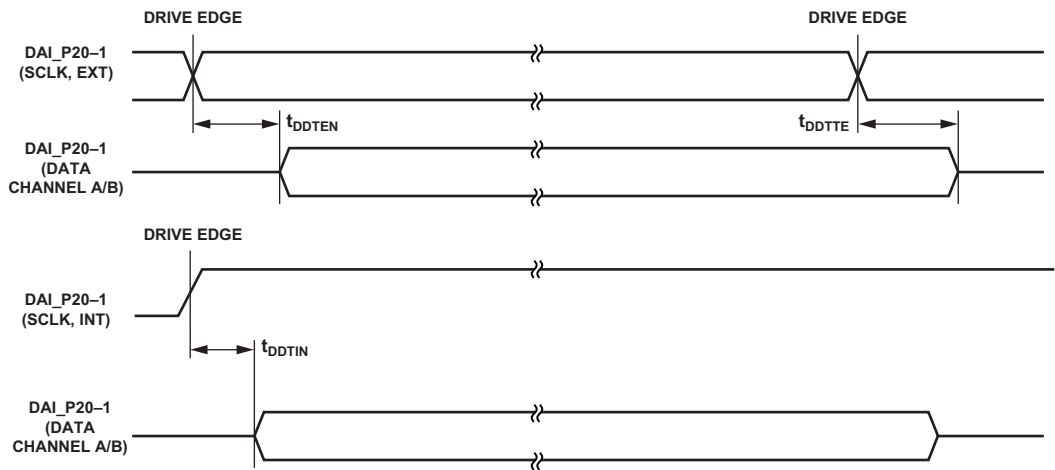


Figure 23. Enable and Three-State

## Input Data Port (IDP)

The timing requirements for the IDP are given in Table 28. IDP signals are routed to the DAI\_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI\_P20–1 pins.

**Table 28. IDP**

| Parameter                  |                                           | Min                              | Unit |
|----------------------------|-------------------------------------------|----------------------------------|------|
| <i>Timing Requirements</i> |                                           |                                  |      |
| $t_{SISFS}^1$              | Frame Sync Setup Before Clock Rising Edge | 3                                | ns   |
| $t_{SIHFS}^1$              | Frame Sync Hold After Clock Rising Edge   | 3                                | ns   |
| $t_{SISD}^1$               | Data Setup Before Clock Rising Edge       | 3                                | ns   |
| $t_{SIHD}^1$               | Data Hold After Clock Rising Edge         | 3                                | ns   |
| $t_{IDPCLKW}$              | Clock Width                               | $(t_{PCLK} \times 4) \div 2 - 1$ | ns   |
| $t_{IDPCLK}$               | Clock Period                              | $t_{PCLK} \times 4$              | ns   |

<sup>1</sup> The data, clock, and frame sync signals can come from any of the DAI pins. Clock and frame sync can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

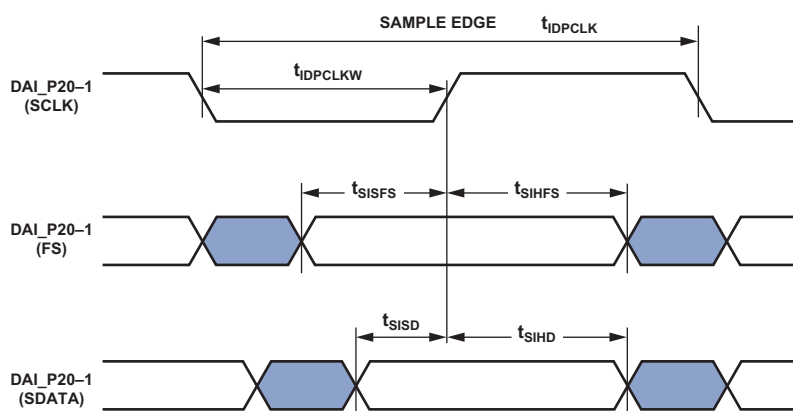


Figure 24. IDP Master Timing

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 29. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the IDP, refer to the *ADSP-2136x SHARC Processor Hardware Reference*, “Input Data Port” chapter.

Note that the most significant 16 bits of external 20-bit PDAP data can be provided through either the parallel port AD15–0 pins or the DAI\_P20–5 pins. The remaining 4 bits can only be sourced through DAI\_P4–1. The timing below is valid at the DAI\_P20–1 pins or at the AD15–0 pins.

**Table 29. Parallel Data Acquisition Port (PDAP)**

| Parameter                        |                                                                  | Min                              | Unit |
|----------------------------------|------------------------------------------------------------------|----------------------------------|------|
| <i>Timing Requirements</i>       |                                                                  |                                  |      |
| $t_{SPCLKEN}^1$                  | PDAP_CLKEN Setup Before PDAP_CLK Sample Edge                     | 2.5                              | ns   |
| $t_{HPCLKEN}^1$                  | PDAP_CLKEN Hold After PDAP_CLK Sample Edge                       | 2.5                              | ns   |
| $t_{PDSD}^1$                     | PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge                  | 3.0                              | ns   |
| $t_{PDHD}^1$                     | PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge                    | 2.5                              | ns   |
| $t_{PDCLKW}$                     | Clock Width                                                      | $(t_{PCLK} \times 4) \div 2 - 3$ | ns   |
| $t_{PDCLK}$                      | Clock Period                                                     | $t_{PCLK} \times 4$              | ns   |
| <i>Switching Characteristics</i> |                                                                  |                                  |      |
| $t_{PDHLDD}$                     | Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word | $2 \times t_{PCLK} - 1$          | ns   |
| $t_{PDSTRB}$                     | PDAP Strobe Pulse Width                                          | $2 \times t_{PCLK} - 1.5$        | ns   |

<sup>1</sup> Data source pins are AD15–0 and DAI\_P4–1, or DAI pins. Source pins for serial clock and frame sync are DAI pins.

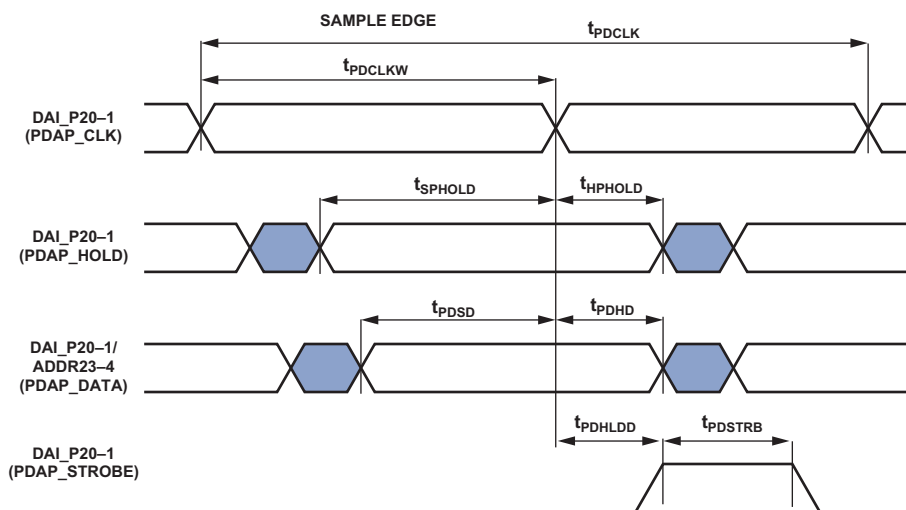


Figure 25. PDAP Timing

## Pulse-Width Modulation Generators

**Table 30. PWM Timing<sup>1</sup>**

| Parameter                                | Min                         | Max                                       | Unit |
|------------------------------------------|-----------------------------|-------------------------------------------|------|
| <i>Switching Characteristics</i>         |                             |                                           |      |
| t <sub>PWMW</sub> PWM Output Pulse Width | t <sub>PCLK</sub> – 2       | (2 <sup>16</sup> – 2) × t <sub>PCLK</sub> | ns   |
| t <sub>PWMP</sub> PWM Output Period      | 2 × t <sub>PCLK</sub> – 1.5 | (2 <sup>16</sup> – 1) × t <sub>PCLK</sub> | ns   |

<sup>1</sup> Note that the PWM output signals are shared on the parallel port bus (AD15-0 pins).

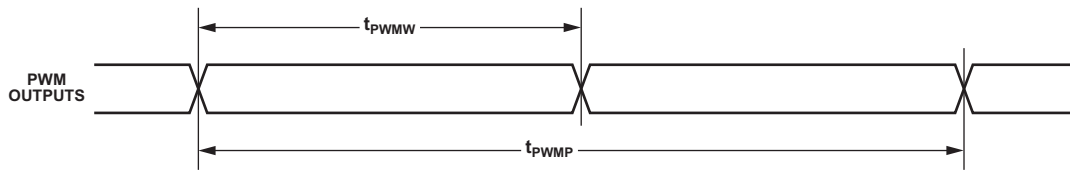


Figure 26. PWM Timing

## Sample Rate Converter—Serial Input Port

The SRC input signals are routed from the DAI\_P20–1 pins using the SRU. Therefore, the timing specifications provided in [Table 31](#) are valid at the DAI\_P20–1 pins. This feature is not available on the ADSP-21363 models.

**Table 31. SRC, Serial Input Port**

| Parameter                                                                         | Min | Unit |
|-----------------------------------------------------------------------------------|-----|------|
| <i>Timing Requirements</i>                                                        |     |      |
| t <sub>SRCSFS</sub> <sup>1</sup> Frame Sync Setup Before Serial Clock Rising Edge | 3   | ns   |
| t <sub>SRCHFS</sub> <sup>1</sup> Frame Sync Hold After Serial Clock Rising Edge   | 3   | ns   |
| t <sub>SRCS</sub> <sup>1</sup> SDATA Setup Before Serial Clock Rising Edge        | 3   | ns   |
| t <sub>SRCH</sub> <sup>1</sup> SDATA Hold After Serial Clock Rising Edge          | 3   | ns   |
| t <sub>SRCLKW</sub> Clock Width                                                   | 36  | ns   |
| t <sub>SRCLK</sub> Clock Period                                                   | 80  | ns   |

<sup>1</sup> The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via the PCGs or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

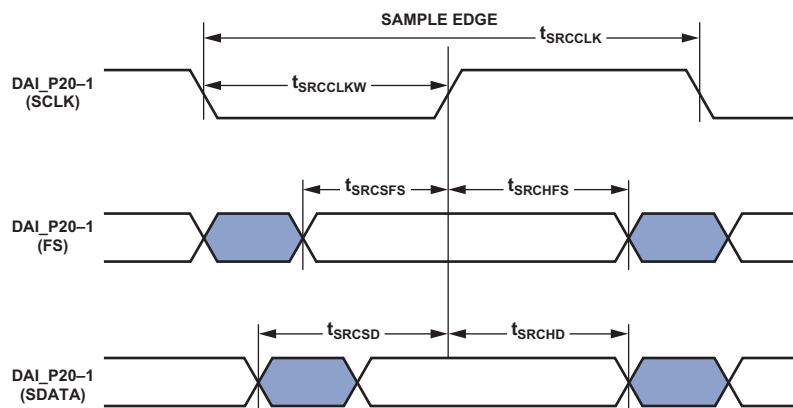


Figure 27. SRC Serial Input Port Timing

## Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and should meet setup and hold times with regard to the serial clock on the output port. The serial data output has a hold time and delay

specification with regard to serial clock. Note that the serial clock rising edge is the sampling edge and the falling edge is the drive edge.

**Table 32. SRC, Serial Output Port**

| Parameter                                                                | K and B Grade |      | Y Grade | Unit |
|--------------------------------------------------------------------------|---------------|------|---------|------|
|                                                                          | Min           | Max  | Max     |      |
| Timing Requirements                                                      |               |      |         |      |
| tSRCFS <sup>1</sup> Frame Sync Setup Before Serial Clock Rising Edge     | 3             |      |         | ns   |
| tSRCHFS <sup>1</sup> Frame Sync Hold After Serial Clock Rising Edge      | 3             |      |         | ns   |
| Switching Characteristics                                                |               |      |         |      |
| tSRCTDD <sup>1</sup> Transmit Data Delay After Serial Clock Falling Edge |               | 10.5 | 12.5    | ns   |
| tSRCTDH <sup>1</sup> Transmit Data Hold After Serial Clock Falling Edge  | 2             |      |         | ns   |

<sup>1</sup> The data, serial clock, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

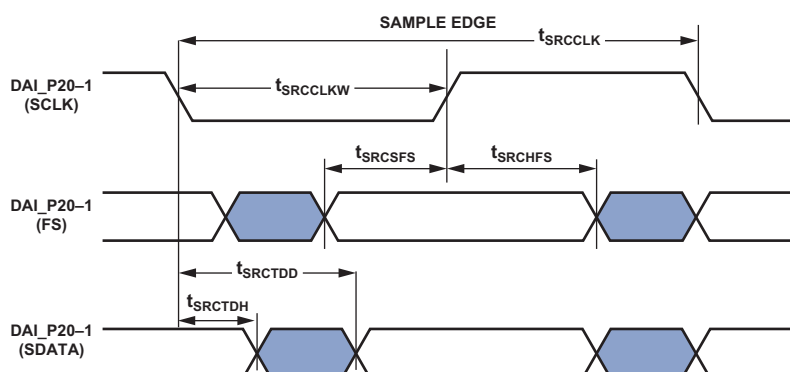


Figure 28. SRC Serial Output Port Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I<sup>2</sup>S, or right justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 29 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Table 33. S/PDIF Transmitter Right-Justified Mode

| Parameter          |                                         | Nominal | Unit |
|--------------------|-----------------------------------------|---------|------|
| Timing Requirement |                                         |         |      |
| t <sub>RJD</sub>   | FS to MSB Delay in Right-Justified Mode |         |      |
|                    | 16-Bit Word Mode                        | 16      | SCLK |
|                    | 18-Bit Word Mode                        | 14      | SCLK |
|                    | 20-Bit Word Mode                        | 12      | SCLK |
|                    | 24-Bit Word Mode                        | 8       | SCLK |

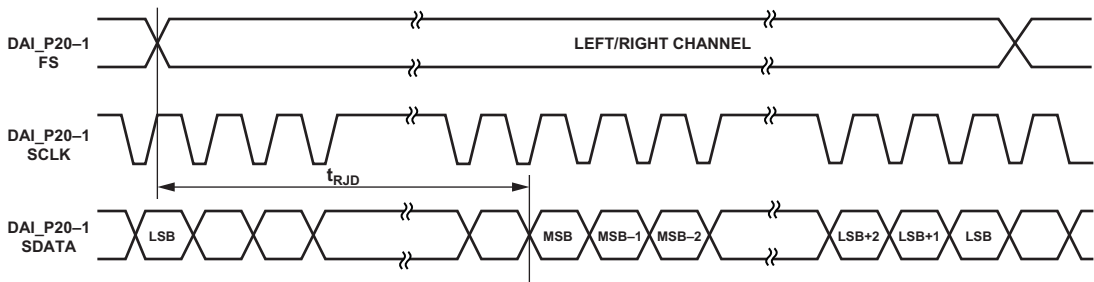


Figure 29. Right-Justified Mode

Figure 30 shows the default I<sup>2</sup>S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

**Table 34. S/PDIF Transmitter I<sup>2</sup>S Mode**

| Parameter                                           | Nominal | Unit |
|-----------------------------------------------------|---------|------|
| <i>Timing Requirement</i>                           |         |      |
| $t_{I2SD}$ FS to MSB Delay in I <sup>2</sup> S Mode | 1       | SCLK |

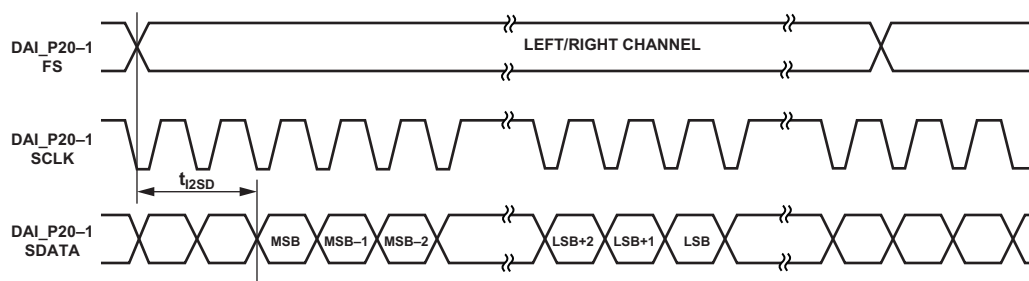


Figure 30. I<sup>2</sup>S-Justified Mode

Figure 31 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

**Table 35. S/PDIF Transmitter Left-Justified Mode**

| Parameter                                        | Nominal | Unit |
|--------------------------------------------------|---------|------|
| <i>Timing Requirement</i>                        |         |      |
| $t_{LJD}$ FS to MSB Delay in Left-Justified Mode | 0       | SCLK |

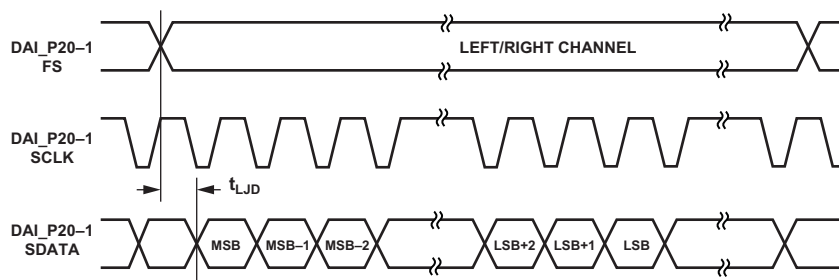


Figure 31. Left-Justified Mode

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 36. Input signals are routed to the DAI\_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI\_P20–1 pins.

**Table 36. S/PDIF Transmitter Input Data Timing**

| Parameter                       |                                                  | K Grade |     | Y Grade |     | Unit |
|---------------------------------|--------------------------------------------------|---------|-----|---------|-----|------|
|                                 |                                                  | Min     | Max | Min     | Max |      |
| Timing Requirements             |                                                  |         |     |         |     |      |
| t <sub>SISFS</sub> <sup>1</sup> | Frame Sync Setup Before Serial Clock Rising Edge | 3       |     | 3       |     | ns   |
| t <sub>SIHFS</sub> <sup>1</sup> | Frame Sync Hold After Serial Clock Rising Edge   | 3       |     | 3       |     | ns   |
| t <sub>SISD</sub> <sup>1</sup>  | Data Setup Before Serial Clock Rising Edge       | 3       |     | 3       |     | ns   |
| t <sub>SIHD</sub> <sup>1</sup>  | Data Hold After Serial Clock Rising Edge         | 3       |     | 3       |     | ns   |
| t <sub>SITXCLKW</sub>           | Transmit Clock Width                             | 9       |     | 9.5     |     | ns   |
| t <sub>SITXCLK</sub>            | Transmit Clock Period                            | 20      |     | 20      |     | ns   |
| t <sub>SISCLKW</sub>            | Clock Width                                      | 36      |     | 36      |     | ns   |
| t <sub>SISCLK</sub>             | Clock Period                                     | 80      |     | 80      |     | ns   |

<sup>1</sup> The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

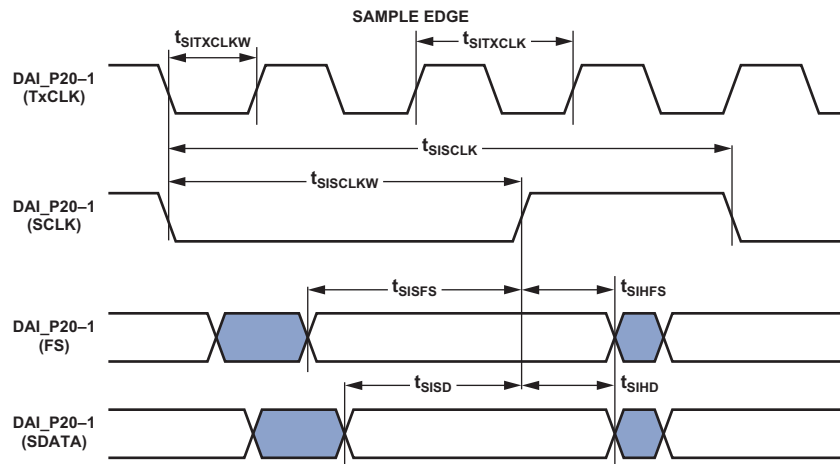


Figure 32. S/PDIF Transmitter Input Timing

## Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

**Table 37. Oversampling Clock (TxCLK) Switching Characteristics**

| Parameter                                     | Max                                                         | Unit |
|-----------------------------------------------|-------------------------------------------------------------|------|
| Frequency for TxCLK = $384 \times$ Frame Sync | Oversampling Ratio $\times$ Frame Sync $\leq 1/t_{SITXCLK}$ | MHz  |
| Frequency for TxCLK = $256 \times$ Frame Sync | 49.2                                                        | MHz  |
| Frame Rate (FS)                               | 192.0                                                       | kHz  |

## S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver. This feature is not available on the ADSP-21363 processors.

### Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the  $512 \times FS$  clock.

**Table 38. S/PDIF Receiver Output Timing (Internal Digital PLL Mode)**

| Parameter                        |                                        | Min | Max | Unit |
|----------------------------------|----------------------------------------|-----|-----|------|
| <i>Switching Characteristics</i> |                                        |     |     |      |
| $t_{DFSI}$                       | Frame Sync Delay After Serial Clock    |     | 5   | ns   |
| $t_{HOFSI}$                      | Frame Sync Hold After Serial Clock     | -2  |     | ns   |
| $t_{DDTI}$                       | Transmit Data Delay After Serial Clock |     | 5   | ns   |
| $t_{HDTI}$                       | Transmit Data Hold After Serial Clock  | -2  |     | ns   |
| $t_{SCLKIW}^1$                   | Transmit Serial Clock Width            | 38  |     | ns   |

<sup>1</sup> Serial clock frequency is  $64 \times FS$  where  $FS$  = the frequency of frame sync.

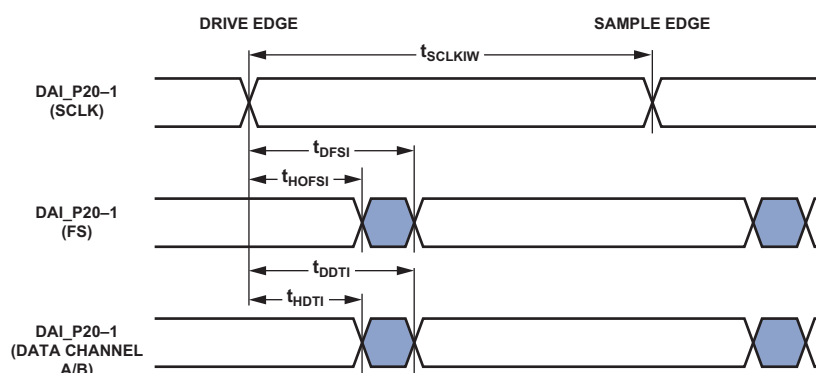


Figure 33. S/PDIF Receiver Internal Digital PLL Mode Timing

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## SPI Interface—Master

The processor contains two SPI ports. The primary has dedicated pins and the secondary is available through the DAI. The timing provided in Table 39 and Table 40 applies to both ports.

**Table 39. SPI Interface Protocol—Master Switching and Timing Specifications**

| Parameter                 |                                                                | K and B Grade               |     | Y Grade                     |     | Unit |
|---------------------------|----------------------------------------------------------------|-----------------------------|-----|-----------------------------|-----|------|
|                           |                                                                | Min                         | Max | Min                         | Max |      |
| Timing Requirements       |                                                                |                             |     |                             |     |      |
| t <sub>SSPIDM</sub>       | Data Input Valid to SPICLK Edge (Data Input Setup Time)        | 5.2                         |     | 6.2                         |     | ns   |
| t <sub>SSPIDM</sub>       | Data Input Valid to SPICLK Edge (Data Input Setup Time) (SPI2) | 8.2                         |     | 9.5                         |     | ns   |
| t <sub>HSPIDM</sub>       | SPICLK Last Sampling Edge to Data Input Not Valid              | 2                           |     | 2                           |     | ns   |
| Switching Characteristics |                                                                |                             |     |                             |     |      |
| t <sub>SPICLKM</sub>      | Serial Clock Cycle                                             | 8 × t <sub>PCLK</sub> – 2   |     | 8 × t <sub>PCLK</sub> – 2   |     | ns   |
| t <sub>SPICHM</sub>       | Serial Clock High Period                                       | 4 × t <sub>PCLK</sub> – 2   |     | 4 × t <sub>PCLK</sub> – 2   |     | ns   |
| t <sub>SPICLM</sub>       | Serial Clock Low Period                                        | 4 × t <sub>PCLK</sub> – 2   |     | 4 × t <sub>PCLK</sub> – 2   |     | ns   |
| t <sub>DDSPIDM</sub>      | SPICLK Edge to Data Out Valid (Data Out Delay Time)            |                             | 3.0 |                             | 3.0 | ns   |
| t <sub>DDSPIDM</sub>      | SPICLK Edge to Data Out Valid (Data Out Delay Time) (SPI2)     |                             | 8.0 |                             | 9.5 | ns   |
| t <sub>HDSPIDM</sub>      | SPICLK Edge to Data Out Not Valid (Data Out Hold Time)         | 4 × t <sub>PCLK</sub> – 2   |     | 4 × t <sub>PCLK</sub> – 2   |     | ns   |
| t <sub>SDSCIM</sub>       | FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge         | 4 × t <sub>PCLK</sub> – 2.5 |     | 4 × t <sub>PCLK</sub> – 3.0 |     | ns   |
| t <sub>SDSCIM</sub>       | FLAG3–0IN (SPI Device Select) Low to First SPICLK Edge (SPI2)  | 4 × t <sub>PCLK</sub> – 2.5 |     | 4 × t <sub>PCLK</sub> – 3.0 |     | ns   |
| t <sub>HDSM</sub>         | Last SPICLK Edge to FLAG3–0IN High                             | 4 × t <sub>PCLK</sub> – 2   |     | 4 × t <sub>PCLK</sub> – 2   |     | ns   |
| t <sub>SPITDM</sub>       | Sequential Transfer Delay                                      | 4 × t <sub>PCLK</sub> – 1   |     | 4 × t <sub>PCLK</sub> – 1   |     | ns   |

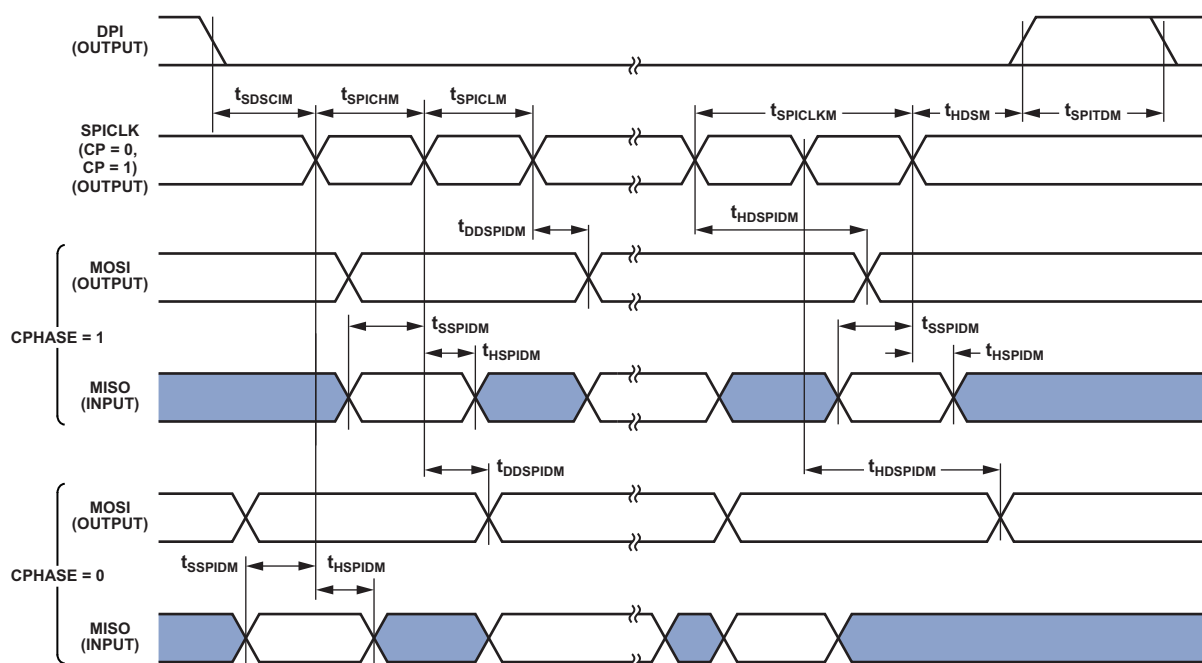


Figure 34. SPI Master Timing

## SPI Interface—Slave

**Table 40. SPI Interface Protocol—Slave Switching and Timing Specifications**

| Parameter                 |                                                         | K and B Grade |           | Y Grade   | Unit |
|---------------------------|---------------------------------------------------------|---------------|-----------|-----------|------|
|                           |                                                         | Min           | Max       | Max       |      |
| Timing Requirements       |                                                         |               |           |           |      |
| tSPICKS                   | Serial Clock Cycle                                      | 4 × tPCLK – 2 |           |           | ns   |
| tSPICH                    | Serial Clock High Period                                | 2 × tPCLK – 2 |           |           | ns   |
| tSPICL                    | Serial Clock Low Period                                 | 2 × tPCLK – 2 |           |           | ns   |
| tSDSCO                    | SPIDS Assertion to First SPICLK Edge                    |               |           |           |      |
|                           | CPHASE = 0                                              | 2 × tPCLK     |           |           | ns   |
|                           | CPHASE = 1                                              | 2 × tPCLK     |           |           | ns   |
| tHDS                      | Last SPICLK Edge to SPIDS Not Asserted, CPHASE = 0      | 2 × tPCLK     |           |           | ns   |
| tSSPIDS                   | Data Input Valid to SPICLK Edge (Data Input Setup Time) | 2             |           |           | ns   |
| tHSPIDS                   | SPICLK Last Sampling Edge to Data Input Not Valid       | 2             |           |           | ns   |
| tSDPPW                    | SPIDS Deassertion Pulse Width (CPHASE = 0)              | 2 × tPCLK     |           |           | ns   |
| Switching Characteristics |                                                         |               |           |           |      |
| tDSOE                     | SPIDS Assertion to Data Out Active                      | 0             | 5         | 5         | ns   |
| tDSOE <sup>1</sup>        | SPIDS Assertion to Data Out Active (SPI2)               | 0             | 8         | 9         | ns   |
| tDSDHI                    | SPIDS Deassertion to Data High Impedance                | 0             | 5         | 5.5       | ns   |
| tDSDHI <sup>1</sup>       | SPIDS Deassertion to Data High Impedance (SPI2)         | 0             | 8.6       | 10        | ns   |
| tDDSPIDS                  | SPICLK Edge to Data Out Valid (Data Out Delay Time)     |               | 9.5       | 11.0      | ns   |
| tHDSPIDS                  | SPICLK Edge to Data Out Not Valid (Data Out Hold Time)  | 2 × tPCLK     |           |           | ns   |
| tDSOV                     | SPIDS Assertion to Data Out Valid (CPHASE = 0)          |               | 5 × tPCLK | 5 × tPCLK | ns   |

<sup>1</sup>The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, refer to the ADSP-2136x SHARC Processor Hardware Reference, “Serial Peripheral Interface Port” chapter.

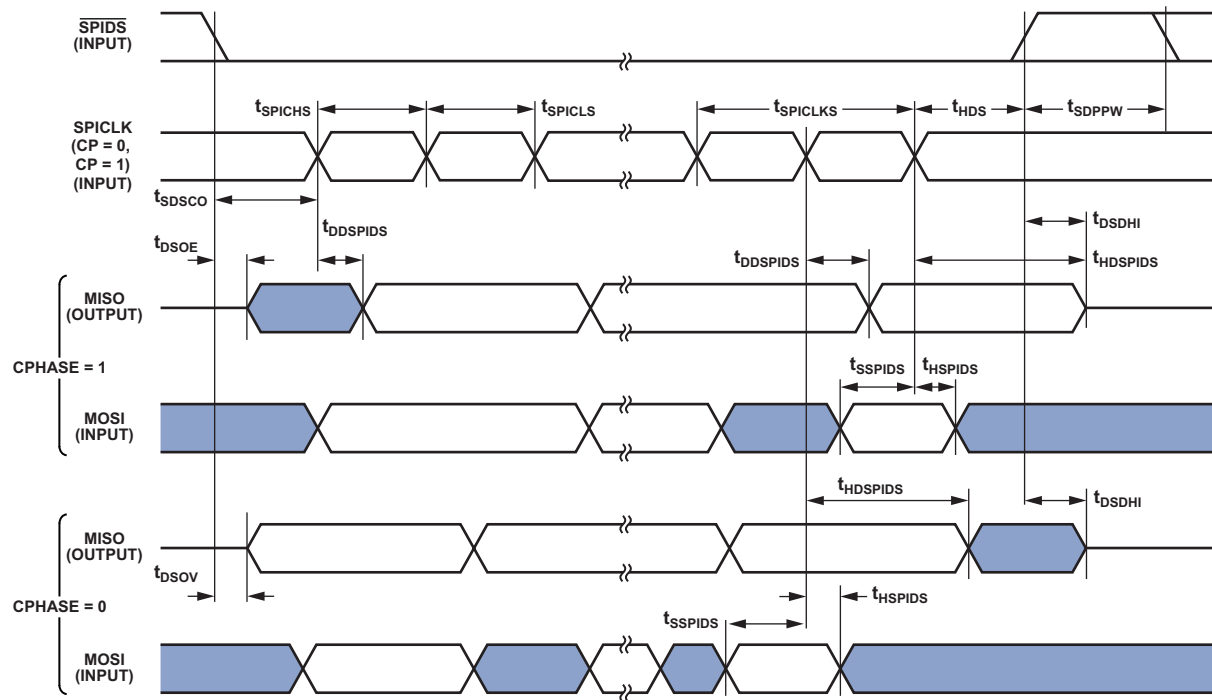


Figure 35. SPI Slave Timing

## JTAG Test Access Port and Emulation

**Table 41. JTAG Test Access Port and Emulation**

| Parameter                        |                                     | Min               | Max                 | Unit |
|----------------------------------|-------------------------------------|-------------------|---------------------|------|
| <i>Timing Requirements</i>       |                                     |                   |                     |      |
| $t_{TCK}$                        | TCK Period                          | $t_{CK}$          |                     | ns   |
| $t_{STAP}$                       | TDI, TMS Setup Before TCK High      | 5                 |                     | ns   |
| $t_{HTAP}$                       | TDI, TMS Hold After TCK High        | 6                 |                     | ns   |
| $t_{SSYS}^1$                     | System Inputs Setup Before TCK High | 7                 |                     | ns   |
| $t_{HSYS}^1$                     | System Inputs Hold After TCK High   | 18                |                     | ns   |
| $t_{TRSTW}$                      | $\overline{TRST}$ Pulse Width       | $4 \times t_{CK}$ |                     | ns   |
| <i>Switching Characteristics</i> |                                     |                   |                     |      |
| $t_{DTDO}$                       | TDO Delay from TCK Low              |                   | 7                   | ns   |
| $t_{DSYS}^2$                     | System Outputs Delay After TCK Low  |                   | $t_{CK} \div 2 + 7$ | ns   |

<sup>1</sup>System Inputs = ADDR15–0,  $\overline{SPIDS}$ , CLK\_CFG1–0,  $\overline{RESET}$ , BOOT\_CFG1–0, MISO, MOSI, SPICLK, DAI\_Px, and FLAG3–0.

<sup>2</sup>System Outputs = MISO, MOSI, SPICLK, DAI\_Px, ADDR15–0,  $\overline{RD}$ ,  $\overline{WR}$ , FLAG3–0,  $\overline{EMU}$ , and ALE.

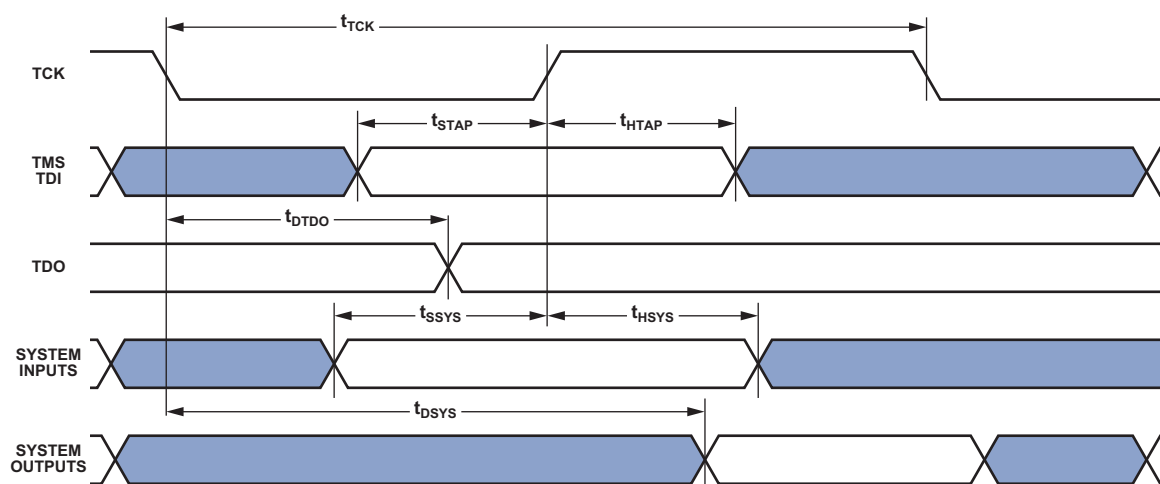


Figure 36. IEEE 1149.1 JTAG Test Access Port

## OUTPUT DRIVE CURRENTS

Figure 37 shows typical I-V characteristics for the output drivers of the processor. The curves represent the current drive capability of the output drivers as a function of output voltage.

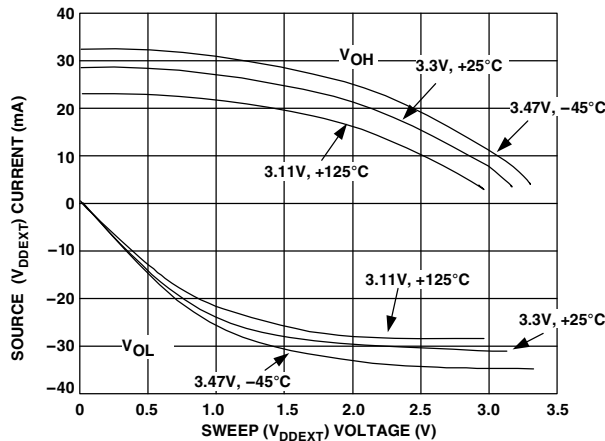


Figure 37. ADSP-2136x Typical Drive

## TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 12 on Page 20 through Table 41 on Page 45. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 38.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

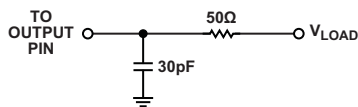


Figure 38. Equivalent Device Loading for AC Measurements  
(Includes All Fixtures)

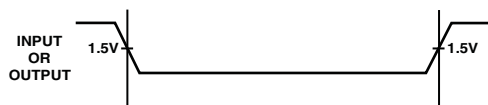


Figure 39. Voltage Reference Levels for AC Measurements

## CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 38). Figure 42 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 40, Figure 41, and Figure 42 may not be linear outside the ranges shown for Typical Output Delay versus Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) versus Load Capacitance.

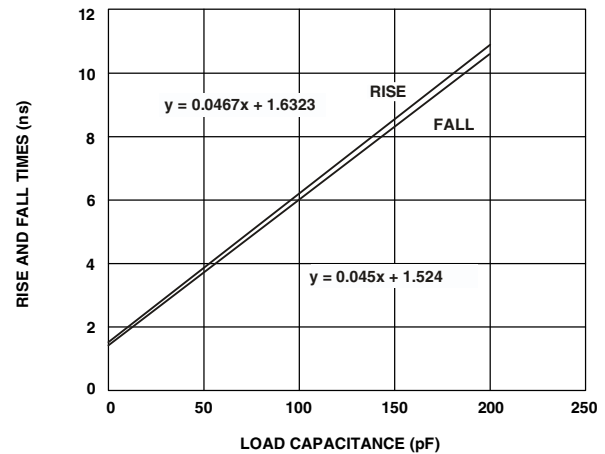


Figure 40. Typical Output Rise/Fall Time  
(20% to 80%,  $V_{DDEXT} = \text{Max}$ )

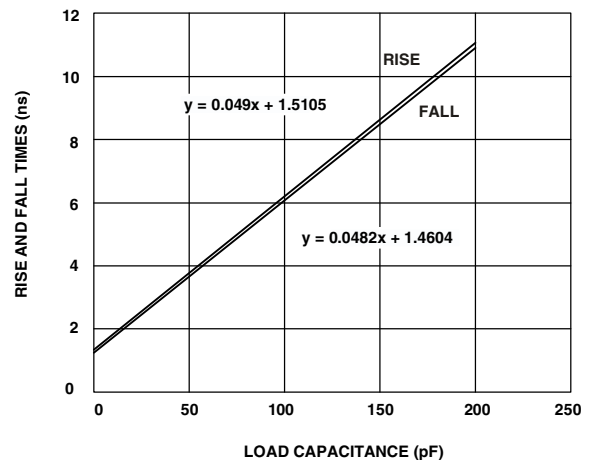


Figure 41. Typical Output Rise/Fall Time  
(20% to 80%,  $V_{DDEXT} = \text{Min}$ )

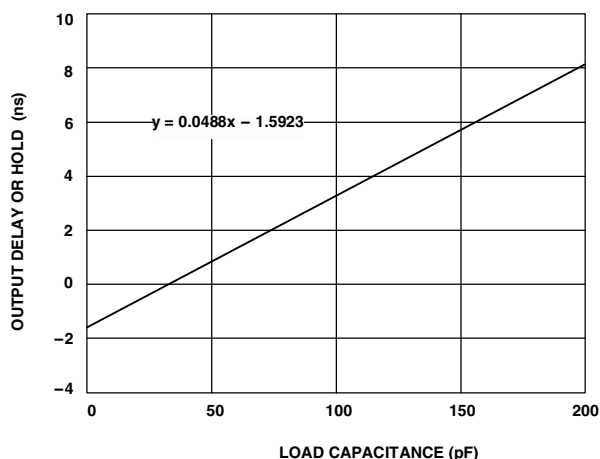


Figure 42. Typical Output Delay or Hold versus Load Capacitance (at Ambient Temperature)

## THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 14.

Table 42 through Table 44 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board and thermal via design comply with JEDEC standards JESD51-9 (BGA) and JESD51-5 (LQFP\_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

Industrial applications using the BGA package require thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Industrial applications using the LQFP\_EP package require thermal trace squares and thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-5 for more information.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$  = junction temperature (°C)

$T_T$  = case temperature (°C) measured at the top center of the package

$\Psi_{JT}$  = junction-to-top (of package) characterization parameter is the typical value from Table 42 through Table 44.

$P_D$  = power dissipation. See the Engineer-to-Engineer Note "Estimating Power for the ADSP-21362 SHARC Processors" (EE-277) for more information.

Values of  $\theta_{JA}$  are provided for package comparison and PCB design considerations.

Values of  $\theta_{JC}$  are provided for package comparison and PCB design considerations when an exposed pad is required. Note that the thermal characteristics values provided in Table 42 through Table 44 are modeled values.

Table 42. Thermal Characteristics for BGA (No Thermal vias in PCB)

| Parameter      | Condition       | Typical | Unit |
|----------------|-----------------|---------|------|
| $\theta_{JA}$  | Airflow = 0 m/s | 25.40   | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 21.90   | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 20.90   | °C/W |
| $\theta_{JC}$  |                 | 5.07    | °C/W |
| $\Psi_{JT}$    | Airflow = 0 m/s | 0.140   | °C/W |
| $\Psi_{JMT}$   | Airflow = 1 m/s | 0.330   | °C/W |
| $\Psi_{JMT}$   | Airflow = 2 m/s | 0.410   | °C/W |

Table 43. Thermal Characteristics for BGA (Thermal vias in PCB)

| Parameter      | Condition       | Typical | Unit |
|----------------|-----------------|---------|------|
| $\theta_{JA}$  | Airflow = 0 m/s | 23.40   | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 20.00   | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 19.20   | °C/W |
| $\theta_{JC}$  |                 | 5.00    | °C/W |
| $\Psi_{JT}$    | Airflow = 0 m/s | 0.130   | °C/W |
| $\Psi_{JMT}$   | Airflow = 1 m/s | 0.300   | °C/W |
| $\Psi_{JMT}$   | Airflow = 2 m/s | 0.360   | °C/W |

Table 44. Thermal Characteristics for LQFP\_EP (with Exposed Pad Soldered to PCB)

| Parameter      | Condition       | Typical | Unit |
|----------------|-----------------|---------|------|
| $\theta_{JA}$  | Airflow = 0 m/s | 16.80   | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 14.20   | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 13.50   | °C/W |
| $\theta_{JC}$  |                 | 7.25    | °C/W |
| $\Psi_{JT}$    | Airflow = 0 m/s | 0.51    | °C/W |
| $\Psi_{JMT}$   | Airflow = 1 m/s | 0.72    | °C/W |
| $\Psi_{JMT}$   | Airflow = 2 m/s | 0.80    | °C/W |

## 144-LEAD LQFP\_EP PIN CONFIGURATIONS

The following table shows the processor's pin names and, when applicable, their default function after reset in parentheses.

**Table 45. LQFP\_EP Pin Assignments**

| Pin Name               | Pin No. | Pin Name               | Pin No. | Pin Name           | Pin No. | Pin Name                             | Pin No. |
|------------------------|---------|------------------------|---------|--------------------|---------|--------------------------------------|---------|
| V <sub>DDINT</sub>     | 1       | V <sub>DDINT</sub>     | 37      | V <sub>DDEXT</sub> | 73      | GND                                  | 109     |
| CLK_CFG0               | 2       | GND                    | 38      | GND                | 74      | V <sub>DDINT</sub>                   | 110     |
| CLK_CFG1               | 3       | $\overline{\text{RD}}$ | 39      | V <sub>DDINT</sub> | 75      | GND                                  | 111     |
| BOOT_CFG0              | 4       | ALE                    | 40      | GND                | 76      | V <sub>DDINT</sub>                   | 112     |
| BOOT_CFG1              | 5       | AD15                   | 41      | DAI_P10 (SD2B)     | 77      | GND                                  | 113     |
| GND                    | 6       | AD14                   | 42      | DAI_P11 (SD3A)     | 78      | V <sub>DDINT</sub>                   | 114     |
| V <sub>DDEXT</sub>     | 7       | AD13                   | 43      | DAI_P12 (SD3B)     | 79      | GND                                  | 115     |
| GND                    | 8       | GND                    | 44      | DAI_P13 (SCLK3)    | 80      | V <sub>DDEXT</sub>                   | 116     |
| V <sub>DDINT</sub>     | 9       | V <sub>DDEXT</sub>     | 45      | DAI_P14 (SFS3)     | 81      | GND                                  | 117     |
| GND                    | 10      | AD12                   | 46      | DAI_P15 (SD4A)     | 82      | V <sub>DDINT</sub>                   | 118     |
| V <sub>DDINT</sub>     | 11      | V <sub>DDINT</sub>     | 47      | V <sub>DDINT</sub> | 83      | GND                                  | 119     |
| GND                    | 12      | GND                    | 48      | GND                | 84      | V <sub>DDINT</sub>                   | 120     |
| V <sub>DDINT</sub>     | 13      | AD11                   | 49      | GND                | 85      | $\overline{\text{RESET}}$            | 121     |
| GND                    | 14      | AD10                   | 50      | DAI_P16 (SD4B)     | 86      | $\overline{\text{SPID\overline{S}}}$ | 122     |
| FLAG0                  | 15      | AD9                    | 51      | DAI_P17 (SD5A)     | 87      | GND                                  | 123     |
| FLAG1                  | 16      | AD8                    | 52      | DAI_P18 (SD5B)     | 88      | V <sub>DDINT</sub>                   | 124     |
| AD7                    | 17      | DAI_P1 (SD0A)          | 53      | DAI_P19 (SCLK5)    | 89      | SPICKL                               | 125     |
| GND                    | 18      | V <sub>DDINT</sub>     | 54      | V <sub>DDINT</sub> | 90      | MISO                                 | 126     |
| V <sub>DDINT</sub>     | 19      | GND                    | 55      | GND                | 91      | MOSI                                 | 127     |
| GND                    | 20      | DAI_P2 (SD0B)          | 56      | GND                | 92      | GND                                  | 128     |
| V <sub>DDEXT</sub>     | 21      | DAI_P3 (SCLK0)         | 57      | V <sub>DDEXT</sub> | 93      | V <sub>DDINT</sub>                   | 129     |
| GND                    | 22      | GND                    | 58      | DAI_P20 (SFS5)     | 94      | V <sub>DDEXT</sub>                   | 130     |
| V <sub>DDINT</sub>     | 23      | V <sub>DDEXT</sub>     | 59      | GND                | 95      | A <sub>vdd</sub>                     | 131     |
| AD6                    | 24      | V <sub>DDINT</sub>     | 60      | V <sub>DDINT</sub> | 96      | A <sub>vss</sub>                     | 132     |
| AD5                    | 25      | GND                    | 61      | FLAG2              | 97      | GND                                  | 133     |
| AD4                    | 26      | DAI_P4 (SFS0)          | 62      | FLAG3              | 98      | $\overline{\text{RESETOUT}}$         | 134     |
| V <sub>DDINT</sub>     | 27      | DAI_P5 (SD1A)          | 63      | V <sub>DDINT</sub> | 99      | $\overline{\text{EMU}}$              | 135     |
| GND                    | 28      | DAI_P6 (SD1B)          | 64      | GND                | 100     | TDO                                  | 136     |
| AD3                    | 29      | DAI_P7 (SCLK1)         | 65      | V <sub>DDINT</sub> | 101     | TDI                                  | 137     |
| AD2                    | 30      | V <sub>DDINT</sub>     | 66      | GND                | 102     | $\overline{\text{TRST}}$             | 138     |
| V <sub>DDEXT</sub>     | 31      | GND                    | 67      | V <sub>DDINT</sub> | 103     | TCK                                  | 139     |
| GND                    | 32      | V <sub>DDINT</sub>     | 68      | GND                | 104     | TMS                                  | 140     |
| AD1                    | 33      | GND                    | 69      | V <sub>DDINT</sub> | 105     | GND                                  | 141     |
| AD0                    | 34      | DAI_P8 (SFS1)          | 70      | GND                | 106     | CLKIN                                | 142     |
| $\overline{\text{WR}}$ | 35      | DAI_P9 (SD2A)          | 71      | V <sub>DDINT</sub> | 107     | XTAL                                 | 143     |
| V <sub>DDINT</sub>     | 36      | V <sub>DDINT</sub>     | 72      | V <sub>DDINT</sub> | 108     | V <sub>DDEXT</sub>                   | 144     |
|                        |         |                        |         |                    |         | GND                                  | 145*    |

\*The ePAD is electrically connected to GND inside the chip (see [Figure 43](#) and [Figure 44](#)), therefore connecting the pad to GND is optional. For better thermal performance the ePAD should be soldered to the board and thermally connected to the GND plane with vias.

Figure 43 shows the top view of the 144-lead LQFP\_EP pin configuration. Figure 44 shows the bottom view of the 144-lead LQFP\_EP lead configuration.

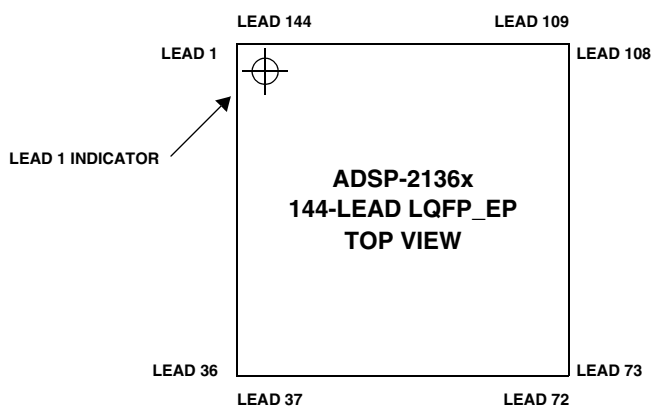


Figure 43. 144-Lead LQFP\_EP Lead Configuration (Top View)

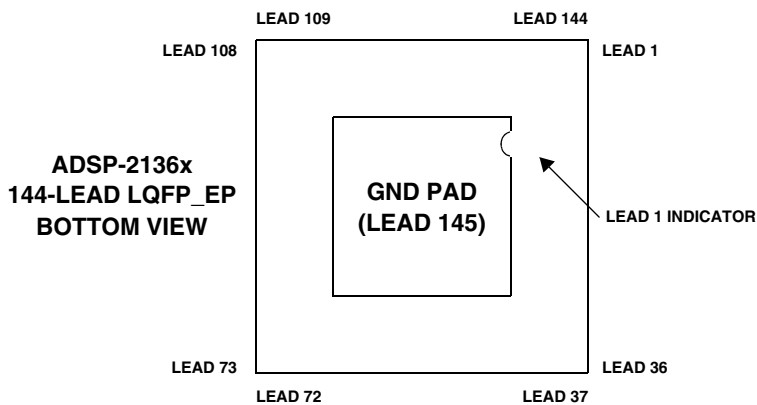


Figure 44. 144-Lead LQFP\_EP Lead Configuration (Bottom View)

## 136-BALL BGA PIN CONFIGURATIONS

The following table shows the processor's ball names and, when applicable, their default function after reset in parentheses.

**Table 46. BGA Pin Assignments**

| Ball Name                    | Ball No. | Ball Name                 | Ball No. | Ball Name          | Ball No. | Ball Name          | Ball No. |
|------------------------------|----------|---------------------------|----------|--------------------|----------|--------------------|----------|
| CLK_CFG0                     | A01      | CLK_CFG1                  | B01      | BOOT_CFG1          | C01      | V <sub>DDINT</sub> | D01      |
| XTAL                         | A02      | GND                       | B02      | BOOT_CFG0          | C02      | GND                | D02      |
| TMS                          | A03      | V <sub>DDEXT</sub>        | B03      | GND                | C03      | GND                | D04      |
| TCK                          | A04      | CLKIN                     | B04      | GND                | C12      | GND                | D05      |
| TDI                          | A05      | $\overline{\text{TRST}}$  | B05      | GND                | C13      | GND                | D06      |
| $\overline{\text{RESETOUT}}$ | A06      | A <sub>VSS</sub>          | B06      | V <sub>DDINT</sub> | C14      | GND                | D09      |
| TDO                          | A07      | A <sub>VDD</sub>          | B07      |                    |          | GND                | D10      |
| $\overline{\text{EMU}}$      | A08      | V <sub>DDEXT</sub>        | B08      |                    |          | GND                | D11      |
| MOSI                         | A09      | SPICLK                    | B09      |                    |          | GND                | D13      |
| MISO                         | A10      | $\overline{\text{RESET}}$ | B10      |                    |          | V <sub>DDINT</sub> | D14      |
| $\overline{\text{SPIDS}}$    | A11      | V <sub>DDINT</sub>        | B11      |                    |          |                    |          |
| V <sub>DDINT</sub>           | A12      | GND                       | B12      |                    |          |                    |          |
| GND                          | A13      | GND                       | B13      |                    |          |                    |          |
| GND                          | A14      | GND                       | B14      |                    |          |                    |          |
| V <sub>DDINT</sub>           | E01      | FLAG1                     | F01      | AD7                | G01      | AD6                | H01      |
| GND                          | E02      | FLAG0                     | F02      | V <sub>DDINT</sub> | G02      | V <sub>DDEXT</sub> | H02      |
| GND                          | E04      | GND                       | F04      | V <sub>DDEXT</sub> | G13      | DAI_P18 (SD5B)     | H13      |
| GND                          | E05      | GND                       | F05      | DAI_P19 (SCLK5)    | G14      | DAI_P17 (SD5A)     | H14      |
| GND                          | E06      | GND                       | F06      |                    |          |                    |          |
| GND                          | E09      | GND                       | F09      |                    |          |                    |          |
| GND                          | E10      | GND                       | F10      |                    |          |                    |          |
| GND                          | E11      | GND                       | F11      |                    |          |                    |          |
| GND                          | E13      | FLAG2                     | F13      |                    |          |                    |          |
| FLAG3                        | E14      | DAI_P20 (SF55)            | F14      |                    |          |                    |          |

**Table 46. BGA Pin Assignments (Continued)**

| Ball Name          | Ball No. | Ball Name          | Ball No. | Ball Name      | Ball No. | Ball Name       | Ball No. |
|--------------------|----------|--------------------|----------|----------------|----------|-----------------|----------|
| AD5                | J01      | AD3                | K01      | AD2            | L01      | AD0             | M01      |
| AD4                | J02      | V <sub>DDINT</sub> | K02      | AD1            | L02      | $\overline{WR}$ | M02      |
| GND                | J04      | GND                | K04      | GND            | L04      | GND             | M03      |
| GND                | J05      | GND                | K05      | GND            | L05      | GND             | M12      |
| GND                | J06      | GND                | K06      | GND            | L06      | DAI_P12 (SD3B)  | M13      |
| GND                | J09      | GND                | K09      | GND            | L09      | DAI_P13 (SCLK3) | M14      |
| GND                | J10      | GND                | K10      | GND            | L10      |                 |          |
| GND                | J11      | GND                | K11      | GND            | L11      |                 |          |
| V <sub>DDINT</sub> | J13      | GND                | K13      | GND            | L13      |                 |          |
| DAI_P16 (SD4B)     | J14      | DAI_P15 (SD4A)     | K14      | DAI_P14 (SFS3) | L14      |                 |          |
| AD15               | N01      | AD14               | P01      |                |          |                 |          |
| ALE                | N02      | AD13               | P02      |                |          |                 |          |
| $\overline{RD}$    | N03      | AD12               | P03      |                |          |                 |          |
| V <sub>DDINT</sub> | N04      | AD11               | P04      |                |          |                 |          |
| V <sub>DDEXT</sub> | N05      | AD10               | P05      |                |          |                 |          |
| AD8                | N06      | AD9                | P06      |                |          |                 |          |
| V <sub>DDINT</sub> | N07      | DAI_P1 (SD0A)      | P07      |                |          |                 |          |
| DAI_P2 (SD0B)      | N08      | DAI_P3 (SCLK0)     | P08      |                |          |                 |          |
| V <sub>DDEXT</sub> | N09      | DAI_P5 (SD1A)      | P09      |                |          |                 |          |
| DAI_P4 (SFS0)      | N10      | DAI_P6 (SD1B)      | P10      |                |          |                 |          |
| V <sub>DDINT</sub> | N11      | DAI_P7 (SCLK1)     | P11      |                |          |                 |          |
| V <sub>DDINT</sub> | N12      | DAI_P8 (SFS1)      | P12      |                |          |                 |          |
| GND                | N13      | DAI_P9 (SD2A)      | P13      |                |          |                 |          |
| DAI_P10 (SD2B)     | N14      | DAI_P11 (SD3A)     | P14      |                |          |                 |          |

Figure 45 and Figure 46 show BGA pin assignments from the bottom and top, respectively.

**Note:** Use the center block of ground pins to provide thermal pathways to your printed circuit board's ground plane.

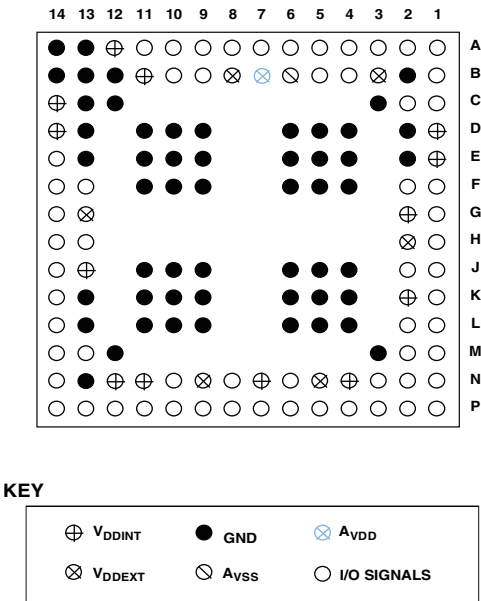


Figure 45. BGA Pin Assignments (Bottom View, Summary)

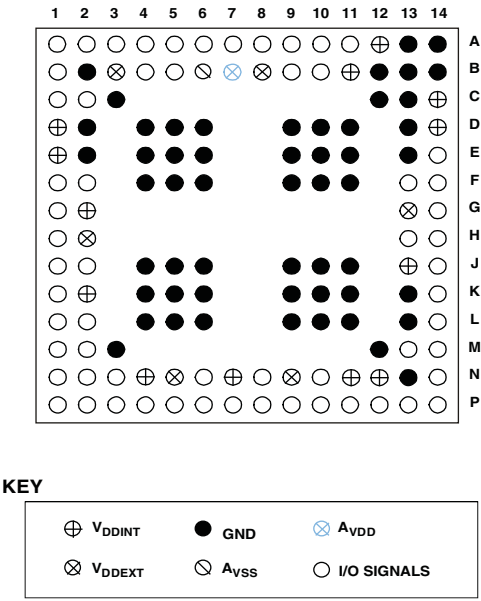
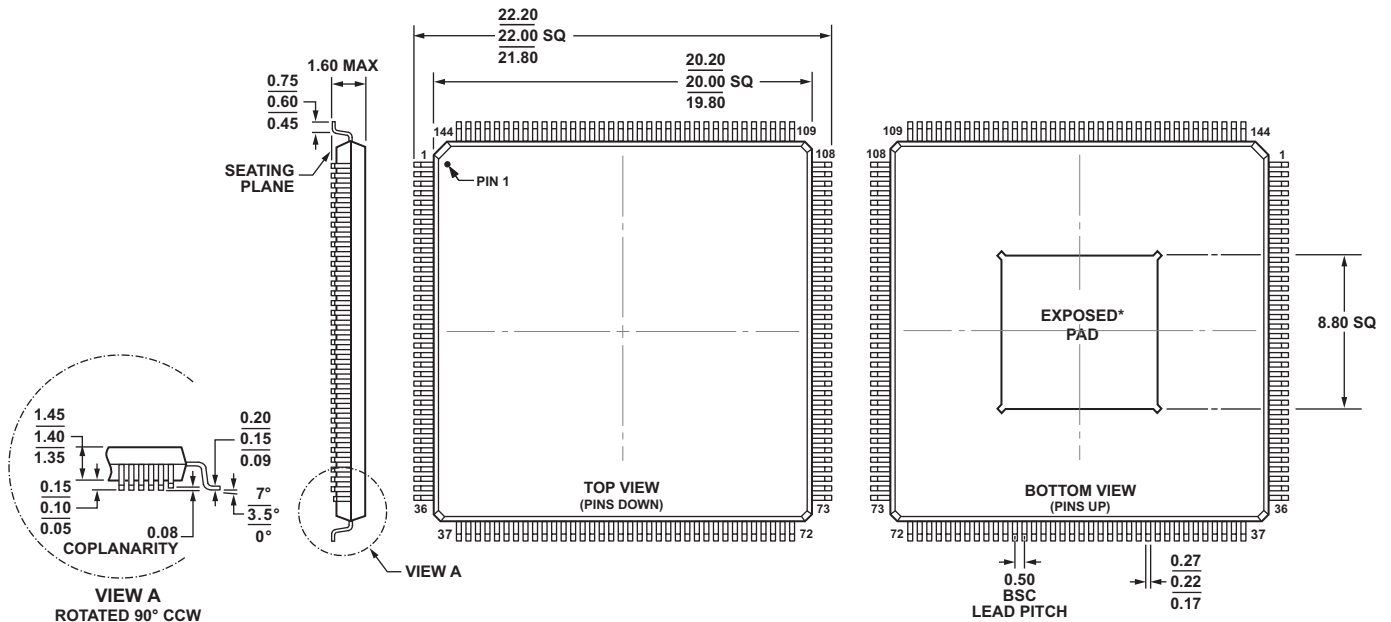


Figure 46. BGA Pin Assignments (Top View, Summary)

## PACKAGE DIMENSIONS

The processor is available in 136-ball BGA and 144-lead exposed pad (LQFP\_EP) packages.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB-HD  
 \*EXPOSED PAD IS COINCIDENT WITH BOTTOM SURFACE AND DOES NOT PROTRUDE BEYOND IT. EXPOSED PAD IS CENTERED.

Figure 47. 144-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP\_EP<sup>1</sup>]  
 (SW-144-1)

Dimensions shown in millimeters

<sup>1</sup> For information relating to the exposed pad on the SW-144-1 package, see the table endnote on Page 48.

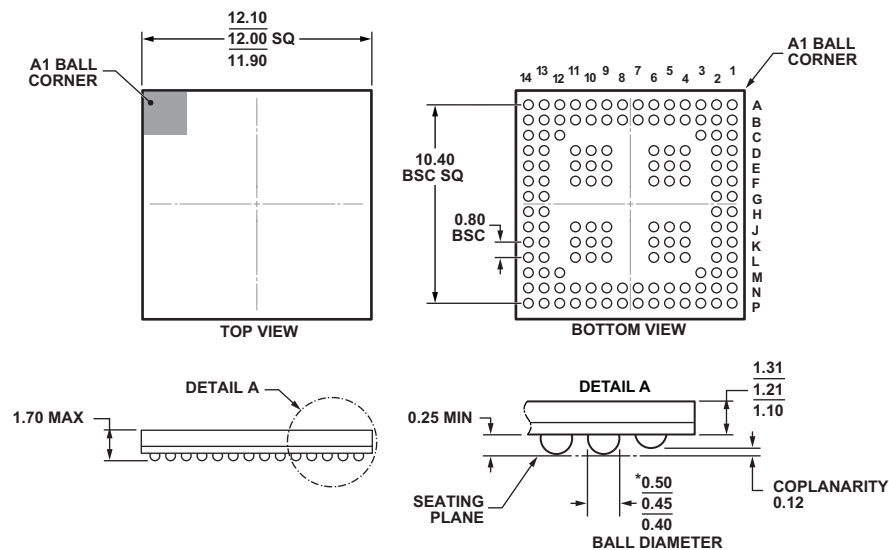


Figure 48. 136-Ball Chip Scale Package Ball Grid Array [CSP\_BGA]  
(BC-136-1)  
Dimensions shown in millimeters

**SURFACE-MOUNT DESIGN**

Table 47 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 47. BGA Data for Use with Surface-Mount Design

| Package                     | Package Ball Attach Type | Package Solder Mask Opening | Package Ball Pad Size |
|-----------------------------|--------------------------|-----------------------------|-----------------------|
| 136-Ball CSP_BGA (BC-136-1) | Solder Mask Defined      | 0.40 mm diameter            | 0.53 mm diameter      |

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## AUTOMOTIVE PRODUCTS

Some ADSP-2136x models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

**Table 48. Automotive Products**

| Model            | Notes        | Temperature Range <sup>1</sup> | Instruction Rate | On-Chip SRAM | ROM    | Package Description | Package Option |
|------------------|--------------|--------------------------------|------------------|--------------|--------|---------------------|----------------|
| AD21362WBBCZ1xx  | <sup>2</sup> | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| AD21362WBSWZ1xx  | <sup>2</sup> | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21362WYSWZ2xx  | <sup>2</sup> | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21363WBBCZ1xx  |              | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| AD21363WBSWZ1xx  |              | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21363WYSWZ2xx  |              | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21364WBBCZ1xx  |              | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| AD21364WBSWZ1xx  |              | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21364WYSWZ2xx  |              | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21365WBSWZ1xxA | 2, 3, 4      | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21365WBSWZ1xxF | 2, 3, 4      | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21365WYSWZ2xxA | 2, 3, 4      | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21366WBBCZ1xxA | 3, 4         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| AD21366WBSWZ1xxA | 3, 4         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| AD21366WYSWZ2xxA | 3, 4         | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |

<sup>1</sup> Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see [Operating Conditions on Page 14](#) for junction temperature (T<sub>J</sub>) specification which is the only temperature specification.

<sup>2</sup> License from DTLA required for these products.

<sup>3</sup> Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at [www.analog.com/sharc](http://www.analog.com/sharc).

<sup>4</sup> License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.

# ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366

## ORDERING GUIDE

| Model <sup>1</sup> | Notes   | Temperature Range <sup>2</sup> | Instruction Rate | On-Chip SRAM | ROM    | Package Description | Package Option |
|--------------------|---------|--------------------------------|------------------|--------------|--------|---------------------|----------------|
| ADSP-21363KBC-1AA  | 3       | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21363KBCZ-1AA |         | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21363KSWZ-1AA |         | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| ADSP-21363BBC-1AA  |         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21363BBCZ-1AA |         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21363BSWZ-1AA |         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| ADSP-21363YSWZ-2AA |         | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| ADSP-21364KBCZ-1AA |         | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21364KSWZ-1AA |         | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| ADSP-21364BBCZ-1AA |         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21364BSWZ-1AA |         | –40°C to +85°C                 | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| ADSP-21364YSWZ-2AA |         | –40°C to +105°C                | 200 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |
| ADSP-21366KBCZ-1AR | 3, 4, 5 | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21366KBCZ-1AA | 3, 4    | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 136-Ball CSP_BGA    | BC-136-1       |
| ADSP-21366KSWZ-1AA | 3, 4    | 0°C to +70°C                   | 333 MHz          | 3M Bit       | 4M Bit | 144-Lead LQFP_EP    | SW-144-1       |

<sup>1</sup>Z = RoHS compliant part.

<sup>2</sup>Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see [Operating Conditions on Page 14](#) for junction temperature (T<sub>j</sub>) specification which is the only temperature specification.

<sup>3</sup>License from Dolby Laboratories, Inc., and Digital Theater Systems (DTS) required for these products.

<sup>4</sup>Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at [www.analog.com/sharc](http://www.analog.com/sharc).

<sup>5</sup>R = Tape and reel.







