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REVISION HISTORY

5/11—Data Sheet Changed from Rev. C to Rev. D

Deleted ADM209	Universal
Changes to Figure 5	5
Updated Outline Dimensions	13
Changes to Ordering Guide	15

1/05—Data Sheet Changed from Rev. B to Rev. C

Changes to Specifications	3
Change to Receivers section	11
Change to Driving Long Cables section	12
Updated Outline Dimensions	13
Changes to Ordering Guide	15

6/02—Data Sheet Changed from Rev. A to Rev. B

Removed all references to ADM205	Universal
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3/02—Data Sheet Changed from Rev. 0 to Rev. A

Changes to numbers in Min/Typ/Max column of Specifications page	2
Updated Figures	8, 9

Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 10\%$ (ADM206, ADM207, ADM208, ADM211, ADM213); $C1-C4 = 0.1\text{ }\mu\text{F}$ ceramic. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Swing	± 5	± 9		V	All transmitter outputs loaded with $3\text{ k}\Omega$ to ground
V_{CC} Power Supply Current		5	13	mA	No load
Shutdown Supply Current		1	10	μA	
Input Logic Threshold Low, V_{INL}			0.8	V	$T_{IN}, \overline{EN}, \overline{SD}, \overline{EN}, \overline{SD}$
Input Logic Threshold High, V_{INH}	2.0			V	$T_{IN}, \overline{EN}, \overline{SD}, \overline{EN}, \overline{SD}$
Logic Pull-Up Current		10	25	μA	$T_{IN} = 0\text{ V}$
RS-232 Input Voltage Range ¹	-30		+30	V	
RS-232 Input Threshold Low	0.8	1.25		V	
RS-232 Input Threshold High		1.9	2.4	V	
RS-232 Input Hysteresis		0.65		V	
RS-232 Input Resistance	3	5	7	$\text{k}\Omega$	$T_A = 0^\circ\text{C}$ to 85°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	$I_{OUT} = 1.6\text{ mA}$
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	$I_{OUT} = -1.0\text{ mA}$
TTL/CMOS Output Leakage Current		0.05	± 10	μA	$\overline{EN} = V_{CC}, \overline{EN} = 0\text{ V}, 0\text{ V} \leq R_{OUT} \leq V_{CC}$
Output Enable Time (T_{EN})		115		ns	ADM206, ADM211 (Figure 22. $C_L = 150\text{ pF}$)
Output Disable Time (T_{DIS})		165		ns	ADM206, ADM211 (Figure 22. $R_L = 1\text{ k}\Omega$)
Propagation Delay		0.5	5	μs	RS-232 to TTL
Transition Region Slew Rate		8		$\text{V}/\mu\text{s}$	$R_L = 3\text{ k}\Omega, C_L = 2500\text{ pF}$; measured from $+3\text{ V}$ to -3 V or -3 V to $+3\text{ V}$
Output Resistance	300			Ω	$V_{CC} = V_+ = V_- = 0\text{ V}, V_{OUT} = \pm 2\text{ V}$
RS-232 Output Short Circuit Current		± 12	± 60	mA	

¹ Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Min
V _{CC}	–0.3 V to +6 V
V ₊	(V _{CC} – 0.3 V) to +14 V
V _–	+0.3 V to –14 V
Input Voltages	
T _{IN}	–0.3 V to (V _{CC} + 0.3 V)
R _{IN}	±30 V
Output Voltages	
T _{OUT}	(V ₊ , +0.3 V) to (V _– , –0.3 V)
R _{OUT}	–0.3 V to (V _{CC} + 0.3 V)
Short-Circuit Duration	
T _{OUT}	Continuous
Power Dissipation	
N-24 PDIP (Derate 13.5 mW/°C above 70°C)	1000 mW
R-24 SOIC (Derate 12 mW/°C above 70°C)	850 mW
R-28 SOIC (Derate 12.5 mW/°C above 70°C)	900 mW
RS-24 SSOP (Derate 12 mW/°C above 70°C)	850 mW
RS-28 SSOP (Derate 10 mW/°C above 70°C)	900 mW
Thermal Impedance, θ _{JA}	
N-24 PDIP	120°C/W
R-24 SOIC	85°C/W
R-28 SOIC	80°C/W
RS-24 SSOP	115°C/W
RS-28 SSOP	100°C/W
Operating Temperature Range	
Industrial (A Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature, Soldering	300°C
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

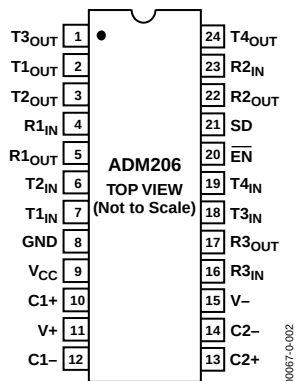


Figure 2. ADM206 PDIP/SSOP Pin Configuration

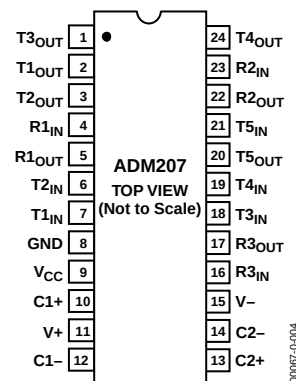
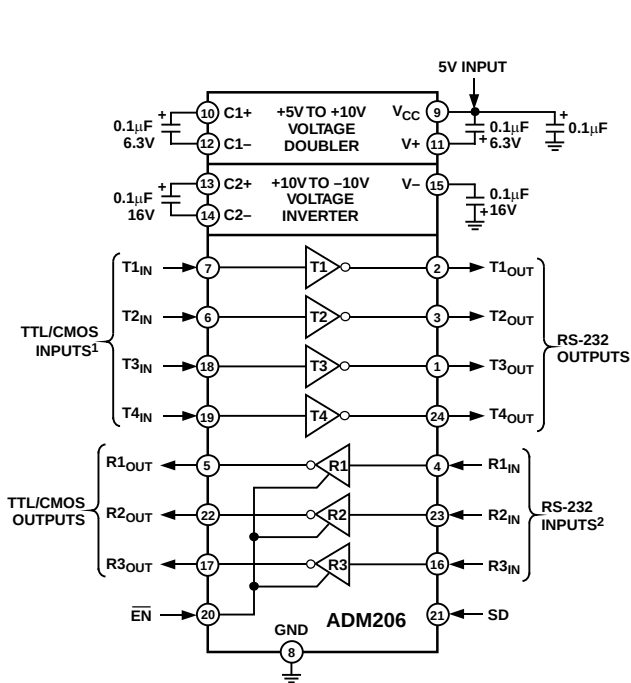
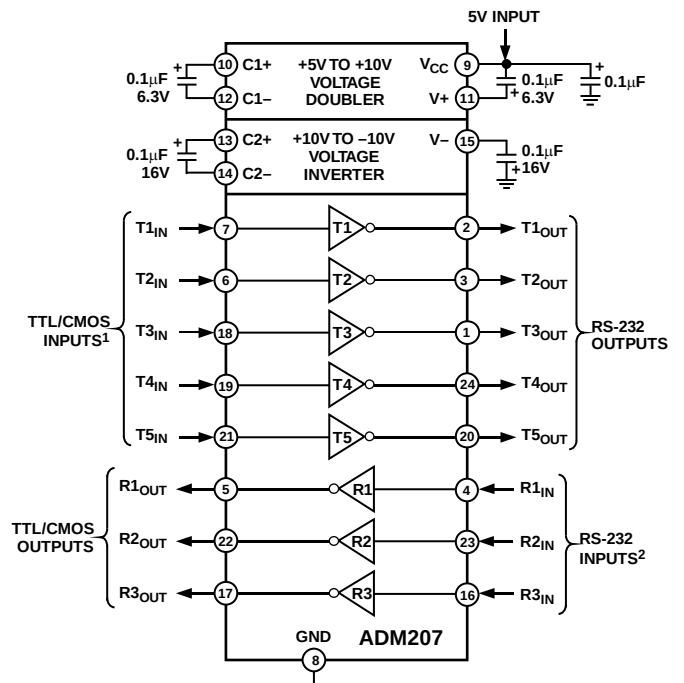


Figure 4. ADM207 PDIP/SSOP Pin Configuration



NOTES
¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

Figure 3. ADM206 Typical Operating Circuit



NOTES
¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

Figure 5. ADM207 Typical Operating Circuit

ADM206/ADM207/ADM208/ADM211/ADM213

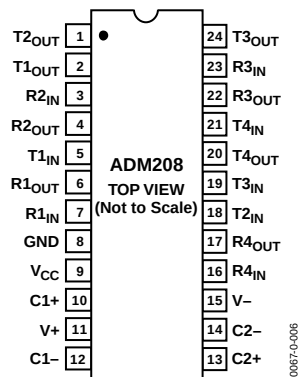


Figure 6. ADM208 PDIP/SSOP Pin Configuration

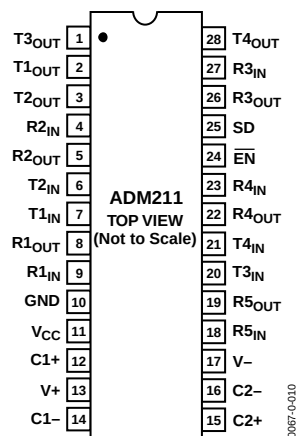
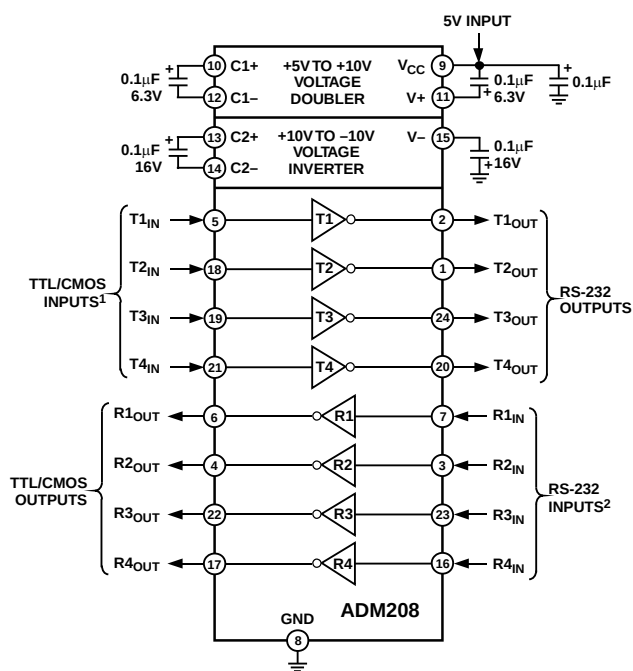


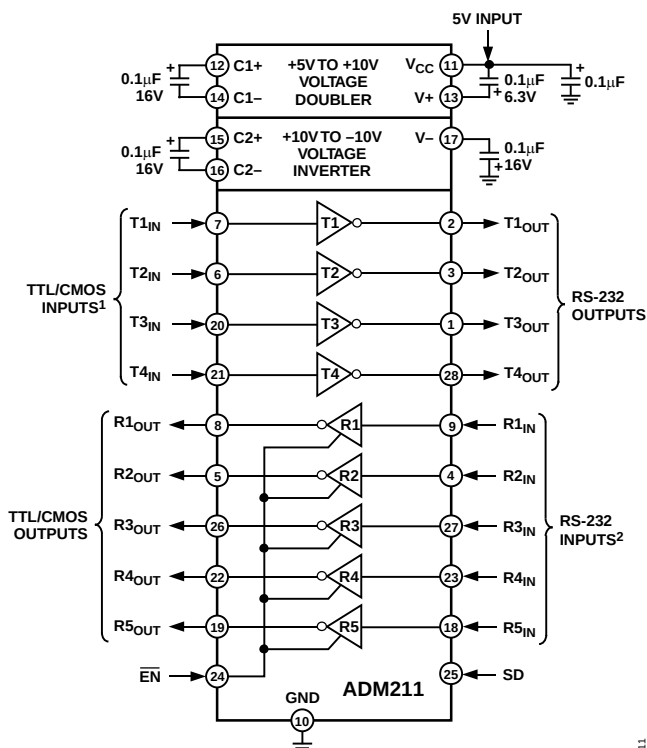
Figure 8. ADM211 SOIC/SSOP Pin Configuration



NOTES

- ¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
- ²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

Figure 7. ADM208 Typical Operating Circuit



NOTES

- ¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
- ²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

Figure 9. ADM211 Typical Operating Circuit

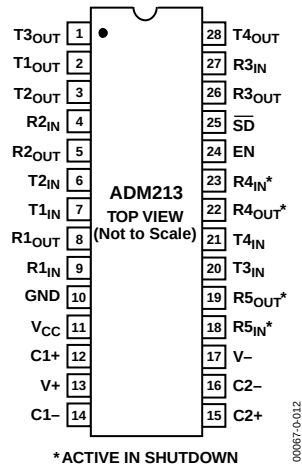


Figure 10. ADM213 SOIC/SSOP Pin Configuration

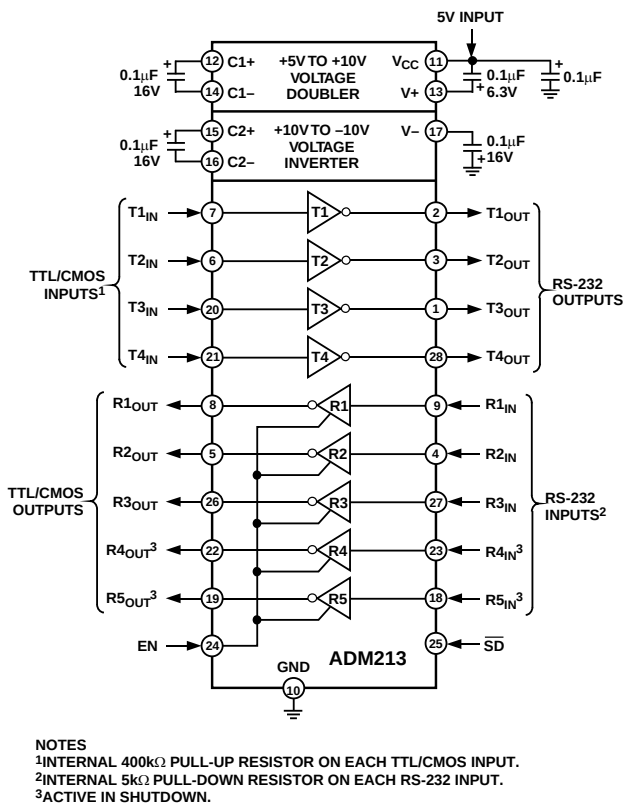


Figure 11. ADM213 Typical Operating Circuit

ADM206/ADM207/ADM208/ADM211/ADM213

Table 4. Pin Function Descriptions

Mnemonic	Function
V _{CC}	Power Supply Input. 5 V ± 10%.
V+	Internally Generated Positive Supply (10 V nominal).
V-	Internally Generated Negative Supply (-10 V Nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+	External Capacitor (+ terminal) is connected to this pin.
C1-	External Capacitor (- terminal) is connected to this pin.
C2+	External Capacitor (+ terminal) is connected to this pin.
C2-	External Capacitor (- terminal) is connected to this pin.
T _{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V _{CC} is connected to each input.
T _{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ± 10 V).
R _{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected to each input.
R _{OUT}	Receiver Outputs. These are TTL/CMOS levels.
EN/ $\overline{\text{EN}}$	Enable Input. Active low on ADM206 and ADM211. Active high on ADM213. This input is used to enable/disable the receiver outputs. With $\overline{\text{EN}}$ = low (EN = high ADM213), the receiver outputs are enabled. With $\overline{\text{EN}}$ = high (EN = low ADM213), the outputs are placed in a high impedance state. This is useful for connecting to microprocessor systems.
SD/ $\overline{\text{SD}}$	Shutdown Input. Active high on ADM206 and ADM211. Active low on ADM213. With SD = high on the ADM206 and ADM211, the charge pump is disabled, the receiver outputs are placed in a high impedance state, and the driver outputs are turned off. With SD = low on the ADM213, the charge pump is disabled, the driver outputs are turned off, and all receivers, except R4 and R5, are placed in a high impedance state. In shutdown, the power consumption reduces to 5 μW.
NC	No Connect. No connections are required to this pin.

Table 5. ADM206 and ADM211 Truth Table

SD	EN	Status	Transmitters T1-T5	Receivers R1-R5
0	0	Normal Operation	Enabled	Enabled
0	1	Normal Operation	Enabled	Disabled
1	0	Shutdown	Disabled	Disabled

Table 6. ADM213 Truth Table

SD	EN	Status	Transmitters T1-T4	Receivers R1-R3	Receivers R4, R5
0	0	Shutdown	Disabled	Disabled	Disabled
0	1	Shutdown	Disabled	Disabled	Enabled
1	0	Normal Operation	Enabled	Disabled	Disabled
1	1	Normal Operation	Enabled	Enabled	Enabled

TYPICAL PERFORMANCE CHARACTERISTICS

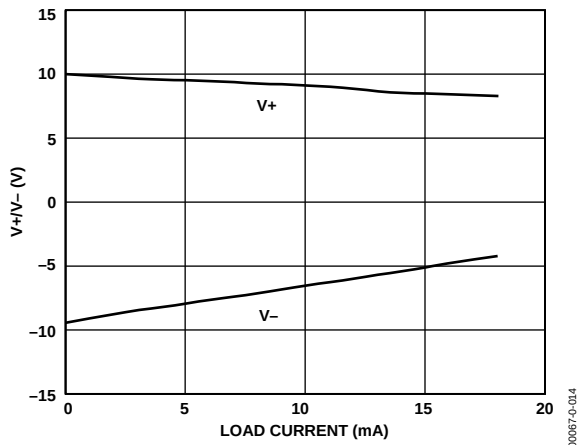


Figure 12. Charge Pump V+, V- vs. Load Current

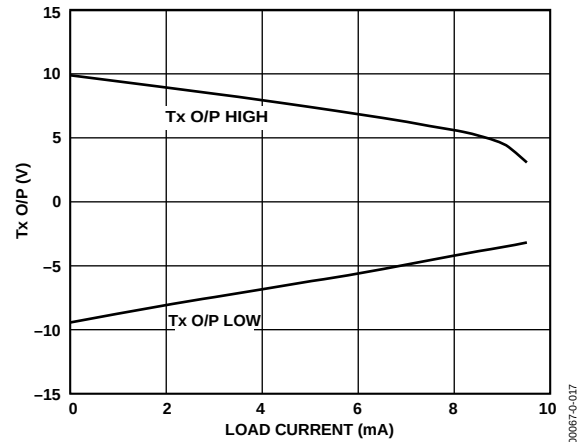


Figure 15. Transmitter Output Voltage vs. Load Current

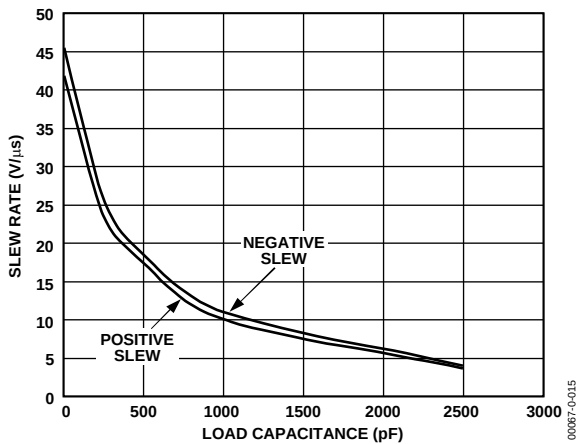


Figure 13. Transmitter Slew Rate vs. Load Capacitance

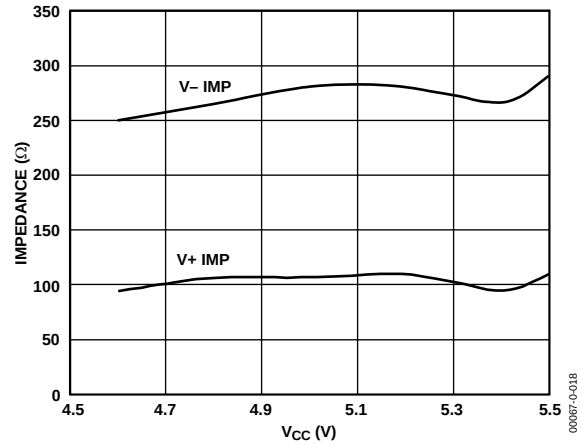


Figure 16. Charge Pump Impedance vs. V_{CC}

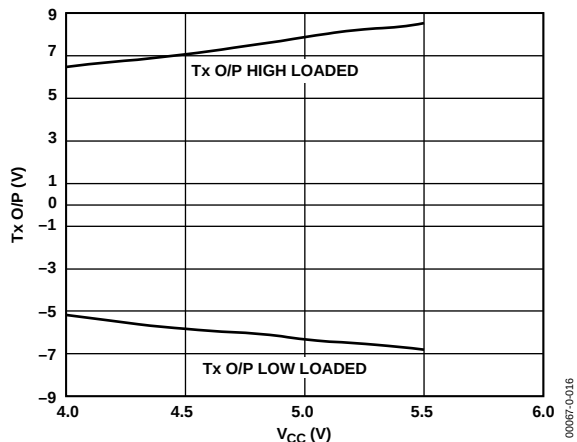


Figure 14. Transmitter Output Voltage vs. V_{CC}

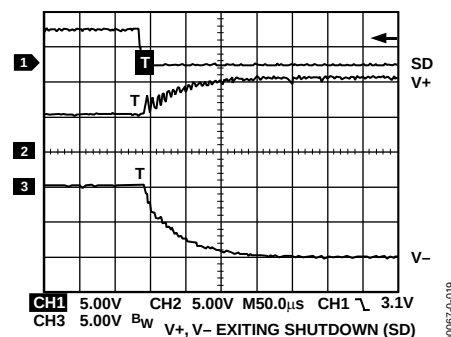


Figure 17. Charge Pump, V+, V- Exiting Shutdown (SD)

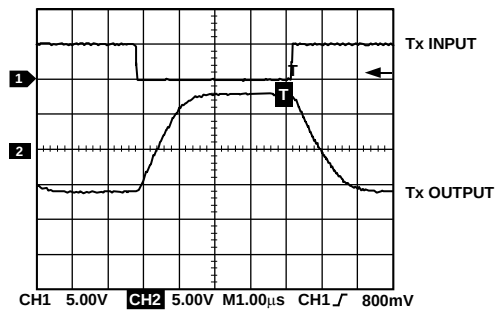


Figure 18. Transmitter Output Loaded Slew Rate

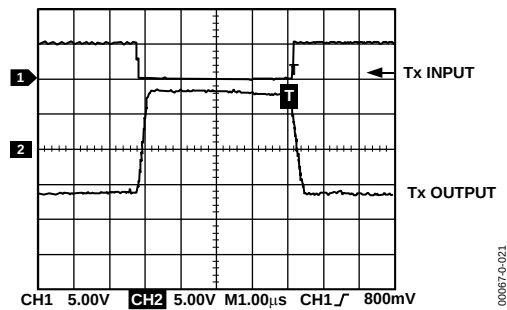


Figure 19. Transmitter Output Unloaded Slew Rate

GENERAL INFORMATION

The ADM2xx family of RS-232 drivers/ receivers is designed to solve interface problems by meeting the EIA-232-E specifications while using a single digital 5 V supply. The EIA-232-E standard requires transmitters that will deliver ± 5 V minimum on the transmission channel and receivers that can accept signal levels down to ± 3 V. The ADM2xx meet these requirements by integrating step-up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/ receiver combinations is available to cover most communication needs. The ADM2xx are modifications, enhancements, and improvements to the AD2xx family and derivatives thereof. They are essentially plug-in compatible and do not have materially different applications.

The ADM206, ADM211, and ADM213 are particularly useful in battery-powered systems because they feature a low power shut-down mode that reduces power dissipation to less than 5 μ W.

To facilitate sharing a common line or for connection to a microprocessor data bus, the ADM206, the ADM211, and the ADM213 feature an enable (EN) function. When the receivers are disabled, their outputs are placed in a high impedance state.

CIRCUIT DESCRIPTION

The internal circuitry in the ADM2xx consists of three main sections: (a) a charge pump voltage converter; (b) RS-232-to-TTL/CMOS receivers; and (c) TTL/CMOS-to-RS-232 transmitters.

Charge Pump DC-to-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ± 10 V supply from the 5 V input. This is done in two stages using a switched capacitor technique, as illustrated in Figure 20 and Figure 21. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate -10 V using C2 as the storage element.

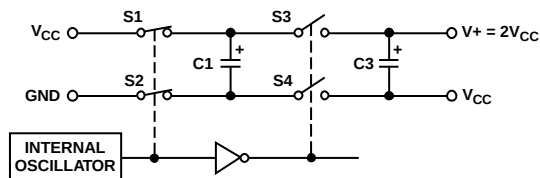


Figure 20. Charge Pump Voltage Doubler

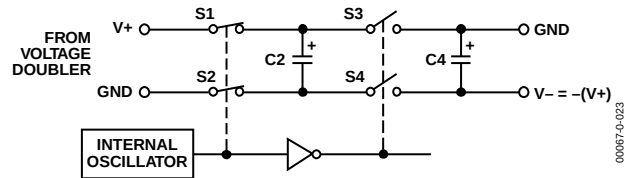


Figure 21. Charge Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V- supplies.

The V+ and V- supplies may also be used to power external circuitry if the current requirements are small.

Transmitters (Drivers)

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With $V_{CC} = +5$ V and driving a typical EIA-232-E load, the output voltage swing is ± 9 V. Even under worst-case conditions, the drivers are guaranteed to meet the ± 5 V EIA-232-E minimum requirement.

The input threshold levels are both TTL- and CMOS-compatible with the switching threshold set at $V_{CC}/4$. With a nominal $V_{CC} = 5$ V, the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, because an internal 400 k Ω pull-up resistor pulls them high, forcing the outputs into a low state.

As required by the EIA-232-E standard, the slew rate is limited to less than 30 V/ μ s, without the need for an external slew limiting capacitor, and the output impedance in the power-off state is greater than 300 Ω .

Receivers

The receivers are inverting level shifters that accept EIA-232-E input levels (± 5 V to ± 15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 k Ω pull-down resistors to ground and are also protected against overvoltages of up to ± 30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum, well within the ± 3 V EIA-232-E requirement. The low level threshold is deliberately positive, since it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt-trigger inputs with a hysteresis level of 0.65 V. This ensures error-free reception for both noisy inputs and inputs with slow transition times.

Shutdown (SD)

The ADM2xx feature a control input that may be used to disable the part and reduce the power consumption to less than 5 Ω W. This is very useful in battery-operated systems. During shutdown, the charge pump is turned off, the transmitters are disabled, and all receivers except R4 and R5 on the ADM213 are put into a high impedance disabled state. Receivers R4 and R5 on the ADM213 remain enabled during shutdown. This feature allows monitoring external activity while the device is in a low power shutdown mode. The shutdown control input is active high on all parts except the ADM213, where it is active low. See Table 5 and Table 6.

Enable Input

The ADM211 and ADM213 feature an enable input used to enable or disable the receiver outputs. The enable input is active low on the ADM211 and active high on the ADM213. See Table 5 and Table 6. When the receivers are disabled, their outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 22.

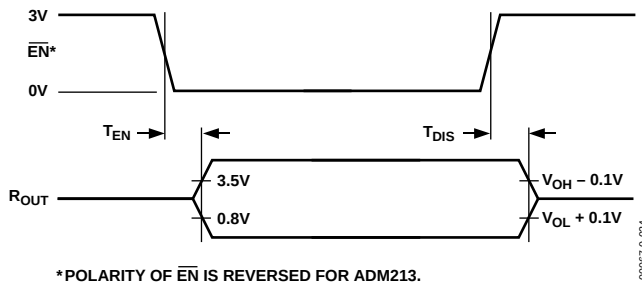


Figure 22. Enable Timing

APPLICATION HINTS

Driving Long Cables

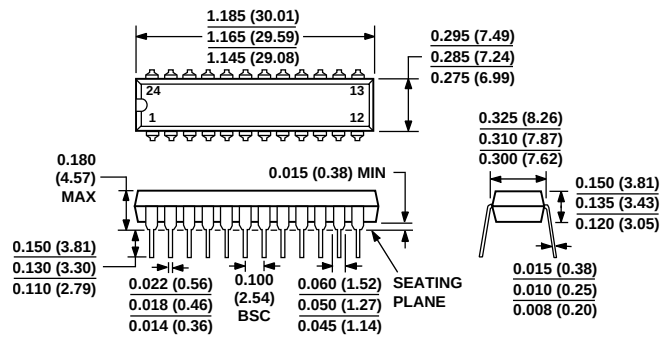
In accordance with the EIA-232-E standard, long cables are permissible provided the total load capacitance does not exceed 2500 pF. For longer cables that do exceed this, it is possible to trade off baud rate for cable length. Large load capacitances cause a reduction in slew rate, and therefore the maximum transmission baud rate is decreased. The ADM2xx are designed to minimize the slew rate reduction that occurs as load capacitance increases.

For the receivers, it is important that a high level of noise immunity be inbuilt so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The ADM2xx have 0.65 V of hysteresis to guard against this. This ensures that even in noisy environments error-free reception can be achieved.

High Baud Rate Operation

The ADM2xx feature high slew rates, permitting data transmission at rates well in excess of the EIA-232-E specification. The drivers maintain ± 5 V signal levels at data rates up to 120 kB/s under worst-case loading conditions.

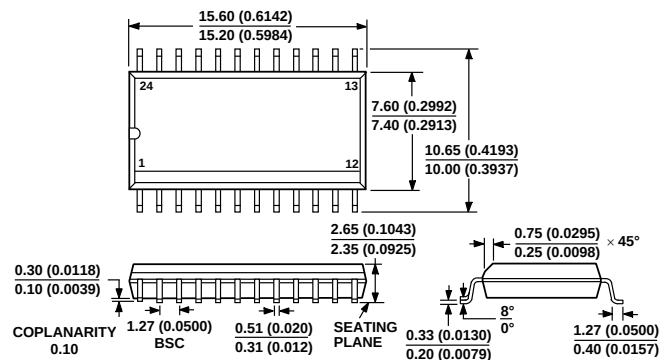
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-095AG
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 23. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 24. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)

Dimensions shown in millimeters and (inches)

ADM206/ADM207/ADM208/ADM211/ADM213

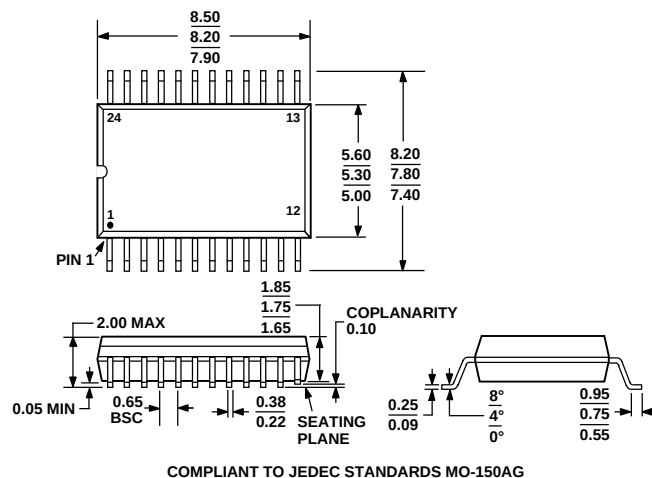


Figure 25. 24-Lead Shrink Small Outline Package [SSOP]
(RS-24)
Dimensions shown in millimeters

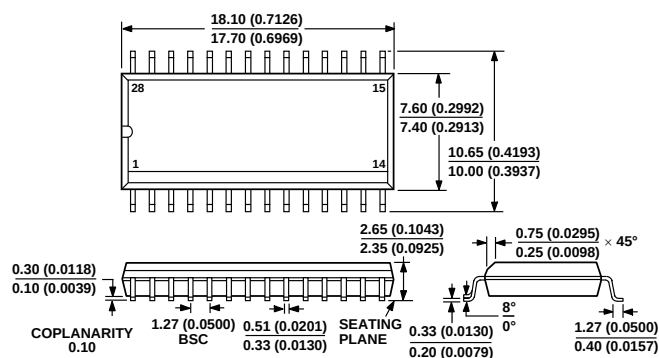
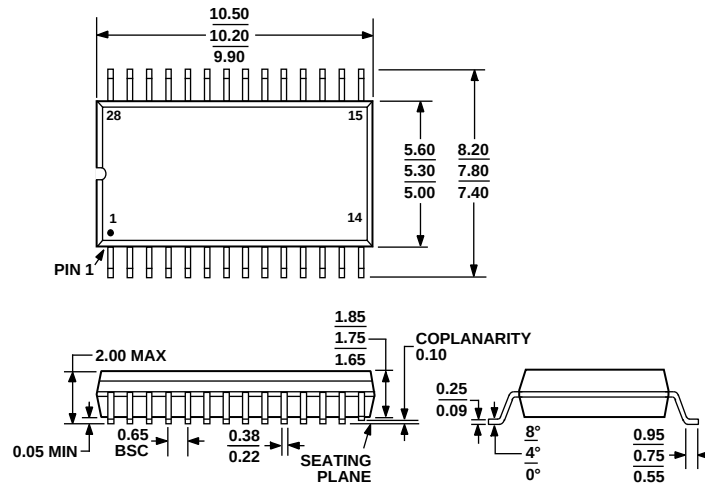


Figure 26. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-150AH

Figure 27. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)

Dimensions shown in millimeters

ADM206/ADM207/ADM208/ADM211/ADM213

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADM206AN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM206ANZ	–40°C to +85°C	24-lead PDIP	N-24-1
ADM206AR	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM206AR-REEL	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM206ARZ	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM206ARZ-REEL	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM206ARS	–40°C to +85°C	24-lead SSOP	RS-24
ADM206ARSZ	–40°C to +85°C	24-lead SSOP	RS-24
ADM206ARSZ-REEL	–40°C to +85°C	24-lead SSOP	RS-24
ADM207AN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM207ANZ	–40°C to +85°C	24-lead PDIP	N-24-1
ADM207AR	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM207ARZ	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM207ARZ-REEL	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM207ARS	–40°C to +85°C	24-lead SSOP	RS-24
ADM207ARSZ	–40°C to +85°C	24-lead SSOP	RS-24
ADM207ARSZ-REEL	–40°C to +85°C	24-lead SSOP	RS-24
ADM208AN	–40°C to +85°C	24-lead PDIP	N-24-1
ADM208ANZ	–40°C to +85°C	24-lead PDIP	N-24-1
ADM208AR	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM208AR-REEL	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM208ARZ	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM208ARZ-REEL	–40°C to +85°C	24-lead SOIC_W	RW-24
ADM208ARSZ	–40°C to +85°C	24-lead SSOP	RS-24
ADM208ARSZ-REEL	–40°C to +85°C	24-lead SSOP	RS-24
ADM211AR	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM211AR-REEL	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM211ARZ	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM211ARZ-REEL	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM211ARS	–40°C to +85°C	28-lead SSOP	RS-28
ADM211ARS-REEL	–40°C to +85°C	28-lead SSOP	RS-28
ADM211ARSZ	–40°C to +85°C	28-lead SSOP	RS-28
ADM211ARSZ-REEL	–40°C to +85°C	28-lead SSOP	RS-28
ADM213AR	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM213ARZ	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM213ARZ-REEL	–40°C to +85°C	28-lead SOIC_W	RW-28
ADM213ARS	–40°C to +85°C	28-lead SSOP	RS-28
ADM213ARS-REEL	–40°C to +85°C	28-lead SSOP	RS-28
ADM213ARSZ	–40°C to +85°C	28-lead SSOP	RS-28
ADM213ARSZ-REEL	–40°C to +85°C	28-lead SSOP	RS-28

¹ Z = RoHS Compliant Part.