

ADG604—SPECIFICATIONS

DUAL SUPPLY¹

($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+125^\circ\text{C}$ unless otherwise noted.)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{SS} to V _{DD}	V	
On Resistance (R_{ON})	85 115	140	160	Ω Typ Ω Max	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})	2 4	5.5	6.5	Ω Typ Ω Max	$V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	25 40	55	60	Ω Typ Ω Max	$V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.1	± 0.25	± 4	nA Typ nA Max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$, Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.01 ± 0.1	± 0.5	± 8	nA Typ nA Max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$, Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.1	± 0.5	± 10	nA Typ nA Max	$V_S = V_D = \pm 4.5\text{ V}$, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V Min	
Input Low Voltage, V_{INL}			0.8	V Max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA Typ μA Max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	2			pF Typ	
DYNAMIC CHARACTERISTICS					
Transition Time	70 100	120	150	ns Typ ns Max	$V_{S1} = +3\text{ V}$, $V_{S4} = -3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4
t_{ON} Enable	80 105	130	150	ns Typ ns Max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
t_{OFF} Enable	30 45	55	65	ns Typ ns Max	$V_S = 3\text{ V}$, Test Circuit 6
Break-Before-Make Time Delay, t_{BBM}	20		10	ns Typ ns Min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$, Test Circuit 5
Charge Injection Off Isolation	-1 -75			pC Typ dB Typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{nF}$, Test Circuit 7
Channel-to-Channel Crosstalk	-70			dB Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 8
Bandwidth -3 dB	280			MHz Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	5			pF Typ	$f = 1\text{ MHz}$
C_D (OFF)	17			pF Typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	18			pF Typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA Typ μA Max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
I_{SS}	0.001		1.0	μA Typ μA Max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Y Version Temperature Range: -40°C to $+125^\circ\text{C}$.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$. All specifications -40°C to $+125^\circ\text{C}$ unless otherwise noted.)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				V	$V_{DD} = 4.5 \text{ V}$, $V_{SS} = 0 \text{ V}$ $V_S = 3.5 \text{ V}$, $I_S = -1 \text{ mA}$, Test Circuit 1
Analog Signal Range			0 V to V_{DD}		
On Resistance (R_{ON})	210 290	350	380	Ω Typ Ω Max	
On Resistance Match Between Channels (ΔR_{ON})	3	12	13	Ω Typ Ω Max	$V_S = 3.5 \text{ V}$, $I_S = -1 \text{ mA}$
LEAKAGE CURRENTS				nA Typ nA Max nA Typ nA Max	$V_{DD} = 5.5 \text{ V}$ $V_S = 1 \text{ V}/4.5 \text{ V}$, $V_D = 4.5 \text{ V}/1 \text{ V}$, Test Circuit 2 $V_S = 1 \text{ V}/4.5 \text{ V}$, $V_D = 4.5 \text{ V}/1 \text{ V}$, Test Circuit 2 $V_S = V_D = 4.5 \text{ V}/1 \text{ V}$, Test Circuit 3
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.1	± 0.25	± 4		
Drain OFF Leakage I_D (OFF)	± 0.01 ± 0.1	± 0.5	± 8		
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.1	± 0.5	10		
DIGITAL INPUTS				V Min V Max μA Typ μA Max pF Typ	$V_{IN} = V_{INL}$ or V_{INH}
Input High Voltage, V_{INH}					
Input Low Voltage, V_{INL}					
Input Current I_{INL} or I_{INH}	0.005		± 0.1		
C_{IN} , Digital Input Capacitance	2				
DYNAMIC CHARACTERISTICS				ns Typ ns Max ns Typ ns Max ns Typ ns Max ns Typ ns Min pC Typ dB Typ dB Typ MHz Typ pF Typ pF Typ pF Typ	$V_{S1} = 3 \text{ V}$, $V_{S4} = 0 \text{ V}$, $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, Test Circuit 4 $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 3 \text{ V}$, Test Circuit 6 $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 3 \text{ V}$, Test Circuit 6 $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_{S1} = V_{S2} = 3 \text{ V}$, Test Circuit 5 $V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$, Test Circuit 7 $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 10 \text{ MHz}$, Test Circuit 8 $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 10 \text{ MHz}$, Test Circuit 10 $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, Test Circuit 9 $f = 1 \text{ MHz}$ $f = 1 \text{ MHz}$ $f = 1 \text{ MHz}$
Transition Time	90				
t_{ON} Enable	150	185	210		
t_{OFF} Enable	105 150	190	220		
Break-Before-Make Time Delay, t_{BBM}	45 70 30	80	90 10		
Charge Injection	0.3				
Off Isolation	-65				
Channel-to-Channel Crosstalk	-70				
Bandwidth -3 dB	250				
C_S (OFF)	5				
C_D (OFF)	17				
C_D , C_S (ON)	18				
POWER REQUIREMENTS	0.001		1.0	μA Typ μA Max	$V_{DD} = 5.5 \text{ V}$ Digital Inputs = 0 V or 5.5 V
I_{DD}					

NOTES

¹Y Version Temperature Range: -40°C to $+125^\circ\text{C}$.

Specifications subject to change without notice.

ADG604—SPECIFICATIONS

SINGLE SUPPLY¹

($V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+125^\circ\text{C}$ unless otherwise noted.)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	380	420	460	Ω Typ	$V_{DD} = 2.7\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$, Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})			5	Ω Typ	$V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01			nA Typ	$V_{DD} = 3.3\text{ V}$
Drain OFF Leakage I_D (OFF)	± 0.1	± 0.25	± 4	nA Max	$V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01	± 0.5	± 8	nA Typ	$V_S = 1\text{ V}/3\text{ V}$, Test Circuit 2
	± 0.1	± 0.5	± 10	nA Max	$V_S = V_D = 1\text{ V}/3\text{ V}$, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V Min	
Input Low Voltage, V_{INL}			0.8	V Max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA Typ	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	2			μA Max	
				pF Typ	
DYNAMIC CHARACTERISTICS					
Transition Time	170			ns Typ	
t_{ON} Enable	320	390	450	ns Max	$V_{S1} = 2\text{ V}$, $V_{S4} = 0\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 4
t_{OFF} Enable	180			ns Typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Break-Before-Make Time Delay, t_{BBM}	250	265	390	ns Max	$V_S = 2\text{ V}$, Test Circuit 6
Charge Injection	100			ns Typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
Off Isolation	160	205	225	ns Max	$V_S = 2\text{ V}$, Test Circuit 6
Channel-to-Channel Crosstalk	100		10	ns Min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 2\text{ V}$, Test Circuit 5
Bandwidth -3 dB	0.3			pC Typ	$V_S = 0\text{ V}$ to 3.3 V , $R_S = 0\ \Omega$, $C_L = 1\ \mu\text{F}$, Test Circuit 7
C_S (OFF)	250			dB Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 8
C_D (OFF)	5			dB Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$, Test Circuit 10
C_D , C_S (ON)	17			MHz Typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
	18			pF Typ	$f = 1\text{ MHz}$
				pF Typ	$f = 1\text{ MHz}$
				pF Typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA Typ	$V_{DD} = 3.3\text{ V}$
				μA Max	Digital Inputs = 0 V or 3.3 V

NOTES

¹Y Version Temperature Range: -40°C to $+125^\circ\text{C}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹(T_A = 25°C unless otherwise noted)

V _{DD} to V _{SS}	13 V
V _{DD} to GND	-0.3 V to +6.5 V
V _{SS} to GND	+0.3 V to -6.5 V
Analog Inputs ²	V _{SS} -0.3 V to V _{DD} + 0.3 V
Digital Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	20 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D	10 mA
Operating Temperature Range (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

Junction Temperature 150°C

TSSOP Package

θ_{JA} Thermal Impedance 150°C/Wθ_{JC} Thermal Impedance 27°C/W

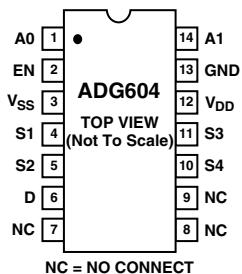
Lead Temperature, Soldering (10 seconds) 300°C

IR Reflow, Peak Temperature 220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overtvoltages at EN, A0, A1, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATION**Table I. Truth Table**

A1	A0	EN	ON Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

CAUTION

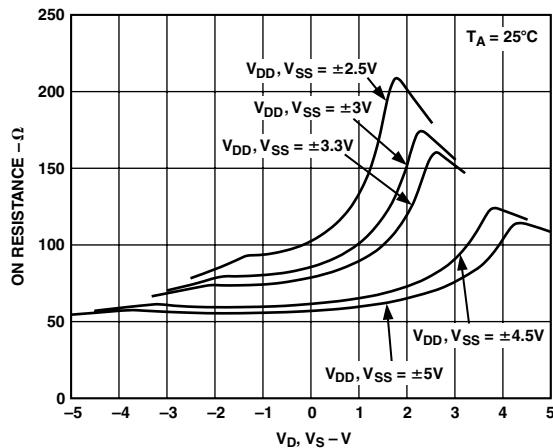
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG604 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



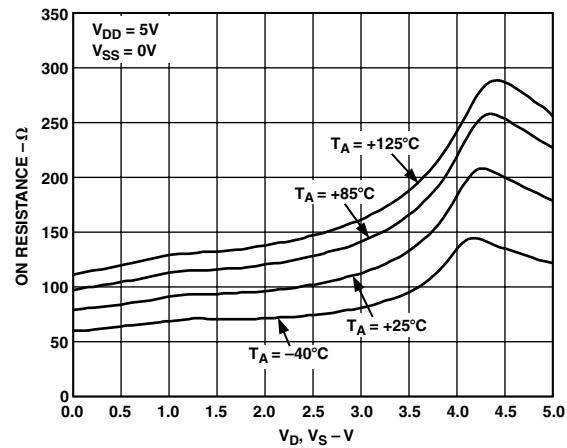
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance Match between any two channels, i.e., $R_{ON\ Max} - R_{ON\ Min}$
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of On resistance as measured over the specified analog signal range.
$I_S\ (OFF)$	Source Leakage Current with the Switch "OFF"
$I_D\ (OFF)$	Drain Leakage Current with the Switch "OFF"
$I_D, I_S\ (ON)$	Channel Leakage Current with the Switch "ON"
V_D, V_S	Analog Voltage on Terminals D, S
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
$I_{INL}\ (I_{INH})$	Input Current of the Digital Input
$C_s\ (OFF)$	Channel Input Capacitance for "OFF" Condition
$C_d\ (OFF)$	Channel Output Capacitance for "OFF" Condition
$C_d, C_s\ (ON)$	"On" Switch Capacitance
C_{IN}	Digital Input Capacitance
$t_{ON}\ (EN)$	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
$t_{OFF}\ (EN)$	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital input and switch "ON" condition when switching from one address state to another.
t_{BBM}	"OFF" time or "ON" time measured between the 80% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "On" switch.
Bandwidth	Frequency Response of the "On" Switch
Insertion Loss	Loss Due to the On Resistance of the Switch

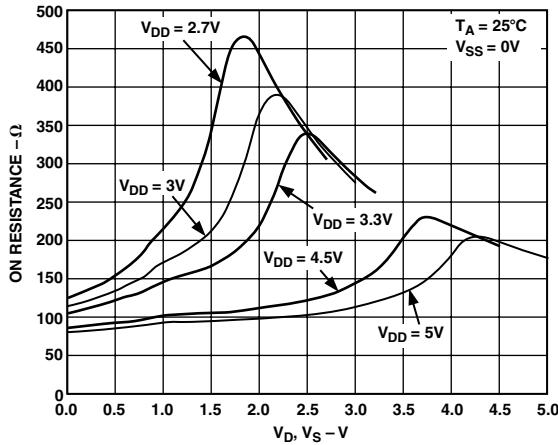
Typical Performance Characteristics—ADG604



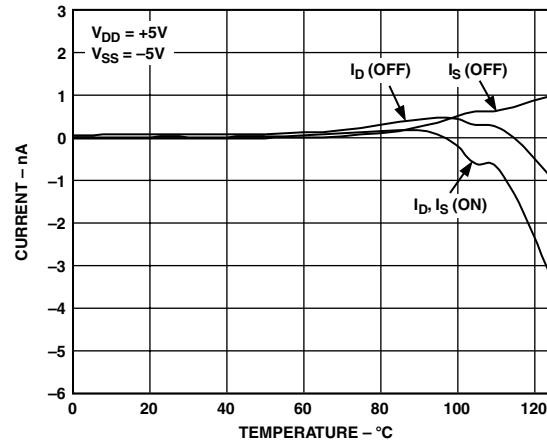
TPC 1. On Resistance vs. V_D (V_S), Dual Supply



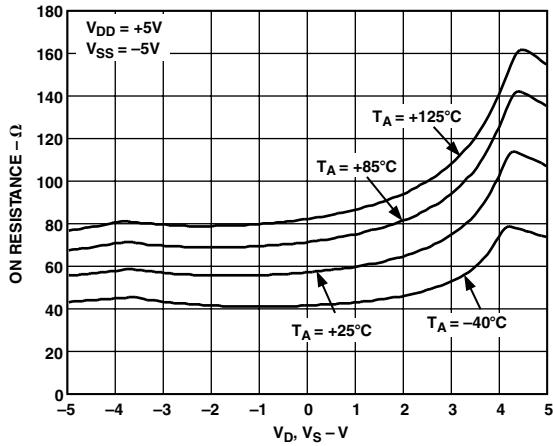
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply



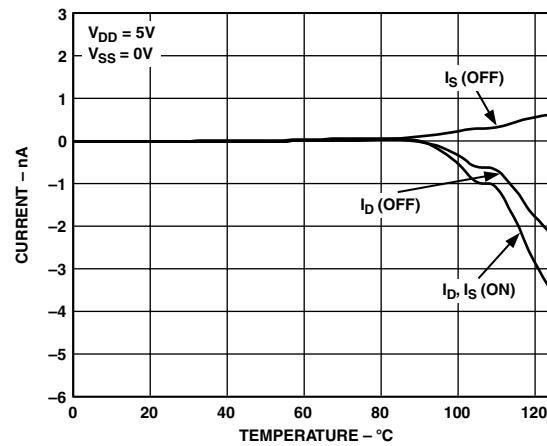
TPC 2. On Resistance vs. V_D (V_S), Single Supply



TPC 5. Leakage Currents vs. Temperature, Dual Supply

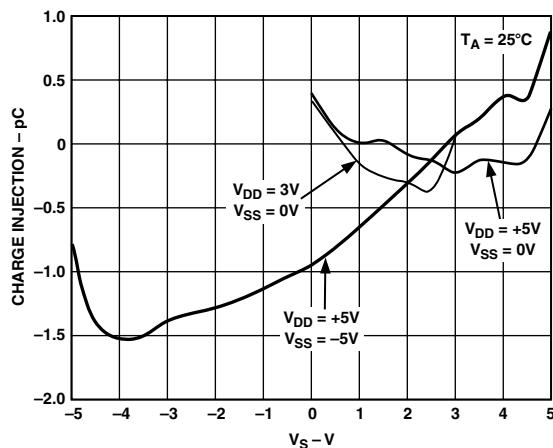


TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures, Dual Supply

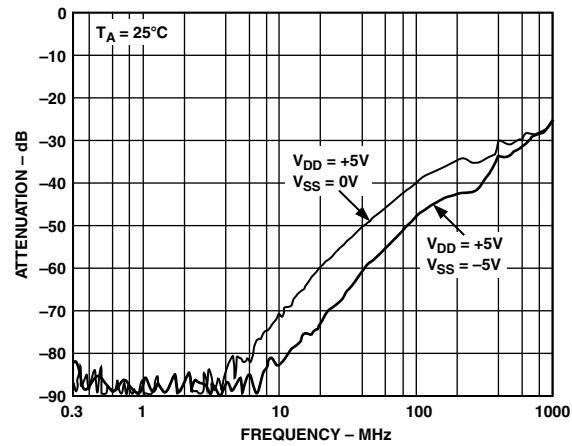


TPC 6. Leakage Currents vs. Temperature, Single Supply

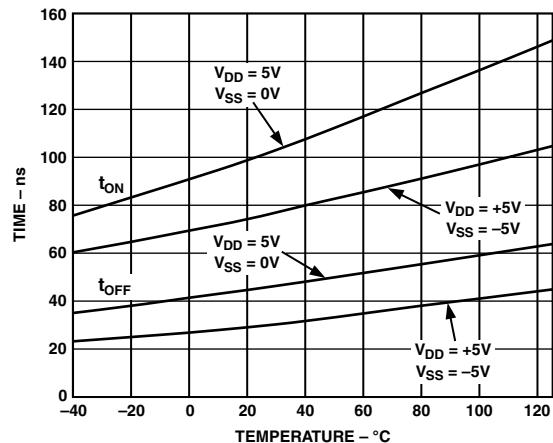
ADG604



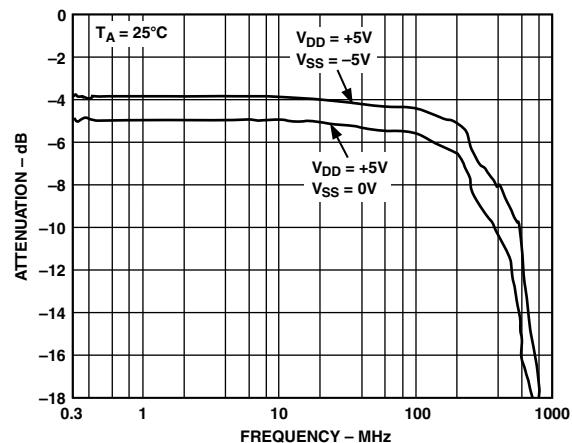
TPC 7. Charge Injection vs. Source Voltage



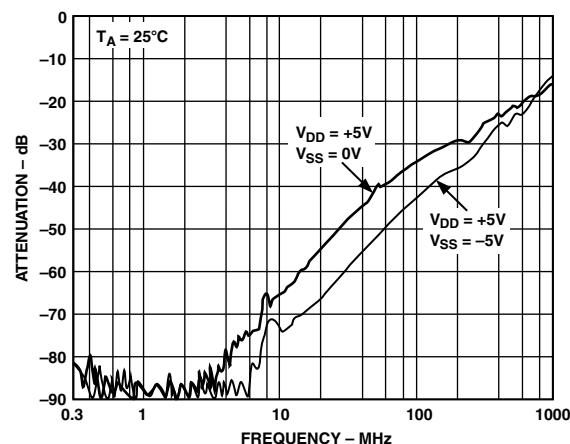
TPC 10. Crosstalk vs. Frequency



TPC 8. t_{ON}/t_{OFF} Times vs. Temperature

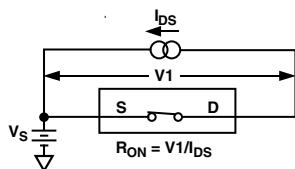


TPC 11. On Response vs. Frequency

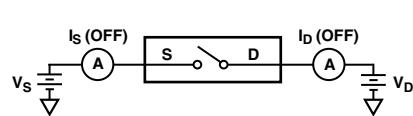


TPC 9. Off Isolation vs. Frequency

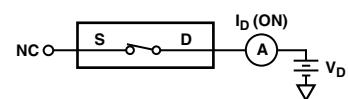
Test Circuits



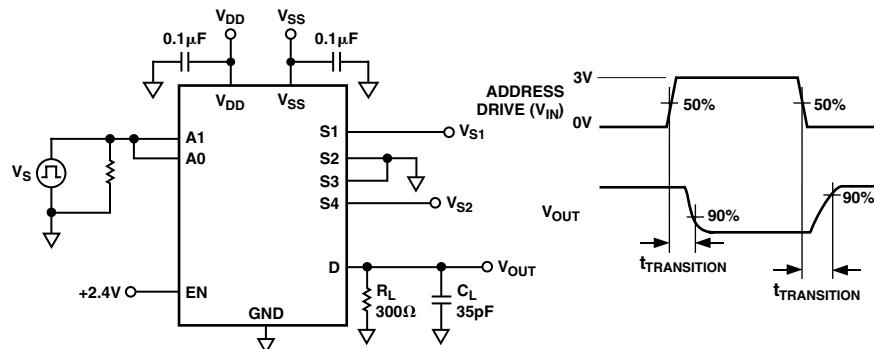
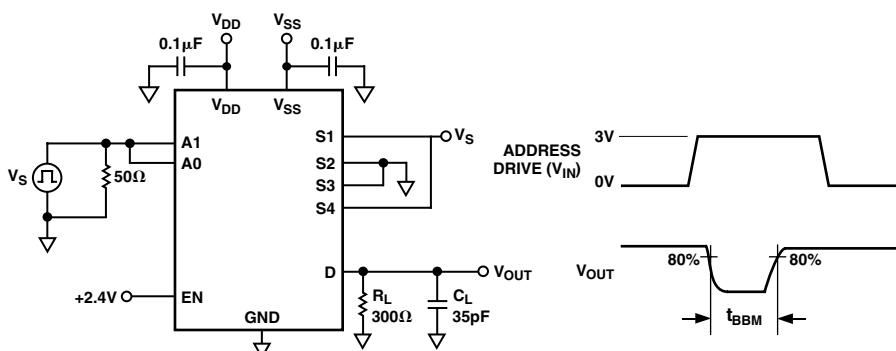
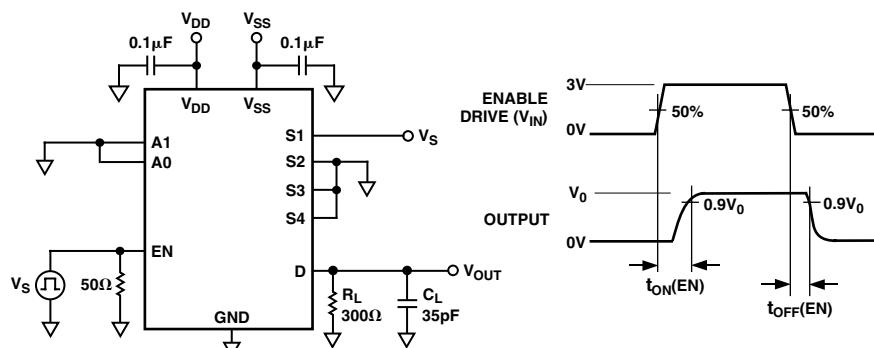
Test Circuit 1. On Resistance



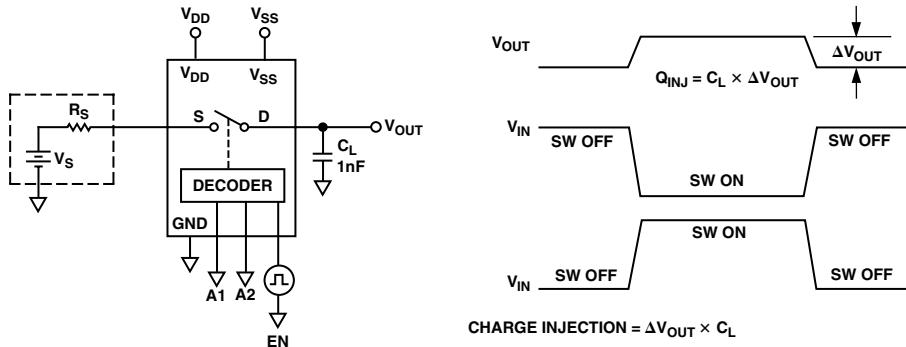
Test Circuit 2. Off Leakage



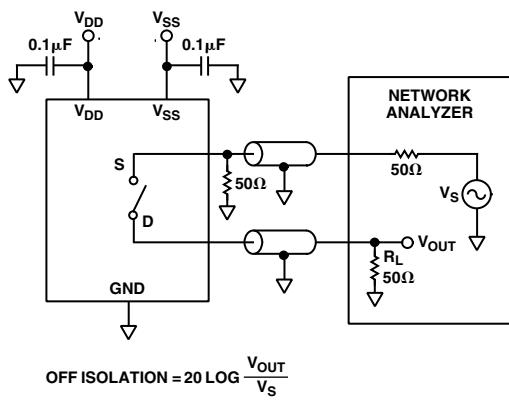
Test Circuit 3. On Leakage

Test Circuit 4. Switching Time of Multiplexer, $t_{TRANSITION}$ Test Circuit 5. Break-Before-Make Delay, t_{BBM} Test Circuit 6. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

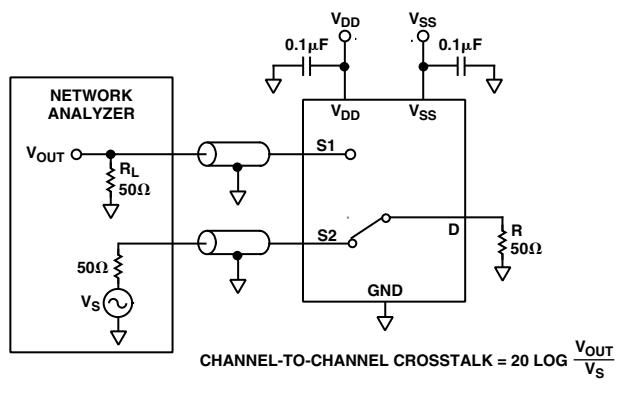
ADG604



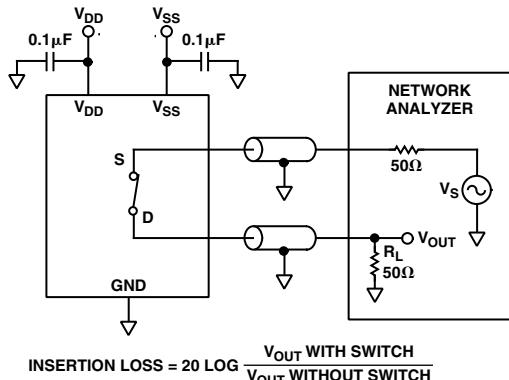
Test Circuit 7. Charge Injection



Test Circuit 8. Off Isolation

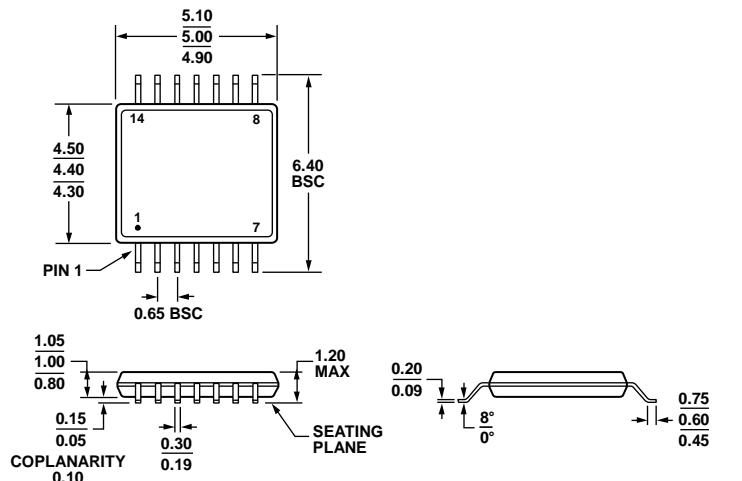


Test Circuit 10. Channel-to-Channel Crosstalk



Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 1. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

061908-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG604YRUZ	–40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG604YRUZ-REEL7	–40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14

¹ Z = RoHS Compliant Part.

REVISION HISTORY

7/2018—Rev. 0 to Rev. A

Changed Automotive Temperature Range: –40°C to +125°C to Temperature Range: –40°C to +125°C	1
Deleted Note 2, Dual Supply Table; Renumbered Sequentially	2
Deleted Note 2, Single Supply Table; Renumbered Sequentially	3
Deleted Note 2, Single Supply Table; Renumbered Sequentially	4
Changed Operating Temperature Range, Automotive (Y Version) to Operating Temperature Range, (Y Version); Absolute Maximum Ratings Table	5
Updated Outline Dimensions.....	11
Moved Ordering Guide	11
Changes to Ordering Guide.....	11

2/2002—Revision 0: Initial Version