

ADG506A/ADG507A—SPECIFICATIONS

Dual Supply ($V_{DD} = +10.8 \text{ V}$ to $+16.5 \text{ V}$, $V_{SS} = -10.8 \text{ V}$ to -16.5 V unless otherwise noted)

	ADG506A ADG507A K Version −40°C to		ADG506A ADG507A B Version −40°C to		ADG506A ADG507A T Version −55°C to			
Parameter	+25°C	+85°C	+25°C	+85°C	+25°C	+125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V min V max	−10 V ≤ V _S ≤ +10 V, I _{DS} = 1 mA; Test Circuit 1 V _{DD} = 15 V (±10%), V _{SS} = −15 V (±10%) V _{DD} = 15 V (±5%), V _{SS} = −15 V (±5%)
R _{ON}	280 450 300	600 400	280 450 300	600 400	280 450 300	600 400	Ω typ Ω max Ω max	
R _{ON} Drift	0.6		0.6		0.6		%/°C typ	
R _{ON} Match	5		5		5		% typ	
I _S (OFF), Off Input Leakage	0.02 1	50	0.02 1	50	0.02 1	50	nA typ nA max	
I _D (OFF), Off Output Leakage	0.04 1	200	0.04 1	200	0.04 1	200	nA typ nA max	V ₁ = ±10 V, V ₂ = ∓10 V; Test Circuit 3
ADG506A	1	100	1	100	1	100	nA max	V ₁ = ±10 V, V ₂ = ∓10 V; Test Circuit 4
ADG507A	1	100	1	100	1	100	nA max	
I _D (ON), On Channel Leakage	0.04 1 1	200 200 100	0.04 1 1	200 200 100	0.04 1 1	200 200 100	nA typ nA max nA max	
I _{DIFF} , Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	V ₁ = ±10 V, V ₂ = ∓10 V; Test Circuit 5
DIGITAL CONTROL								
V _{INH} , Input High Voltage		2.4		2.4		2.4	V min	V _{IN} = 0 to V _{DD}
V _{INL} , Input Low Voltage		0.8		0.8		0.8	V max	
I _{INL} or I _{INH}		1		1		1	μA max	
C _{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
t _{TRANSITION} ¹	200 300 400		200 300 400		200 300 400		ns typ ns max	V ₁ = ±10 V, V ₂ = +10 V; Test Circuit 6
t _{OPEN} ¹	50 25 10		50 25 10		50 25 10		ns typ ns min	Test Circuit 7
t _{ON} (EN) ¹	200 300 400		200 300 400		200 300 400		ns typ ns max	Test Circuit 8
t _{OFF} (EN) ¹	200 300 400		200 300 400		200 300 400		ns typ ns max	Test Circuit 8
OFF Isolation	68 50		68 50		68 50		dB typ dB min	V _{EN} = 0.8 V, R _L = 1 kΩ, C _L = 15 pF, V _S = 7 V rms, f = 100 kHz
C _S (OFF)	5		5		5		pF typ	V _{EN} = 0.8 V
C _D (OFF)								
ADG506A	44		44		44		pF typ	V _{EN} = 0.8 V
ADG507A	22		22		22		pF typ	
Q _{INJ} , Charge Injection	4		4		4		pC typ	R _S = 0 Ω, V _S = 0 V; Test Circuit 9
POWER SUPPLY								
I _{DD}	0.6		0.6		0.6		mA typ	V _{IN} = V _{INL} or V _{INH}
		1.5		1.5		1.5	mA max	V _{IN} = V _{IN} or V _{INH}
I _{SS}	20		20		20		μA typ	
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTES

¹Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Single Supply ($V_{DD} = +10.8 \text{ V to } +16.5 \text{ V}$, $V_{SS} = \text{GND} = 0 \text{ V}$ unless otherwise noted)

	ADG506A ADG507A K Version -40°C to		ADG506A ADG507A B Version -40°C to		ADG506A ADG507A T Version -55°C to			
Parameter	+25°C	+85°C	+25°C	+85°C	+25°C	+125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V _{SS} V _{DD}	V min V max	0 V ≤ V _S ≤ +10 V, I _{DS} = 0.5 mA; Test Circuit 1
R _{ON}	500	1000	500	1000	500	1000	Ω typ Ω max	
R _{ON} Drift	0.6		0.6		0.6		%/°C typ	
R _{ON} Match	5		5		5		% typ	
I _S (OFF), Off Input Leakage	0.02 1	50	0.02 1	50	0.02 1	50	nA typ nA max	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 2
I _D (OFF), Off Output Leakage	0.04 1	200	0.04 1	200	0.04 1	200	nA typ nA max	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 3
ADG506A	1	100	1	100	1	100	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I _D (ON), On Channel Leakage	0.04 1	200	0.04 1	200	0.04 1	200	nA typ nA max	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I _{DIFF} , Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 5
DIGITAL CONTROL								
V _{INH} , Input High Voltage		2.4		2.4		2.4	V min	V _{IN} = 0 to V _{DD}
V _{INL} , Input Low Voltage		0.8		0.8		0.8	V max	
I _{INL} or I _{INH}		1		1		1	μA max	
C _{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
t _{TRANSITION} ¹	300 450	600	300 450	600	300 450	600	ns typ ns max	V1 = +10 V/0 V, V2 = +10 V; Test Circuit 6
t _{OPEN} ¹	50 25	10	50 25	10	50 25	10	ns typ ns min	Test Circuit 7
t _{ON} (EN) ¹	250 450	600	250 450	600	250 450	600	ns typ ns max	Test Circuit 8
t _{OFF} (EN) ¹	250 450	600	250 450	600	250 450	600	ns typ ns max	Test Circuit 8
OFF Isolation	68 50		68 50		68 50		dB typ dB min	V _{EN} = 0.8 V, R _L = 1 kΩ, C _L = 15 pF, V _S = 3.5 V rms, f = 100 kHz
C _S (OFF)	5		5		5		pF typ	V _{EN} = 0.8 V
C _D (OFF)								
ADG506A	44		44		44		pF typ	V _{EN} = 0.8 V
ADG507A	22		22		22		pF typ	
Q _{INJ} , Charge Injection	4		4		4		pC typ	R _S = 0 Ω, V _S = 0 V; Test Circuit 9
POWER SUPPLY								
I _{DD}	0.6	1.5	0.6	1.5	0.6	1.5	mA typ mA max	V _{IN} = V _{INL} or V _{INH}
Power Dissipation	10	25	10	25	10	25	mW typ mW max	

NOTES

¹Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Truth Table (ADG506A)

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table (ADG507A)

A2	A1	A0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

ADG506A/ADG507A

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted)

V _{DD} to V _{SS}	44 V
V _{DD} to GND	25 V
V _{SS} to GND	-25 V
Analog Inputs ²	
Voltage at S, D	V _{SS} - 2 V to V _{DD} + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D	20 mA
Pulsed Current S or D	40 mA
1 ms Duration, 10% Duty Cycle	
Digital Inputs ²	
Voltage at A, EN	V _{SS} - 4 V to V _{DD} + 4 V or 20 mA, Whichever Occurs First

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG506A/ADG507A feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Power Dissipation (Any Package)

Up to +75°C	470 mW
Derates above +75°C by	6 mW/°C

Operating Temperature

Commercial (K Version)	-40°C to +85°C
Industrial (B Version)	-40°C to +85°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

NOTES

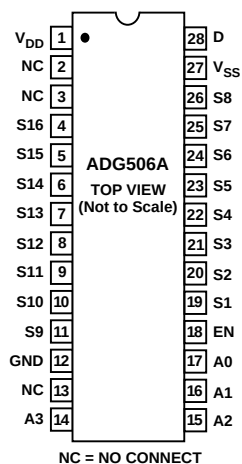
¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

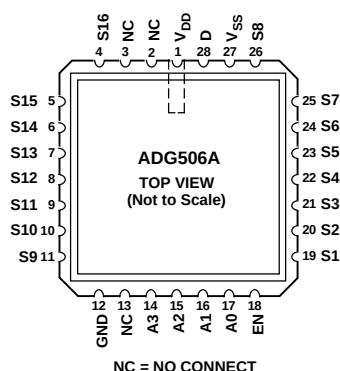


PIN CONFIGURATIONS

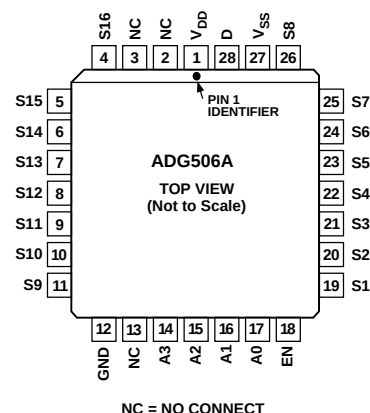
DIP, SOIC



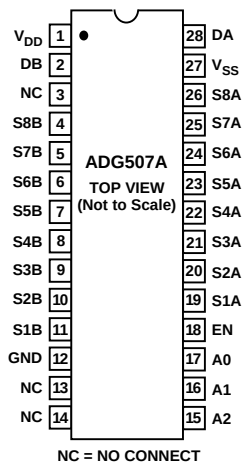
LCCC



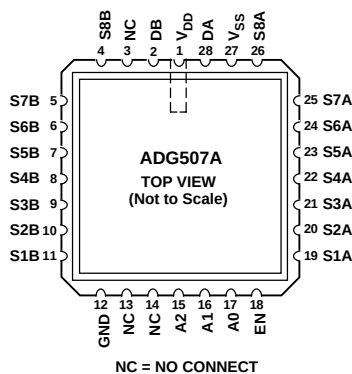
PLCC



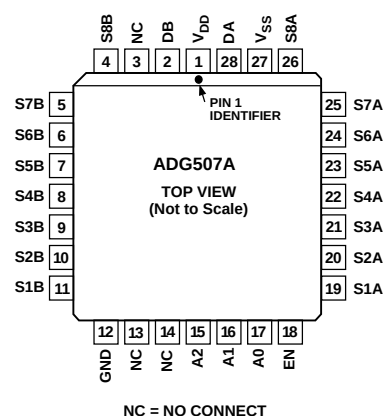
DIP, SOIC, TSSOP



LCCC



PLCC



Typical Performance Characteristics—ADG506A/ADG507A

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

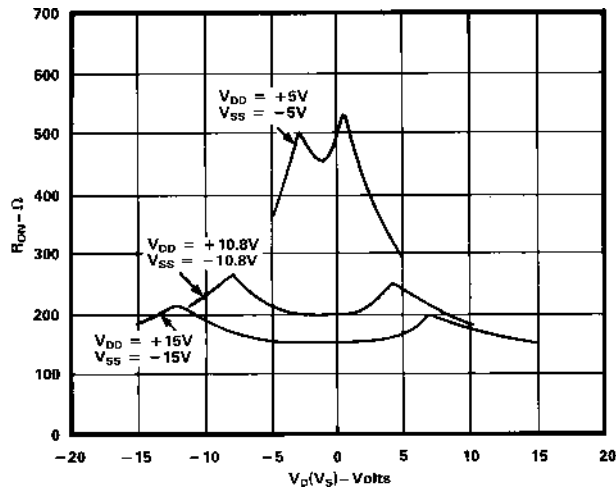


Figure 1. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage, $T_A = +25^\circ\text{C}$

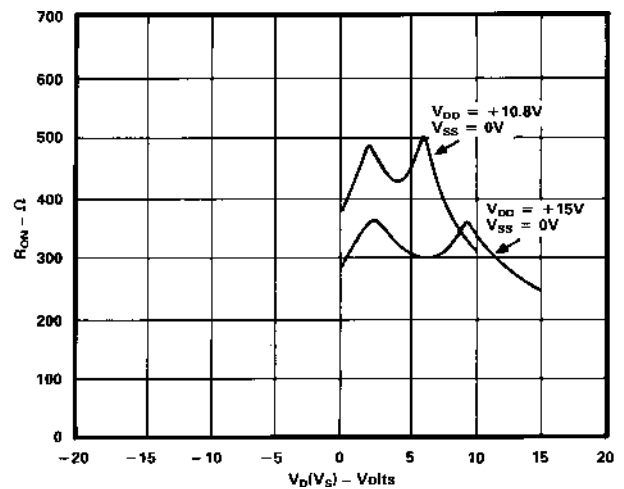


Figure 4. R_{ON} as a Function of V_D (V_S) Single Supply Voltage, $T_A = +25^\circ\text{C}$

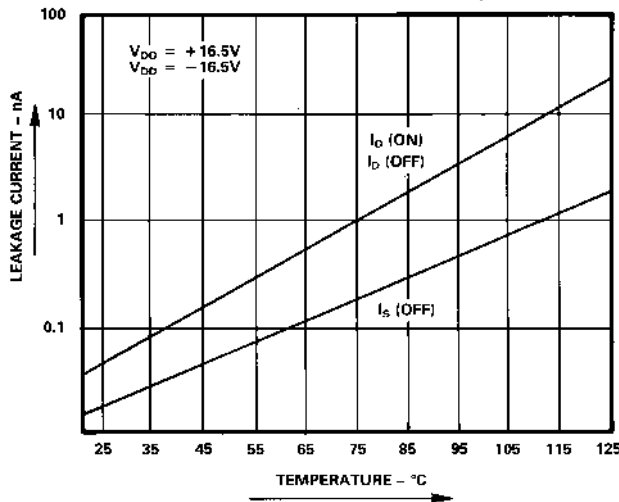


Figure 2. Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

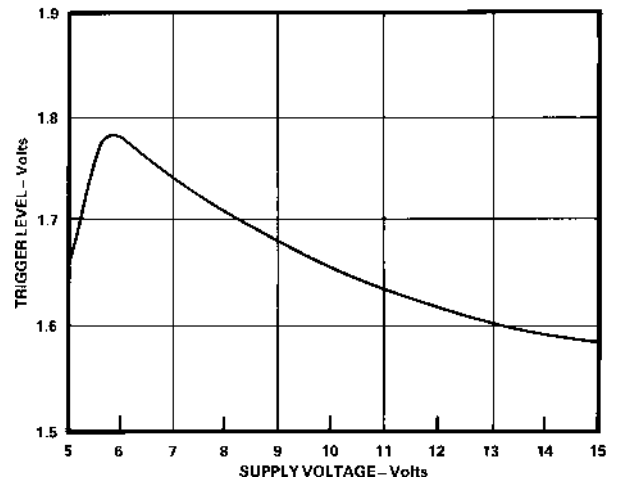


Figure 5. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, $T_A = +25^\circ\text{C}$

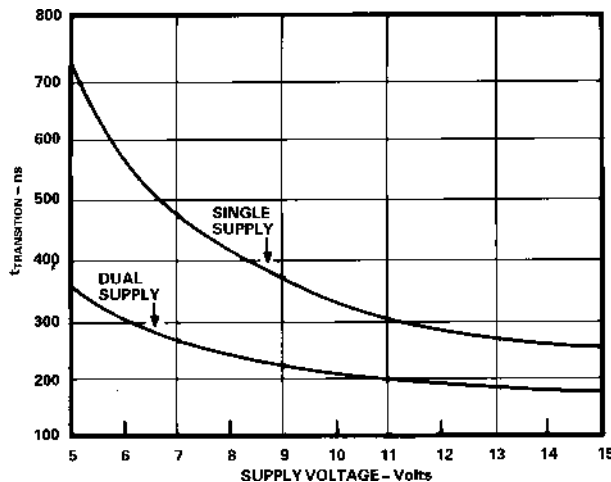


Figure 3. $t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, $T_A = +25^\circ\text{C}$ (Note: For V_{DD} and $|V_{SS}| < 10\text{ V}$; $V1 = V_{DD}/V_{SS}$, $V2 = V_{SS}/V_{DD}$. See Test Circuit 6)

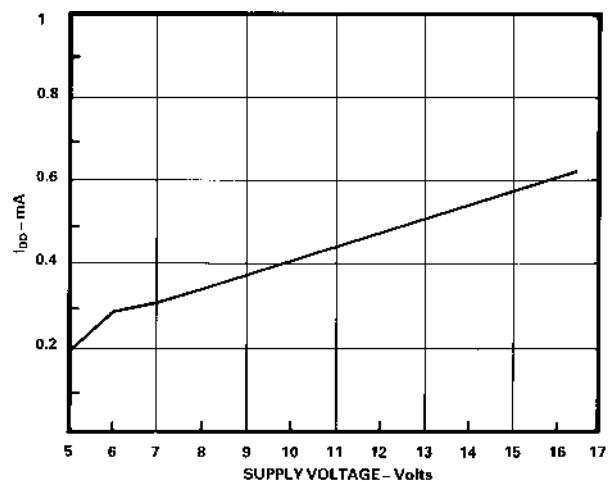
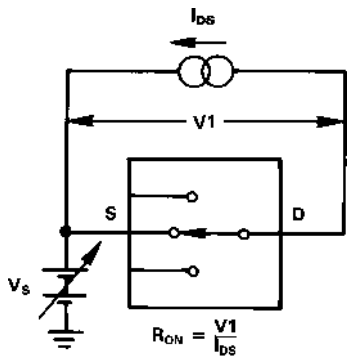


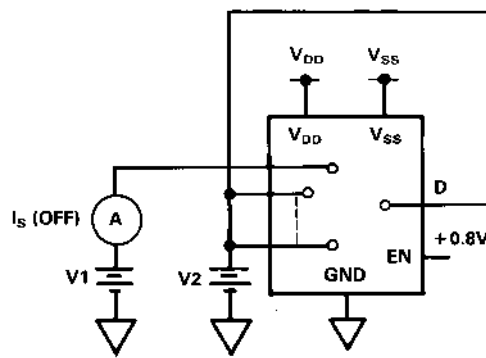
Figure 6. I_{DD} vs. Supply Voltage: Dual or Single Supply, $T_A = +25^\circ\text{C}$

ADG506A/ADG507A—Test Circuits

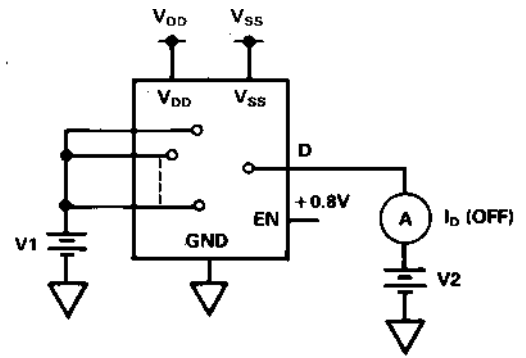
Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.



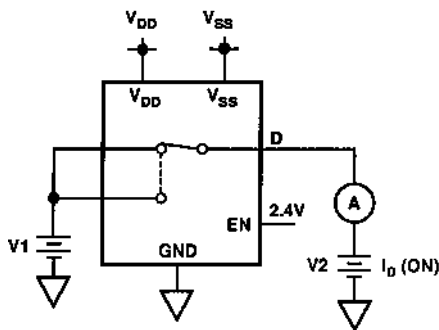
Test Circuit 1. R_{ON}



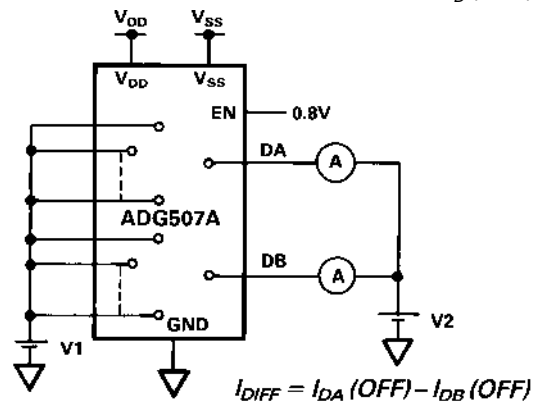
Test Circuit 2. I_S (OFF)



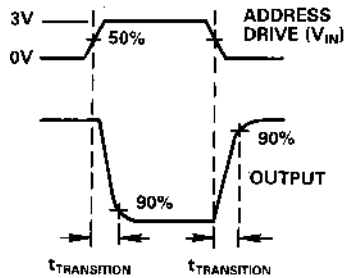
Test Circuit 3. I_D (OFF)



Test Circuit 4. I_D (ON)

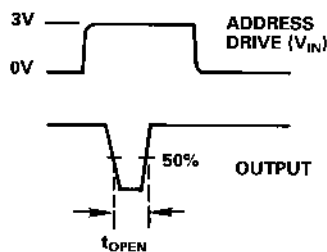
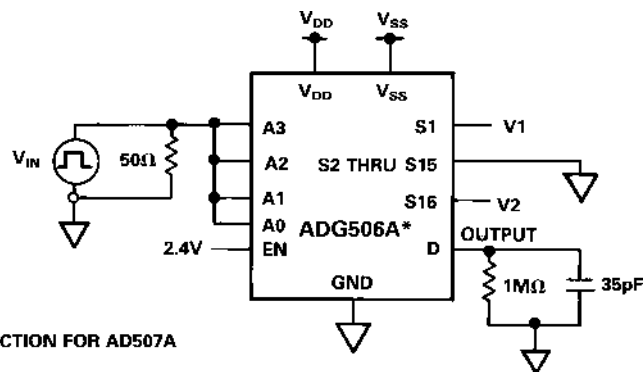


Test Circuit 5. I_{DIFF}



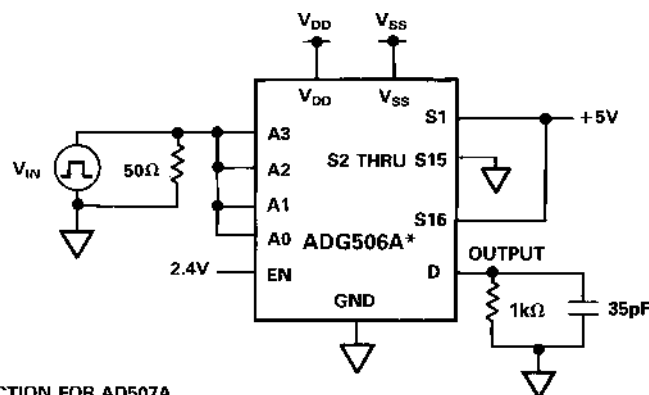
*SIMILAR CONNECTION FOR AD507A

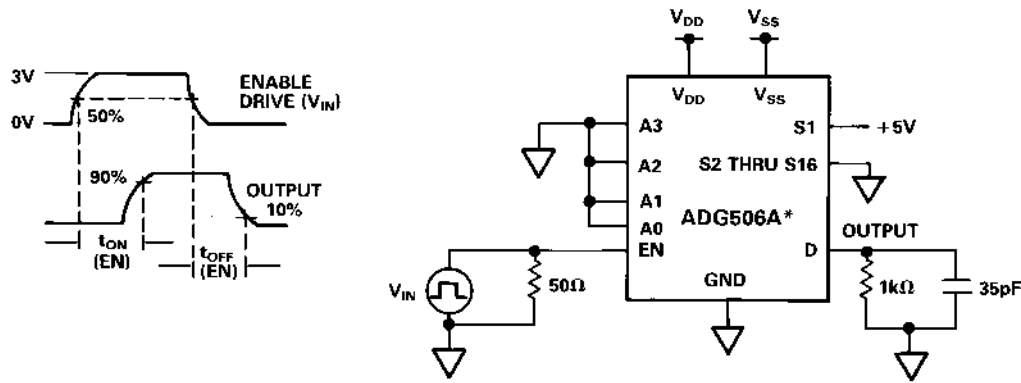
Test Circuit 6. Switching Time of Multiplexer, $t_{TRANSITION}$



*SIMILAR CONNECTION FOR AD507A

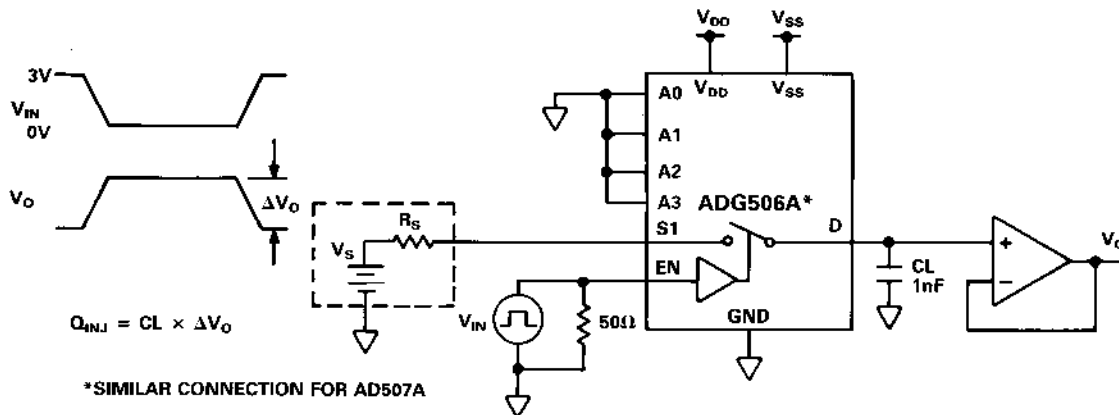
Test Circuit 7. Break-Before-Make Delay, t_{OPEN}





*SIMILAR CONNECTION FOR AD507A

Test Circuit 8. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$



*SIMILAR CONNECTION FOR AD507A

Test Circuit 9. Charge Injection

SINGLE SUPPLY AUTOMOTIVE APPLICATION

The excellent performance of the multiplexers under single supply conditions makes the ADG506A/ADG507A suitable in applications such as automotive and disc drives where only positive power supply voltages are normally available. The following application circuit shows the ADG507A connected as an 8-channel differential multiplexer in an automotive, data acquisition application circuit.

The AD7580 is a 10-bit successive approximation ADC, which has an on-chip sample-and-hold amplifier and provides a conversion result in 20 μ s. The ADC has differential analog inputs and is configured in the application circuit for a span of 2.5 V over a common-mode range 0 V to +5 V. Wider common-mode ranges can be accommodated. See the AD7579/AD7580 data sheet for more details. The complete system operates from +12 V (+10%) and +5 V supplies. The analog input signals to the ADG507A contain information such as temperature, pressure, speed etc.

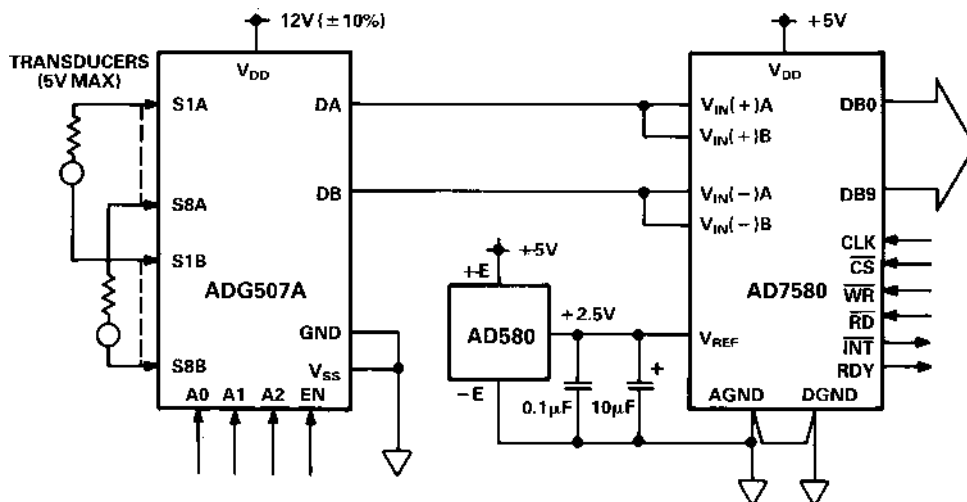


Figure 7. ADG507A in a Single Supply Automotive Data Acquisition Application

C1150c-0-6/98

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for “OFF” condition
C_D (OFF)	Channel output capacitance for “OFF” condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch “ON” condition

$t_{\text{OFF}} (\text{EN})$	Delay time between the 50% and 10% points of the digital input and switch “OFF” condition
$t_{\text{TRANSITION}}$	Delay time between the 50% and 90% points of the digital inputs and switch “ON” condition when switching from one address state to another
t_{OPEN}	“OFF” time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic “0”
V_{INH}	Minimum input voltage for Logic “1”
$I_{\text{INL}} (I_{\text{INH}})$	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

Dimensions shown in inches and (mm).

Technical drawing of the 100-pin connector showing top, side, and detail views with dimensions in inches and millimeters.

Top View Dimensions:

- Overall Width: 0.550 (13.97)
- Width (excluding pins): 0.53 (13.47)
- Overall Length: 1.45 (36.83)
- Length (excluding pins): 1.44 (36.58)

Side View Dimensions:

- Pin Height: 0.2 (5.08) MAX
- Pin Pitch: 0.065 (1.66)
- Pin Width: 0.020 (0.508)
- Pin Spacing: 0.105 (2.67)
- Pin Thickness: 0.015 (0.381)
- Pin Base Width: 0.095 (2.42)
- Pin Base Thickness: 0.175 (4.45)
- Pin Base Spacing: 0.12 (3.05)
- Pin Base Width (excluding pins): 0.008 (0.203)

Detail View Dimensions:

- Overall Width: 0.606 (15.4)
- Width (excluding pins): 0.594 (15.09)
- Pin Height: 0.16 (4.07)
- Pin Width: 0.14 (3.56)
- Pin Angle: 15°

The drawing illustrates the mechanical specifications of the 16-pin package. The top view shows a rectangular body with a maximum width of 1.490 (37.84) and a maximum height of 0.525 (13.33). The side view shows a maximum height of 0.515 (13.08). The cross-sectional view shows a maximum height of 0.18 (4.57) and a maximum width of 0.62 (15.74). The package is shown with a 15° lead angle and a 0° pitch.

Dimensions (inches (millimeters)):

- Top View:
 - Width: 1.490 (37.84) MAX
 - Height: 0.525 (13.33)
 - Height: 0.515 (13.08)
- Side View:
 - Height: 0.125 (3.175) MIN
- Cross-sectional View:
 - Height: 0.18 (4.57) MAX
 - Width: 0.62 (15.74)
 - Width: 0.59 (14.93)
 - Lead Angle: 15°
 - Pitch: 0°
 - Pin Spacing: 0.11 (2.79)
 - Pin Spacing: 0.099 (2.28)
 - Pin Spacing: 0.02 (0.5)
 - Pin Spacing: 0.016 (0.406)
 - Pin Spacing: 0.012 (0.305)
 - Pin Spacing: 0.008 (0.203)

Other labels include: GLASS SEALANT, 0.06 (1.52), 0.05 (1.27), 0.22 (5.59) MAX, and 0.125 (3.175) MIN.

Figure 1: Mechanical drawing of the test chip. The drawing shows a top view and a side view of a rectangular chip with pins. The top view includes dimensions for the overall size (0.7125 (18.10) by 0.6969 (17.70)), pin pitch (0.0125 (0.32)), and pin width (0.0091 (0.23)). The side view shows the chip thickness (0.0118 (0.30)) and the pin height (0.0192 (0.49)). The chip is labeled with 'PIN 1' and 'SEATING PLANE'.

The drawing shows the mechanical specifications for a 28-pin package. The top view is a rectangle with dimensions 0.386 (9.80) inches by 0.256 (6.50) inches. The pin pitch is 0.0378 (9.60) inches. The pin diameter is 0.0177 (4.50) inches. The package is labeled with 28, 15, 14, and 1. The side view shows the package height as 0.169 (4.30) inches. The pin height is 0.246 (6.25) inches. The pin diameter is 0.006 (0.15) inches. The pin pitch is 0.002 (0.05) inches. The package is labeled with PIN 1, 0.006 (0.15), 0.002 (0.05), 0.0433 (1.10) MAX, 0.0079 (0.20), 0.0035 (0.090), 8° 0', 0.028 (0.70), and 0.020 (0.50).

Figure 1: Dimensions of the test specimen. The figure shows two views of a rectangular specimen: a top view and a bottom view. The top view shows a rectangular plate with a central rectangular hole. Dimensions are given in inches and millimeters. The top view dimensions include: overall width 0.100 (2.54) and 0.064 (1.63); overall height 0.458 (11.63) and 0.442 (11.23); hole width 0.088 (2.24) and 0.054 (1.37); hole height 0.058 (1.48) and 0.045 (1.14); and a 45° chamfer. The bottom view shows the underside of the plate with a central rectangular hole. Dimensions include: overall width 0.300 (7.62) and 0.150 (3.51); overall height 0.075 (1.91) and 0.075 (1.90); hole width 0.075 (1.91) and 0.075 (1.90); hole height 0.011 (0.28) and 0.007 (0.18); and a 45° chamfer. The bottom view is labeled 'BOTTOM VIEW'.