

AD9051—SPECIFICATIONS ($V_D = 5\text{ V}$, $V_{DD} = 3\text{ V}$; external reference = 2.50 V; ENCODE = 60 MSPS unless otherwise noted)

| Parameter | Temp | Test Level | AD9051BRS/ AD9051BRSZ | | | AD9051BRS-2V/ AD9051BRSZ-2V | | | Unit |
|--|------|------------|--------------------------|--------|------|--------------------------------|--------|------|---------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | 10 | | | 10 | | | Bits |
| DC ACCURACY | | | | | | | | | |
| Differential Nonlinearity | 25°C | I | | 0.75 | 1.50 | | 0.75 | 1.50 | LSB |
| | Full | V | | 0.90 | | | 0.90 | | LSB |
| Integral Nonlinearity | 25°C | I | | 0.75 | 1.50 | | 0.75 | 1.50 | LSB |
| | Full | V | | 0.90 | | | 0.90 | | LSB |
| No Missing Codes | 25°C | I | GUARANTEED | | | GUARANTEED | | | |
| Gain Error ¹ | 25°C | I | | ±0.3 | ±2.5 | | ±0.3 | ±3.0 | % FS |
| | Full | VI | | | ±5.0 | | | ±5.5 | % FS |
| Gain Tempco ¹ | Full | V | | ±10 | | | ±10 | | ppm/°C |
| ANALOG INPUT | | | | | | | | | |
| Input Voltage Range ² | 25°C | V | | 1.25 | | | 2.0 | | V p-p |
| Input Offset Voltage | 25°C | I | -14 | +5.0 | +26 | -14 | +5.0 | +26 | LSB |
| Input Resistance | 25°C | I | 4.0 | 6.0 | | 4.0 | 6.0 | | kΩ |
| Input Capacitance | 25°C | V | | 5 | | | 5 | | pF |
| Analog Bandwidth (BW SEL +V _D /NC) ³ | 25°C | V | | 50/130 | | | 50/130 | | MHz |
| BANDGAP REFERENCE | | | | | | | | | |
| Output Voltage (I _O @ 200 μA) | Full | VI | 2.4 | 2.5 | 2.6 | 2.4 | 2.5 | 2.6 | V |
| Temperature Coefficient | Full | V | | ±33 | | | ±33 | | ppm/°C |
| Power Supply Sensitivity | Full | V | | 6.2 | | | 6.2 | | mV/V |
| Reference Input Current (V _{IN} = 2.50 V) | Full | VI | | 2.0 | 25 | | 2.0 | 25 | μA |
| SWITCHING PERFORMANCE | | | | | | | | | |
| Maximum Conversion Rate | Full | VI | 60 | | | 60 | | | MSPS |
| Minimum Conversion Rate ⁴ | Full | IV | | 2.0 | 5.0 | | 2.0 | 5.0 | MSPS |
| Aperture Delay (t _A) | 25°C | V | | 2.5 | | | 2.5 | | ns |
| Aperture Uncertainty (Jitter) | 25°C | V | | 5 | | | 5 | | ps, rms |
| Output Valid Time (t _V) ⁵ | Full | VI | 4.0 | | | 4.0 | | | ns |
| Output Propagation Delay (t _{PD}) ⁵ | Full | VI | | 5.5 | 10 | | 5.5 | 10 | ns |
| DYNAMIC PERFORMANCE ⁶ | | | | | | | | | |
| Transient Response | 25°C | V | | 10 | | | 10 | | ns |
| Overvoltage Recovery Time | 25°C | V | | 10 | | | 10 | | ns |
| ENOBs | | | | | | | | | |
| f _{IN} = 1.20 MHz | 25°C | V | | 9.3 | | | 9.1 | | ENOB |
| f _{IN} = 10.3 MHz | 25°C | I | 8.76 | 9.0 | | 8.59 | 8.8 | | ENOB |
| f _{IN} = 29.0 MHz | 25°C | V | | 8.8 | | | 8.6 | | ENOB |
| Signal-to-Noise Ratio (SINAD) | | | | | | | | | |
| f _{IN} = 1.20 MHz | 25°C | V | | 56.5 | | | 56.5 | | dB |
| f _{IN} = 10.3 MHz | 25°C | I | 53.5 | 56 | | 52.5 | 55 | | dB |
| f _{IN} = 29.0 MHz | 25°C | V | | 54 | | | 53 | | dB |
| Signal-to-Noise Ratio (Without Harmonics) | | | | | | | | | |
| f _{IN} = 1.20 MHz | 25°C | V | | 55.5 | | | 56.5 | | dB |
| f _{IN} = 10.3 MHz | 25°C | I | 54.5 | 56.5 | | 53.5 | 55.5 | | dB |
| f _{IN} = 29.0 MHz | 25°C | V | | 55 | | | 54 | | dB |
| 2nd Harmonic Distortion | | | | | | | | | |
| f _{IN} = 1.20 MHz | 25°C | V | | -74 | | | -68 | | dBc |
| f _{IN} = 10.3 MHz | 25°C | I | | -73 | -60 | | -64 | -58 | dBc |
| f _{IN} = 29.0 MHz | 25°C | V | | -67 | | | -60 | | dBc |
| 3rd Harmonic Distortion | | | | | | | | | |
| f _{IN} = 1.20 MHz | 25°C | V | | -74 | | | -69 | | dBc |
| f _{IN} = 10.3 MHz | 25°C | I | | -70 | -60 | | -65 | -60 | dBc |
| f _{IN} = 29.0 MHz | 25°C | V | | -65 | | | -60 | | dBc |
| Two-Tone Intermodulation | | | | | | | | | |
| Distortion (IMD) | 25°C | V | | -65 | | | -65 | | dBc |
| Differential Phase | 25°C | V | | 0.1 | | | 0.1 | | Degrees |
| Differential Gain | 25°C | V | | 0.5 | | | 0.5 | | % |

| Parameter | Temp | Test Level | AD9051BRS/ AD9051BRSZ | | | AD9051BRS-2V/ AD9051BRSZ-2V | | | Unit |
|--|------|------------|--------------------------|-----|------|--------------------------------|-----|------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| ENCODE INPUT | | | | | | | | | |
| Logic "1" Voltage | Full | VI | 2.0 | | | 2.0 | | | V |
| Logic "0" Voltage | Full | VI | | | 0.8 | | | 0.8 | V |
| Logic "1" Current | Full | VI | | | 1 | | | 1 | μA |
| Logic "0" Current | Full | VI | | | 1 | | | 1 | μA |
| Input Capacitance | 25°C | V | | 7.5 | | | 7.5 | | pF |
| Encode Pulsewidth High (t_{EH}) | 25°C | IV | 7.5 | | | 7.5 | | | ns |
| Encode Pulsewidth Low (t_{EL}) | 25°C | IV | 7.5 | | | 7.5 | | | ns |
| DIGITAL OUTPUTS | | | | | | | | | |
| Logic "1" Voltage (5.0 V_{DD}) | Full | VI | 4.95 | | | 4.95 | | | V |
| Logic "0" Voltage (5.0 V_{DD}) | Full | VI | | | 0.05 | | | 0.05 | V |
| Logic "1" Voltage (3.0 V_{DD}) | Full | VI | 2.95 | | | 2.95 | | | V |
| Logic "0" Voltage (3.0 V_{DD}) | Full | VI | | | 0.05 | | | 0.05 | V |
| Output Coding ⁷ | | | Offset Binary | | | Offset Binary | | | |
| POWER SUPPLY | | | | | | | | | |
| V_D , V_{DD} Supply Current | Full | VI | | 50 | 63 | | 50 | 63 | mA |
| Power Dissipation ⁸ | Full | VI | | 250 | 315 | | 250 | 315 | mW |
| Power Supply Rejection Ratio (PSRR) ⁹ | 25°C | I | | ±2 | ±10 | | ±7 | ±15 | mV/V |

NOTES

¹Gain error and gain temperature coefficient are based on the ADC only (with a fixed 2.5 V external reference).

²Contact factory or authorized sales agent for information concerning the availability of expanded input voltage range devices.

³3 dB bandwidth with full-power input signal.

⁴Minimum conversion rate at which all data sheet specifications remain stable.

⁵ t_V and t_{PD} are measured from the threshold crossing of the ENCODE input to valid TTL levels 0.5 V and 2.4 V of the digital outputs with $V_{DD} = 3.0$ V. The output ac load during test is 5 pF.

⁶SNR/harmonics tested with an analog input voltage of -0.5 dBFS. All tests performed at 60 MSPS.

⁷Contact factory or authorized sales agent for information concerning the availability of alternative output coding and input range devices.

⁸Power dissipation is measured under the following conditions: analog input = -FS at 60 MSPS ENCODE.

⁹A change in input offset voltage with respect to a change in V_D .

Specifications subject to change without notice.

AD9051

ABSOLUTE MAXIMUM RATINGS*

| | |
|------------------------------------|-------------------------|
| V_D, V_{DD} | 7 V |
| Analog Inputs | -0.5 V to $V_D + 0.5$ V |
| Digital Inputs | -0.5 V to V_D |
| VREF Input | -0.5 V to V_D |
| Digital Output Current | 20 mA |
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Maximum Case Temperature | 150°C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

Table I. Digital Coding (Single-Ended Input with AIN, AINB Bypassed to GND)

| Analog Input | Voltage Level | OR (Out of Range) | Digital Output MSB . . . LSB |
|---------------|-----------------------------|----------------------|---------------------------------|
| 3.126 (3.50)* | Positive Full Scale + 1 LSB | 1 | 1111111111 |
| 2.5 | Midscale | 0 | 0111111111 |
| 1.874 (1.50)* | Negative Full Scale - 1 LSB | 1 | 0000000000 |

*(BRS-2V Version)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9051 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

| Pin No. | Mnemonic | Description |
|---------------------|-----------------|--|
| 1, 6, 7, 12, 21, 23 | GND | Ground |
| 2, 8, 11 | V _D | Analog 5 V Power Supply |
| 3 | VREFOUT | Internal Bandgap Voltage Reference (Nominally 2.5 V) |
| 4 | VREFIN | Input to Reference Amplifier. Voltage reference for ADC is connected here. |
| 5 | BWSEL | Bandwidth Select. NC = 130 MHz nominal. +V _D = 50 MHz nominal. |
| 9 | AINB | Complementary Analog Input Pin (Analog Input Bar) |
| 10 | AIN | Analog Input Pin |
| 13 | ENCODE | Encode Clock Input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal. |
| 14 | OR | Out of Range Signal. Logic "0" when analog input is in nominal range. Logic "1" when analog input is out of nominal range. |
| 15 | D9 (MSB) | Most Significant Bit of ADC Output |
| 16–19 | D8–D5 | Digital Output Bits of ADC |
| 20, 22 | V _{DD} | Digital Output Power Supply (Only Used by Digital Outputs) |
| 24–27 | D4–D1 | Digital Output Bits of ADC |
| 28 | D0 (LSB) | Least Significant Bit of ADC Output |

PIN CONFIGURATION

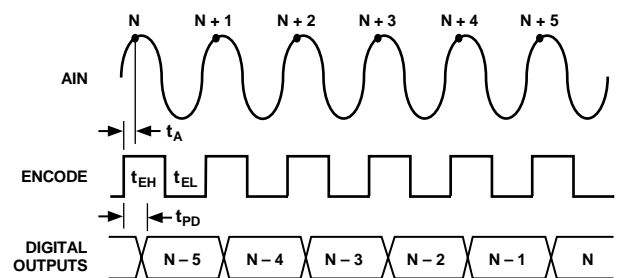
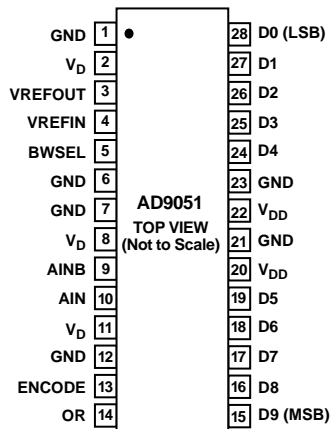


Figure 1. Timing Diagram

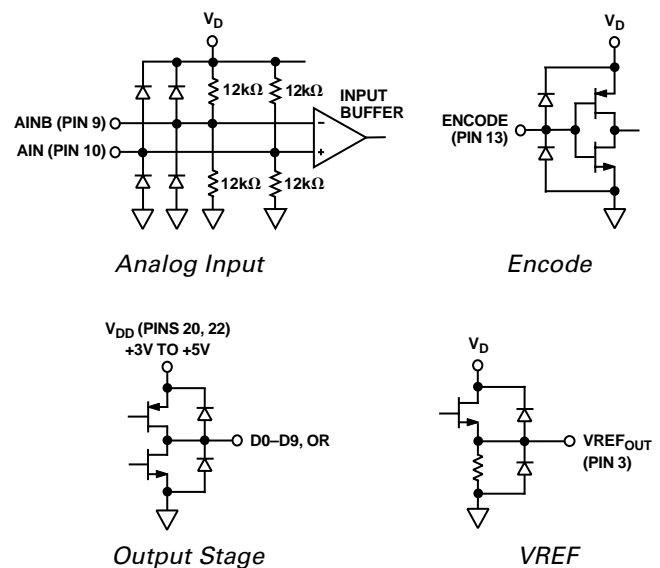
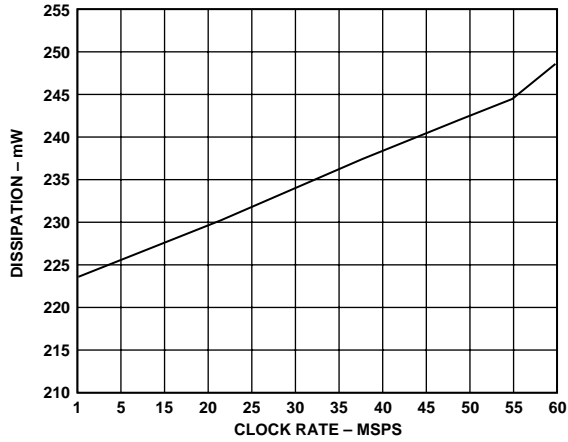
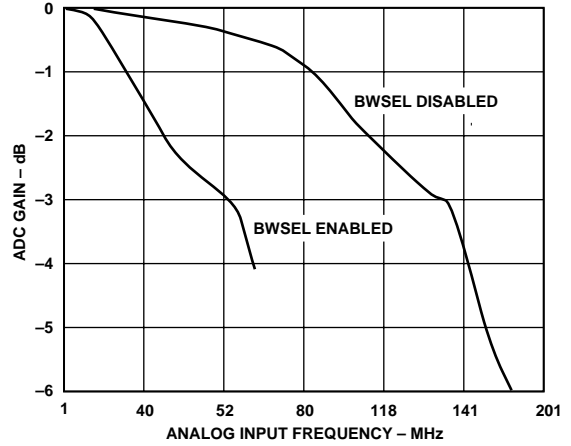


Figure 2. Equivalent Circuits

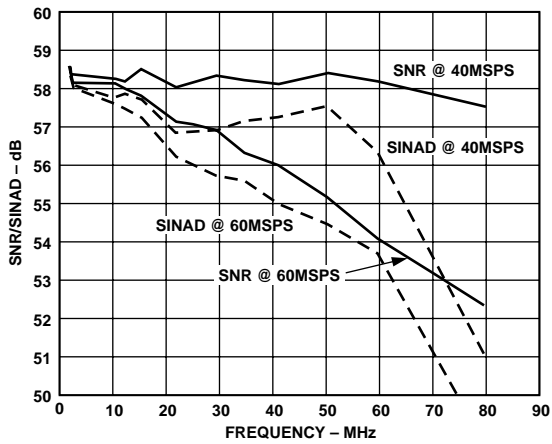
AD9051



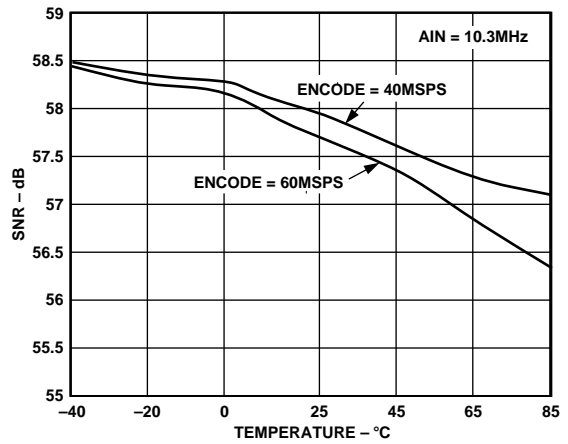
TPC 1. Power Dissipation vs. Clock Rate



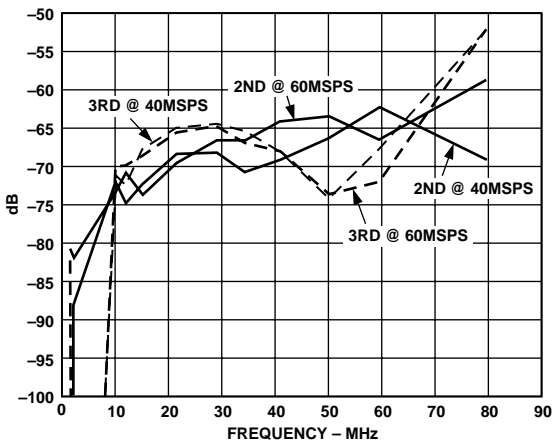
TPC 4. ADC Gain vs. AIN Frequency



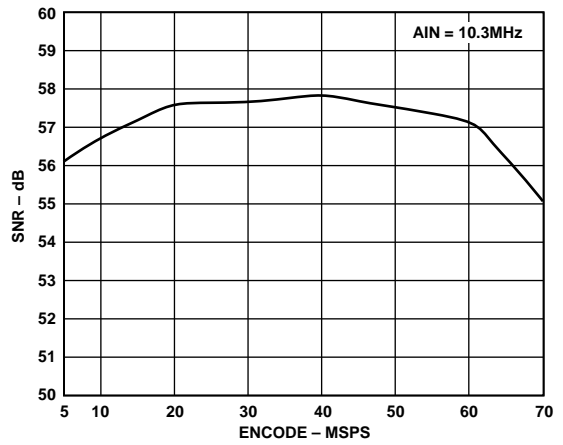
TPC 2. SNR/SINAD vs. AIN Frequency



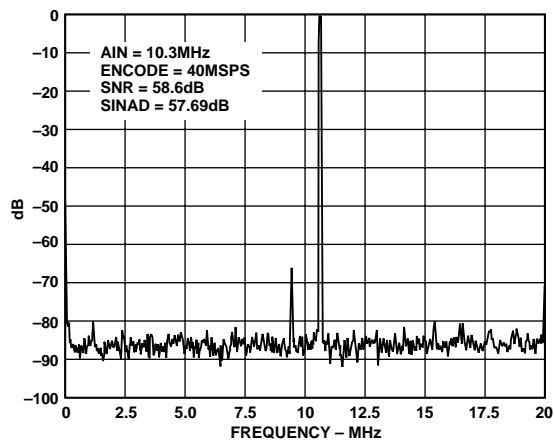
TPC 5. SNR vs. Temperature



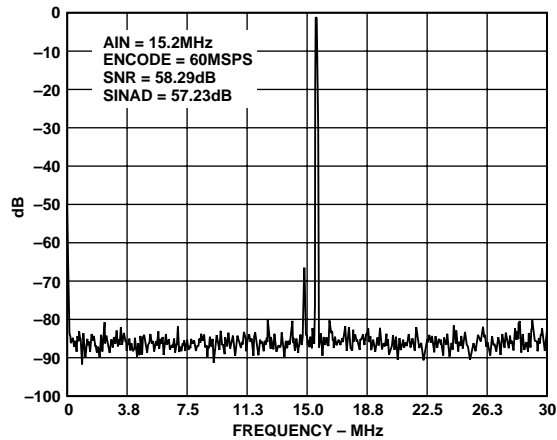
TPC 3. Harmonics vs. AIN Frequency



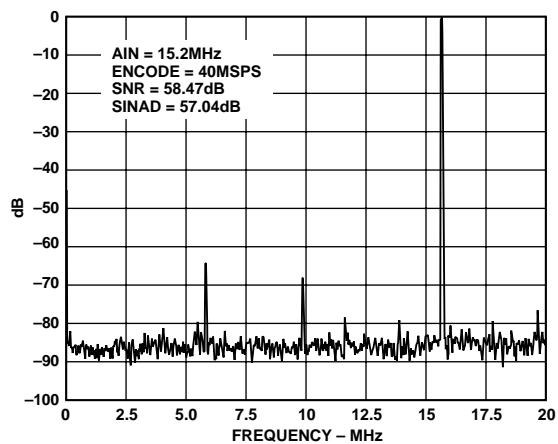
TPC 6. SNR vs. Clock Rate



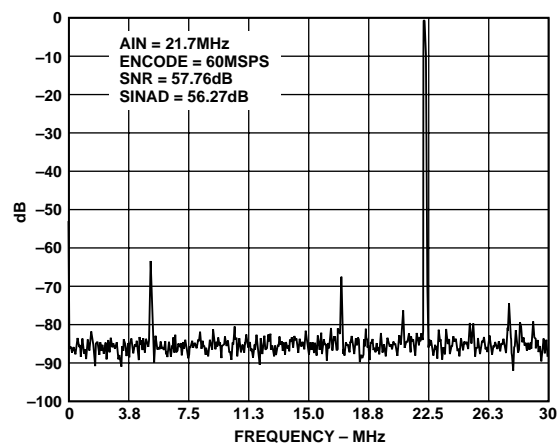
TPC 7. FFT Plot 40 MSPS, 10.3 MHz



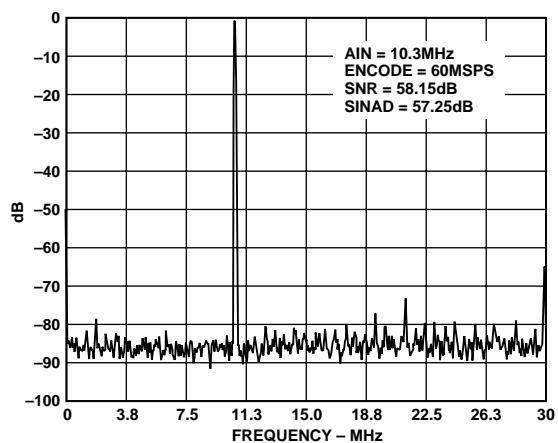
TPC 10. FFT Plot 60 MSPS, 15.2 MHz



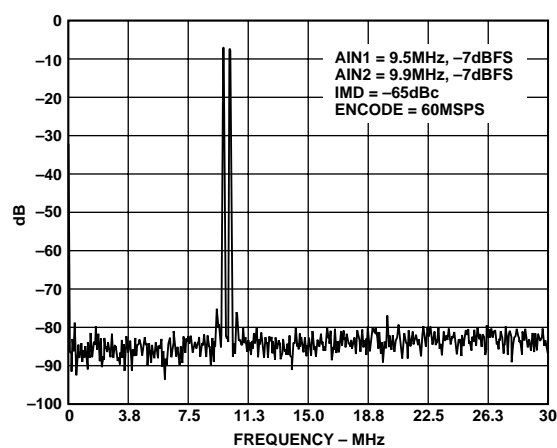
TPC 8. FFT Plot 40 MSPS, 15.2 MHz



TPC 11. FFT Plot 60 MSPS, 21.7 MHz

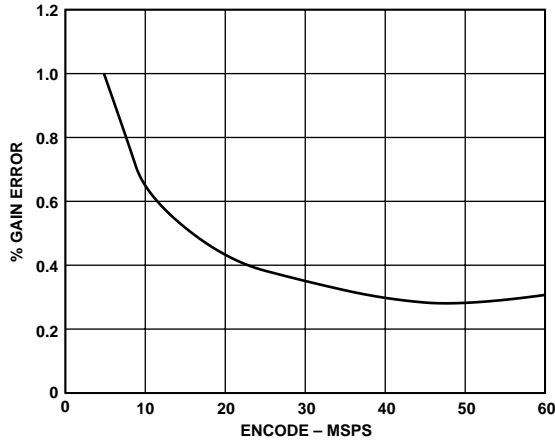


TPC 9. FFT Plot 60 MSPS, 10.3 MHz

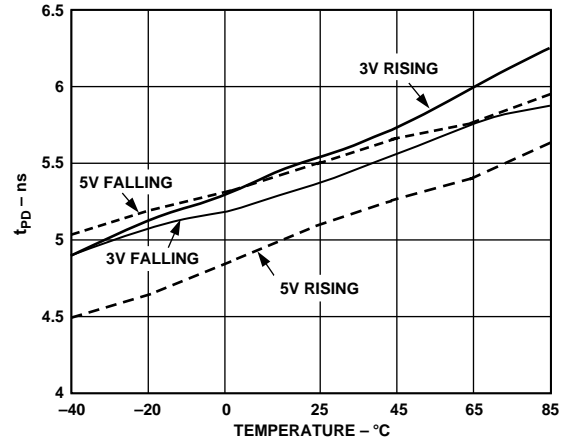


TPC 12. Two-Tone IMD

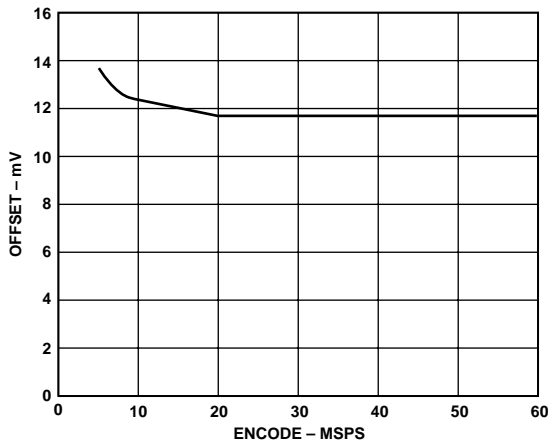
AD9051



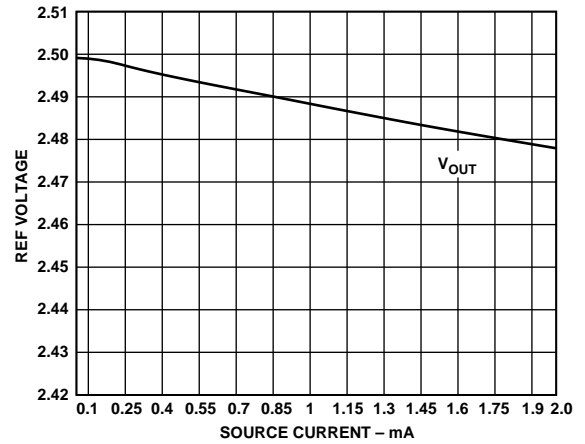
TPC 13. Gain vs. Clock Rate



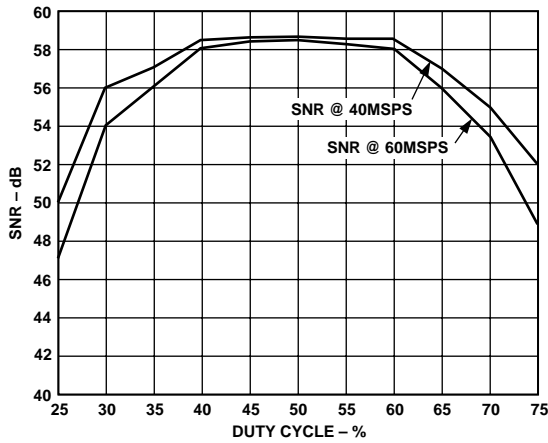
TPC 16. t_{PD} vs. Temperature 3 V/5 V



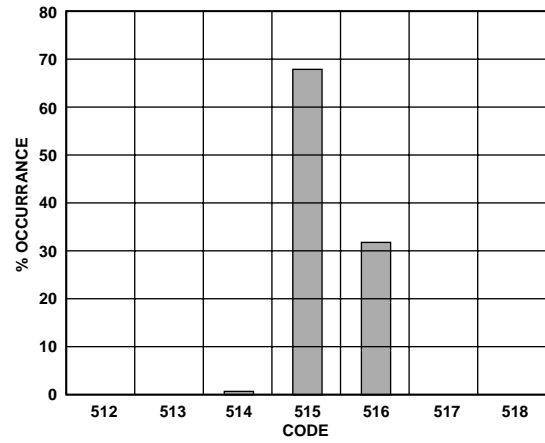
TPC 14. Offset vs. Clock Rate



TPC 17. Reference Load Regulation



TPC 15. SNR vs. Duty Cycle



TPC 18. Midscale Histogram (Inputs Tied)

THEORY OF OPERATION

Refer to the block diagram on the front page.

The AD9051 employs a subranging architecture with digital error correction. This combination of design techniques ensures true 10-bit accuracy at the digital outputs of the converter.

At the input, the analog signal is buffered by a high speed differential buffer and applied to a track-and-hold (T/H) that holds the analog value present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse. The two stage architecture completes a coarse and then a fine conversion of the T/H output signal.

Error correction and decode logic correct and align data from the two conversions and present the result as a 10-bit parallel digital word. Output data are strobed on the rising edge of the ENCODE command. The subranging architecture results in five pipeline delays for the output data. Refer to the AD9051 Timing Diagram.

USING THE AD9051

3 V System

The digital input and outputs of the AD9051 can be easily configured to directly interface to 3 V logic systems. The encode input (Pin 13) is TTL compatible with a logic threshold of 1.5 V. This input is actually a CMOS stage (refer to Equivalent Encode Input Stage) with a TTL threshold, allowing operation with TTL, CMOS and 3 V CMOS logic families. Using 3 V CMOS logic allows the user to drive the encode directly without the need to translate to 5 V. This saves the user power and board space. As with all high speed data converters, the clock signal must be clean and jitter free to prevent the degradation of dynamic performance.

The AD9051 outputs can also directly interface to 3 V logic systems. The digital outputs are standard CMOS stages (refer to AD9051 Output Stage) with isolated supply pins (Pins 20, 22 V_{DD}). By varying the voltage on the V_{DD} pins, the digital output levels vary respectively. By connecting Pins 20 and 22 to the 3 V logic supply, the AD9051 will supply 3 V output levels. Care should be taken to filter and isolate the output supply of the AD9051 as noise could be coupled into the ADC, limiting performance.

Analog Input

The analog input of the AD9051 is a differential input buffer (refer to AD9051 Equivalent Analog Input). The differential inputs are internally biased at 2.5 V, obviating the need for external biasing. Excellent performance is achieved whether the analog inputs are driven single-endedly or differentially (for best dynamic performance, impedances at AIN and AINB should match).

Figure 3 shows typical connections for the analog inputs when using the AD9051 in a dc-coupled system with single-ended signals. All components are powered from a single 5 V supply. The AD820 is used to offset the ground referenced input signal to the level required by the AD9051.

AC coupling of the analog inputs of the AD9051 is easily accomplished. Figure 4 shows capacitive coupling of a single-ended signal while Figure 5 shows transformer coupling differentially into the AD9051.

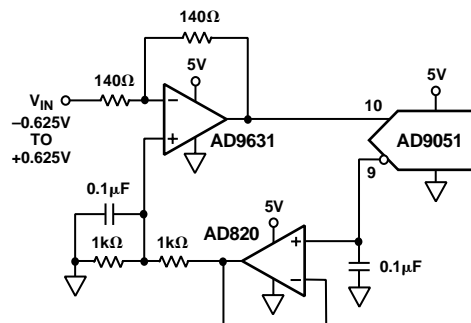


Figure 3. Single Supply, Single-Ended, DC-Coupled AD9051

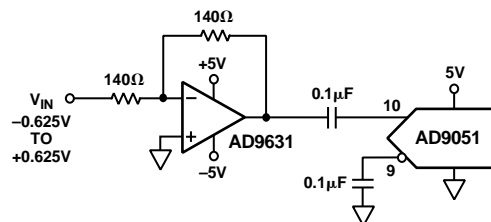


Figure 4. Single-Ended, Capacitively-Coupled AD9051

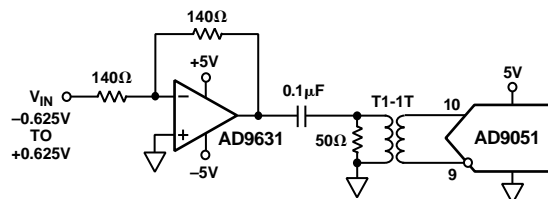


Figure 5. Differentially Driven AD9051 Using Transformer Coupling

The AD830 provides a unique method of providing dc level shift for the analog input. Using the AD830 allows a great deal of flexibility for adjusting offset and gain. Figure 6 shows the AD830 configured to drive the AD9051. The offset is provided by the internal biasing of the AD9051 differential input (Pin 9). For more information regarding the AD830, see the AD830 data sheet.

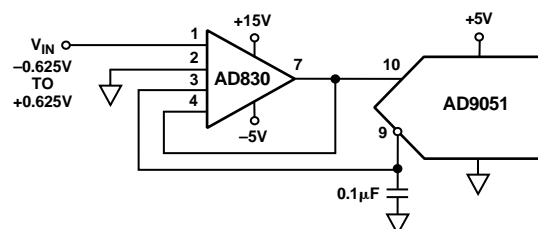


Figure 6. Level-Shifting with the AD830

AD9051

Overdrive of the Analog Input

Special care was taken in the design of the analog input section of the AD9051 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.875 V to 3.125 V (1.25 V p-p centered at 2.5 V). Out-of-range comparators detect when the analog input signal is out of this range and the input buffer is clamped. The digital outputs are locked at their maximum or minimum value (i.e., all “0” or all “1”). This precludes the digital outputs changing to an invalid value when the analog input is out of range.

The input is protected to one volt outside the power supply rails. For nominal power (5 V and ground), the analog input will not be damaged with signals from +5.5 V to -0.5 V.

Timing

The performance of the AD9051 is very insensitive to the duty cycle of the clock. Pulsewidth variations of as much as $\pm 15\%$ for encode rates of 40 MSPS and $\pm 10\%$ for encode rates of 60 MSPS will cause no degradation in performance. (See Figure 17, SNR vs. Duty Cycle.)

The AD9051 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (refer to Figure 1, Timing Diagram). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9051; these transients can detract from the converter's dynamic performance.

Power Dissipation

The power dissipation specification in the parameter table is measured under the following conditions: encode is 60 MSPS, analog input is -FS.

As shown in Figure 3, the actual power dissipation varies based on these conditions. For instance, reducing the clock rate will reduce power as expected for CMOS-type devices. The loading determines the power dissipated in the output stages.

The analog input frequency and amplitude in conjunction with the clock rate determine the switching rate of the output data bits. Power dissipation increases as more data bits switch at faster rates. For instance, if the input is a dc signal that is out of range, no output bits will switch. This minimizes power in the output stages, but is not realistic from a usage standpoint.

The dissipation in the output stages can be minimized by interfacing the outputs to 3 V logic (refer to Using the AD9051, 3 V System). The lower output swings minimize power consumption as follows: $(1/2 C_{LOAD} \times V_{DD}^2 \times \text{Update Rate})$.

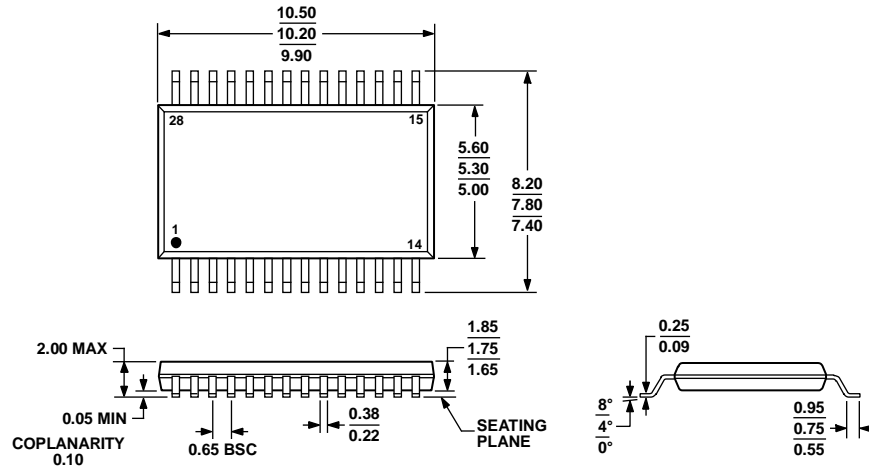
Voltage Reference

A stable and accurate 2.5 V voltage reference is built into the AD9051 (Pin 3, VREFOUT). In normal operation the internal reference is used by strapping together Pins 3 and 4 of the AD9051. The internal reference has 500 μA of extra drive current that can be used for other circuits.

Some applications may require greater accuracy, improved temperature performance, or adjustment of the gain of the AD9051, which cannot be obtained by using the internal reference. For these applications, an external 2.5 V reference can be used to connect to Pin 4 of the AD9051. The VREFIN requires 2 μA of drive current.

The input range can be adjusted by varying the reference voltage applied to the AD9051. No appreciable degradation in performance occurs when the reference is adjusted $\pm 5\%$. The full-scale range of the ADC tracks reference voltage changes linearly.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AH

Figure 7.28-Lead Shrink Small Outline Package [SSOP] (RS-28)

Dimensions shown in millimeters

060106-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| AD9051BRS | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRS-2V | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRSRL | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRSZ | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRSZRL | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRSRL-2V | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRSZ-2V | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |
| AD9051BRSZRL-2V | -40°C to +85°C | 28-Lead Shrink Small Outline Package (SSOP) | RS-28 |

¹ Z = RoHS Compliant Part.

REVISION HISTORY

11/10—Rev. B to Rev. C

- Changes to Specifications Section.....2
- Deleted Evaluation Board Section10
- Updated Outline Dimensions.....11
- Changes to Ordering Guide.....11

7/01—Rev. A to Rev. B

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