

AD818* PRODUCT PAGE QUICK LINKS

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- Universal Evaluation Board for Single High Speed Operational Amplifiers

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Application Notes

- AN-356: User's Guide to Applying and Measuring Operational Amplifier Specifications
- AN-402: Replacing Output Clamping Op Amps with Input Clamping Amps
- AN-417: Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems
- AN-581: Biasing and Decoupling Op Amps in Single Supply Applications
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- AD818: Low Cost, Low Power Video Op Amp Data Sheet

User Guides

- UG-135: Evaluation Board for Single, High Speed Operational Amplifiers (8-Lead SOIC and Exposed Paddle)

TOOLS AND SIMULATIONS

- Analog Filter Wizard
- Analog Photodiode Wizard
- Power Dissipation vs Die Temp
- VRMS/dBm/dBu/dBV calculators
- AD818 SPICE Macro Models

REFERENCE MATERIALS

Product Selection Guide

- High Speed Amplifiers Selection Table

Tutorials

- MT-032: Ideal Voltage Feedback (VFB) Op Amp
- MT-033: Voltage Feedback Op Amp Gain and Bandwidth
- MT-047: Op Amp Noise
- MT-048: Op Amp Noise Relationships: 1/f Noise, RMS Noise, and Equivalent Noise Bandwidth
- MT-049: Op Amp Total Output Noise Calculations for Single-Pole System
- MT-050: Op Amp Total Output Noise Calculations for Second-Order System
- MT-052: Op Amp Noise Figure: Don't Be Misled
- MT-056: High Speed Voltage Feedback Op Amps
- MT-058: Effects of Feedback Capacitance on VFB and CFB Op Amps
- MT-059: Compensating for the Effects of Input Capacitance on VFB and CFB Op Amps Used in Current-to-Voltage Converters
- MT-060: Choosing Between Voltage Feedback and Current Feedback Op Amps

DESIGN RESOURCES

- AD818 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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AD818—SPECIFICATIONS

(@ $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Conditions	V _S	AD818A			Unit
			Min	Typ	Max	
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	Gain = +2	±5 V	70	95		MHz
		±15 V	100	130		MHz
		0 V, +5 V	40	55		MHz
Bandwidth for 0.1 dB Flatness	Gain = –1	±5 V	50	70		MHz
		±15 V	70	100		MHz
		0 V, +5 V	30	50		MHz
	Gain = +2 C _C = 2 pF	±5 V	20	43		MHz
		±15 V	40	55		MHz
		0 V, +5 V	10	18		MHz
Full Power Bandwidth*	Gain = –1 C _C = 2 pF	±5 V	18	34		MHz
		±15 V	40	72		MHz
	V _{OUT} = 5 V p-p R _{LOAD} = 500 Ω V _{OUT} = 20 V p-p R _{LOAD} = 1 kW	0 V, +5 V	10	19		MHz
		±5 V		25.5		MHz
Slew Rate	R _{LOAD} = 1 kW Gain = –1	±15 V		8.0		MHz
		±5 V	350	400		V/μs
		±15 V	450	500		V/μs
		0 V, +5 V	250	300		V/μs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
Settling Time to 0.01%	0 V–10 V Step, A _V = –1	±15 V		45		ns
	–2.5 V to +2.5 V	±5 V		80		ns
Total Harmonic Distortion	0 V–10 V Step, A _V = –1	±15 V		80		ns
	F _C = 1 MHz	±15 V		63		dB
Differential Gain Error (R _L = 150 Ω)	NTSC	±15 V		0.005	0.01	%
	Gain = +2	±5 V		0.01	0.02	%
		0 V, +5 V		0.08		%
Differential Phase Error (R _L = 150 Ω)	NTSC	±15 V		0.045	0.09	Degrees
	Gain = +2	±5 V		0.06	0.09	Degrees
		0 V, +5 V		0.1		Degrees
Cap Load Drive				10		pF
INPUT OFFSET VOLTAGE						
Offset Drift	T _{MIN} to T _{MAX}	±5 V to ±15 V		0.5	2	mV
					3	mV
				10		mV/°C
INPUT BIAS CURRENT						
	T _{MIN} T _{MAX}	±5 V, ±15 V		3.3	6.6	μA
					10	μA
					4.4	μA
INPUT OFFSET CURRENT						
Offset Current Drift	T _{MIN} to T _{MAX}	±5 V, ±15 V		25	300	nA
					500	nA
				0.3		nA/°C
OPEN-LOOP GAIN						
	V _{OUT} = ±2.5 V R _{LOAD} = 500 Ω T _{MIN} to T _{MAX} R _{LOAD} = 150 Ω	±5 V	3	5		V/mV
			2			V/mV
			2	4		V/mV
	V _{OUT} = ±10 V R _{LOAD} = 1 kW T _{MIN} to T _{MAX}	±15 V	6	9		V/mV
			3			V/mV
	V _{OUT} = ±7.5 V R _{LOAD} = 150 Ω (50 mA Output)	±15 V				
			3	5		V/mV
COMMON-MODE REJECTION						
	V _{CM} = ±2.5 V	±5 V	82	100		dB
	V _{CM} = ±12 V	±15 V	86	120		dB
	T _{MIN} to T _{MAX}	±15 V	84	100		dB

Parameter	Conditions	V _S	AD818A			Unit
			Min	Typ	Max	
POWER SUPPLY REJECTION	V _S = ±5 V to ±15 V T _{MIN} to T _{MAX}		80	90		dB
			80			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V, ±15 V		10		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V	+3.8	+4.3		V
			−2.7	−3.4		V
		±15 V	+13	+14.3		V
			−12	−13.4		V
		0 V, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
OUTPUT VOLTAGE SWING	R _{LOAD} = 500 W	±5 V	3.3	3.8		±V
	R _{LOAD} = 150 W	±5 V	3.2	3.6		±V
	R _{LOAD} = 1 kW	±15 V	13.3	13.7		±V
	R _{LOAD} = 500 W	±15 V	12.8	13.4		±V
	R _{LOAD} = 500 W	0 V, +5 V	1.5, 3.5			V
	Output Current	±15 V	50			mA
		±5 V	50			mA
	Short-Circuit Current	0 V, +5 V	30			mA
		±15 V		90		mA
INPUT RESISTANCE				300		kW
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			8		W
POWER SUPPLY Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current	T _{MIN} to T _{MAX}	±5 V		7.0	7.5	mA
		±5 V			7.5	mA
	T _{MIN} to T _{MAX}	±15 V			7.5	mA
		±15 V		7.0	7.5	mA

*Full power bandwidth = slew rate/(2p V_{PEAK}).

Specifications subject to change without notice.

AD818

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage ± 18 V

Internal Power Dissipation²

Plastic (N) See Derating Curves

Small Outline (R) See Derating Curves

Input Voltage (Common Mode) $\pm V_S$

Differential Input Voltage ± 6 V

Output Short-Circuit Duration See Derating Curves

Storage Temperature Range (N, R) -65°C to $+125^{\circ}\text{C}$

Operating Temperature Range -40°C to $+85^{\circ}\text{C}$

Lead Temperature Range (Soldering 10 sec) 300°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Specification is for device in free air: 8-lead plastic package, $\theta_{JA} = 90^{\circ}\text{C}/\text{W}$; 8-lead SOIC package, $\theta_{JA} = 155^{\circ}\text{C}/\text{W}$.

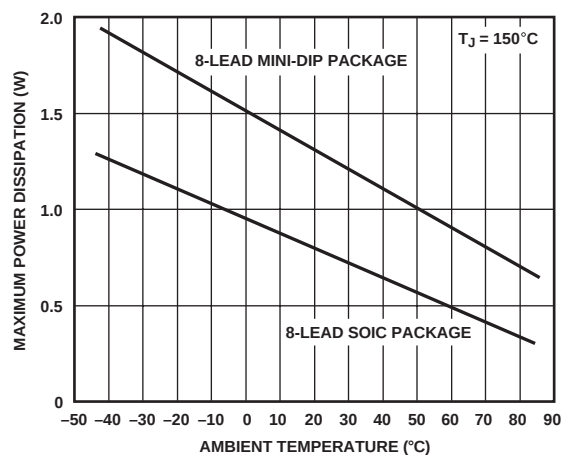


Figure 3. Maximum Power Dissipation vs. Temperature for Different Package Types

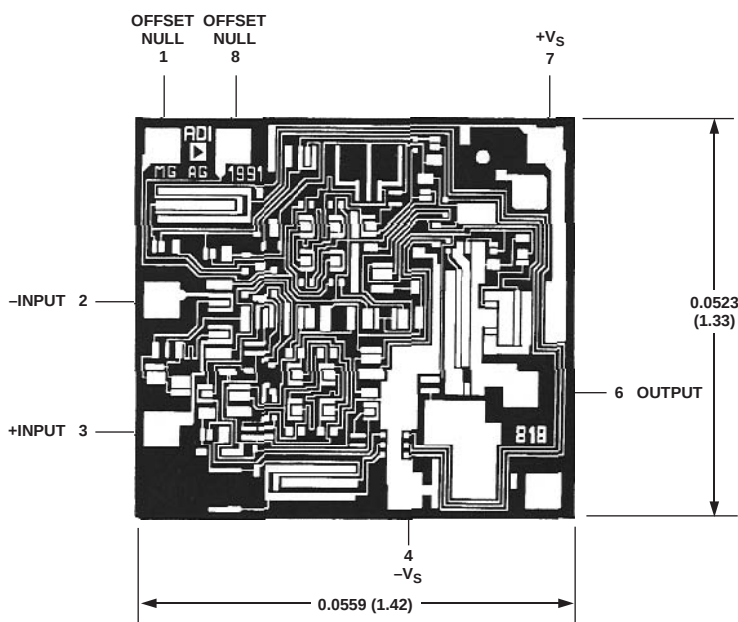
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD818 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

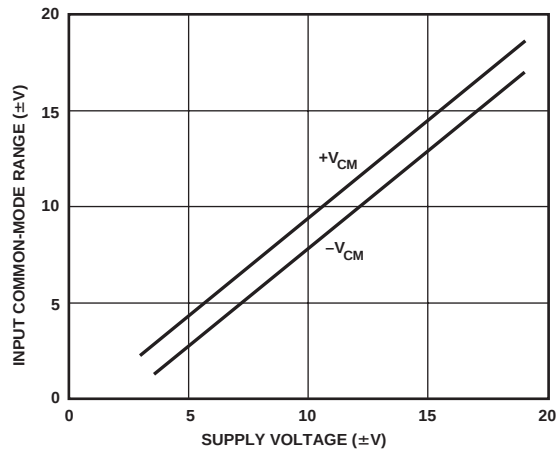


METALLIZATION PHOTOGRAPH

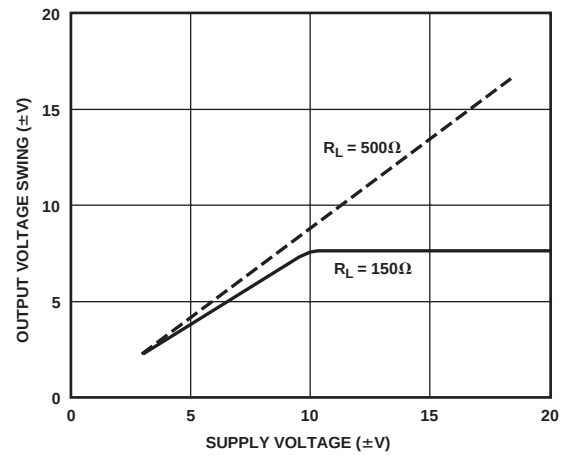
Dimensions shown in inches and (mm)



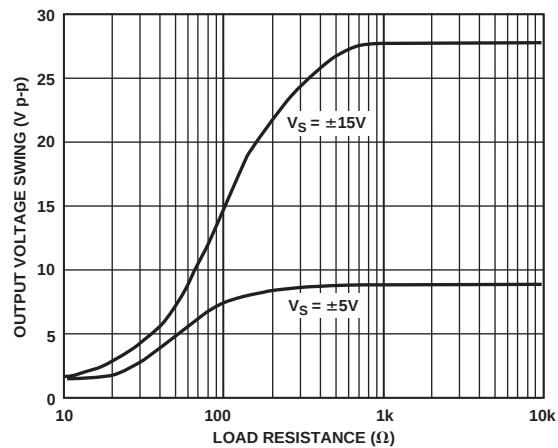
Typical Performance Characteristics—AD818



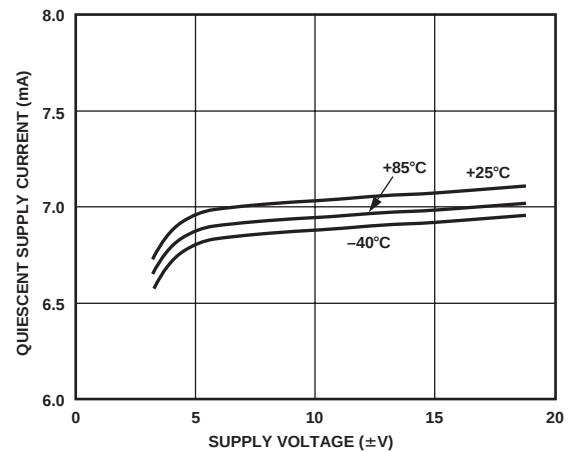
TPC 1. Common-Mode Voltage Range vs. Supply



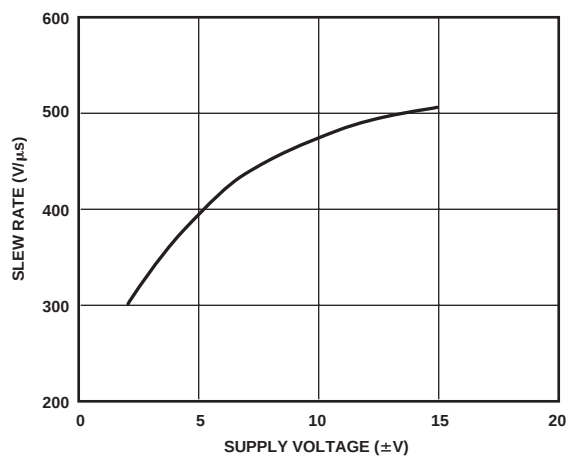
TPC 4. Output Voltage Swing vs. Supply



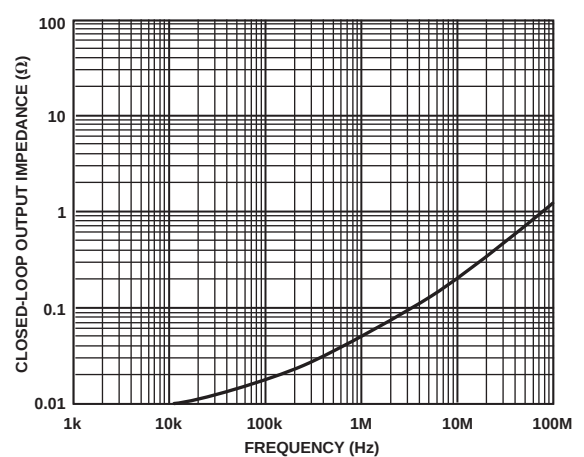
TPC 2. Output Voltage Swing vs. Load Resistance



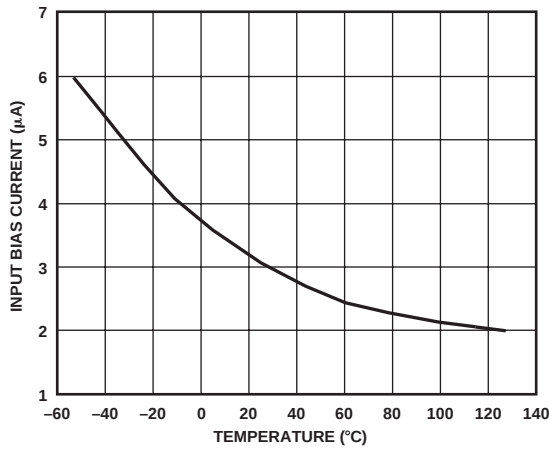
TPC 5. Quiescent Supply Current vs. Supply Voltage



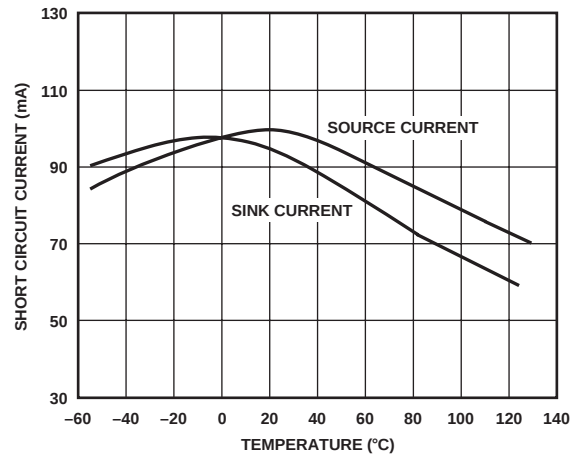
TPC 3. Slew Rate vs. Supply Voltage



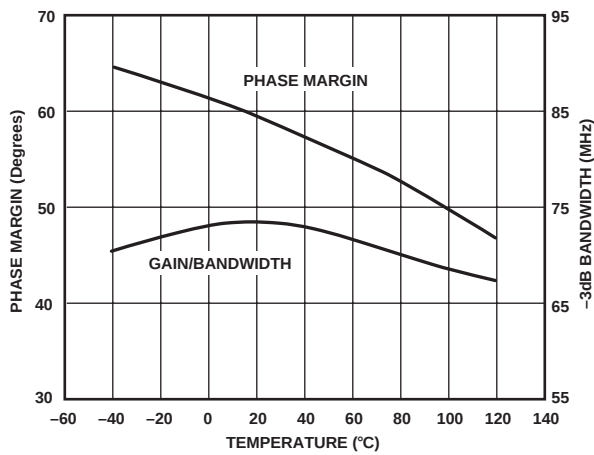
TPC 6. Closed-Loop Output Impedance vs. Frequency



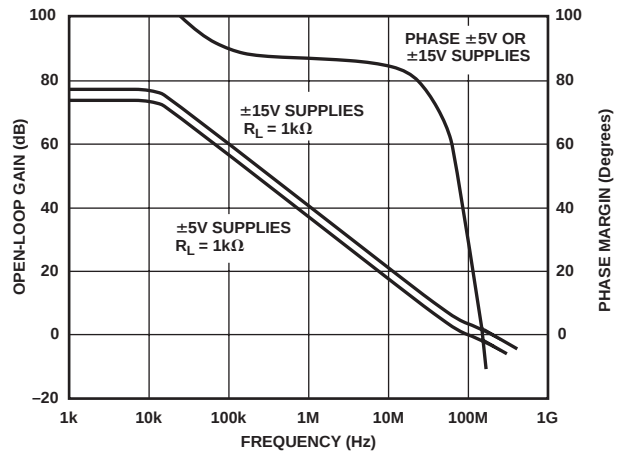
TPC 7. Input Bias Current vs. Temperature



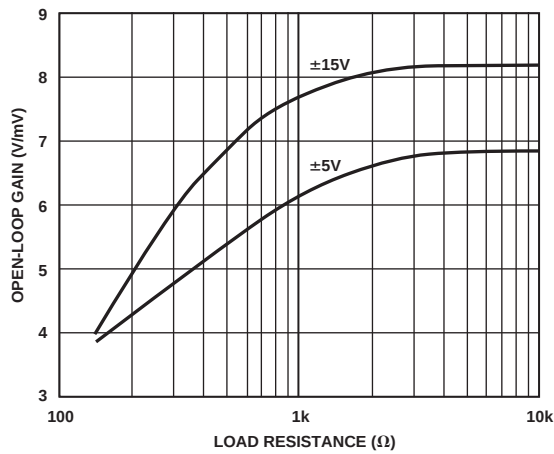
TPC 10. Short-Circuit Current vs. Temperature



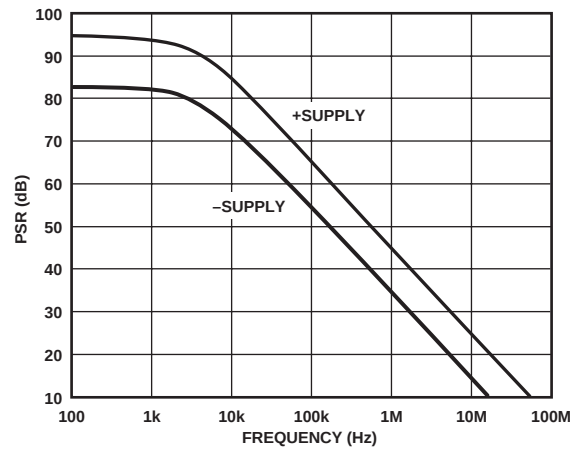
TPC 8. -3 dB Bandwidth and Phase Margin vs. Temperature, Gain = +2



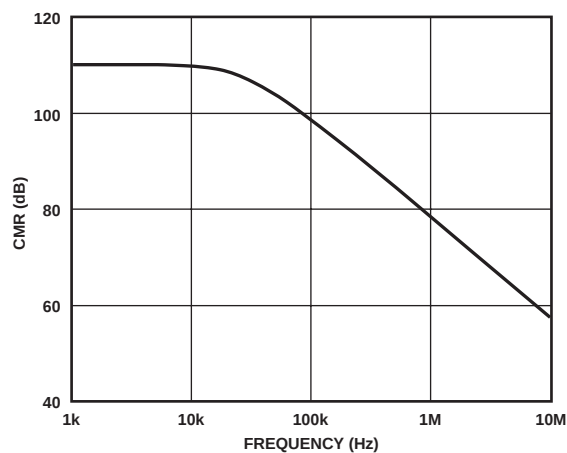
TPC 11. Open-Loop Gain and Phase Margin vs. Frequency



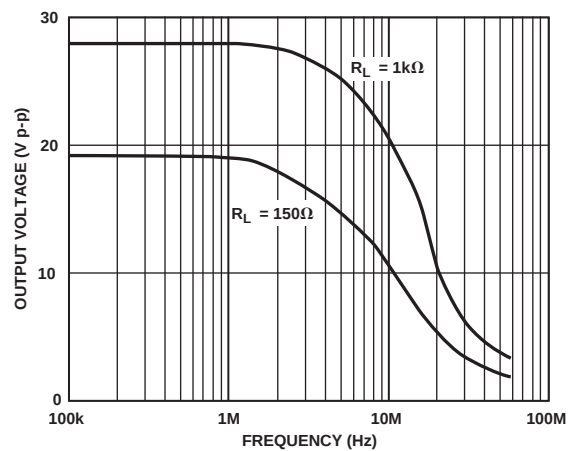
TPC 9. Open-Loop Gain vs. Load Resistance



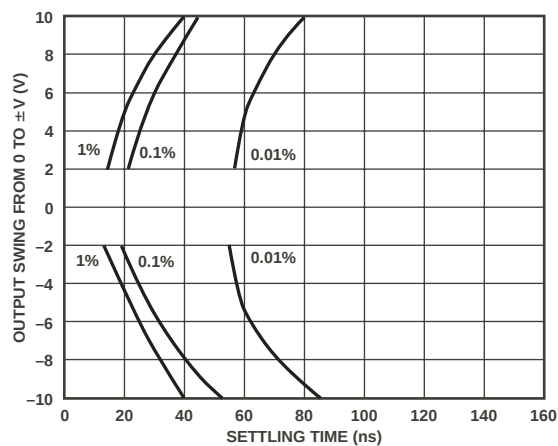
TPC 12. Power Supply Rejection vs. Frequency



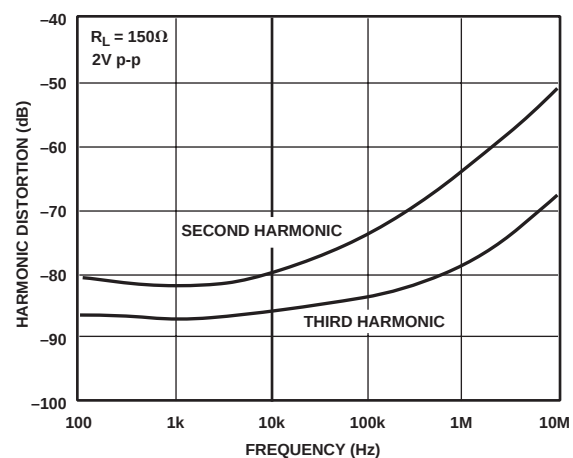
TPC 13. Common-Mode Rejection vs. Frequency



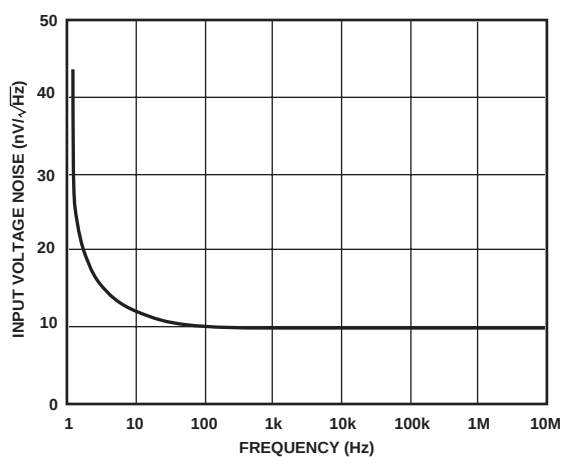
TPC 16. Output Voltage vs. Frequency



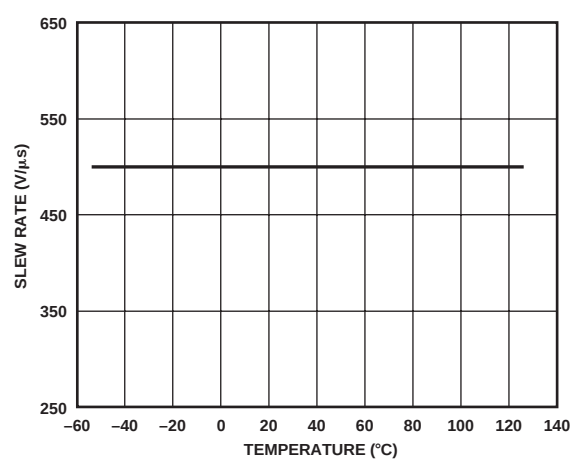
TPC 14. Output Swing and Error vs. Settling Time



TPC 17. Harmonic Distortion vs. Frequency

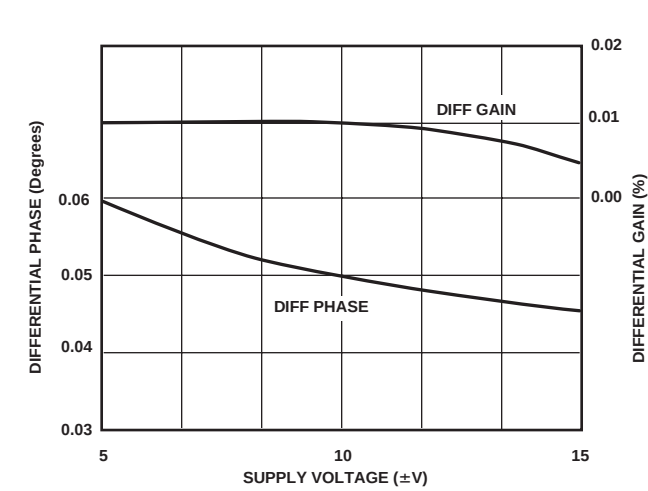


TPC 15. Input Voltage Noise Spectral Density vs. Frequency

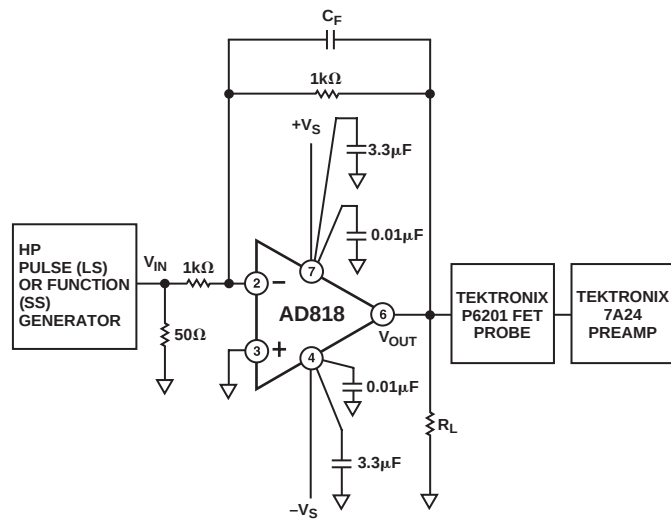


TPC 18. Slew Rate vs. Temperature

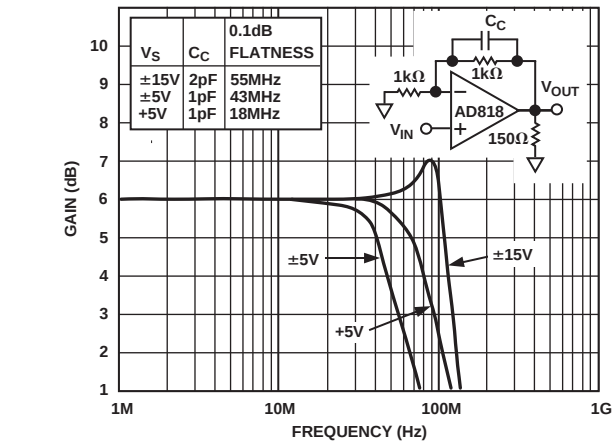
AD818



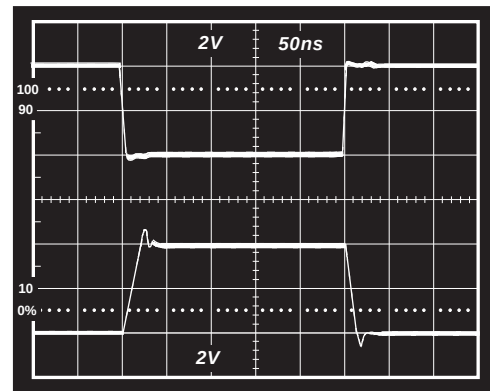
TPC 19. Differential Gain and Phase vs. Supply Voltage



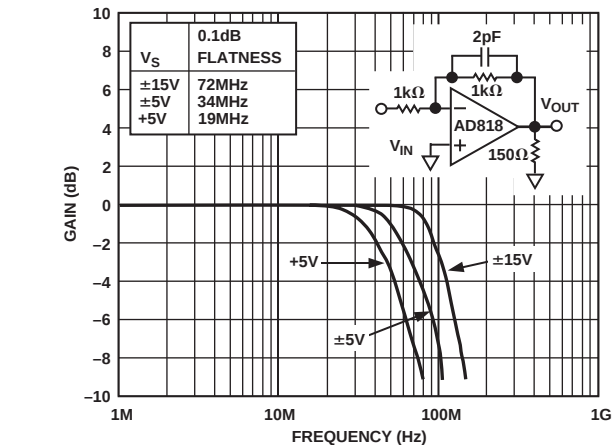
TPC 22. Inverting Amplifier Connection



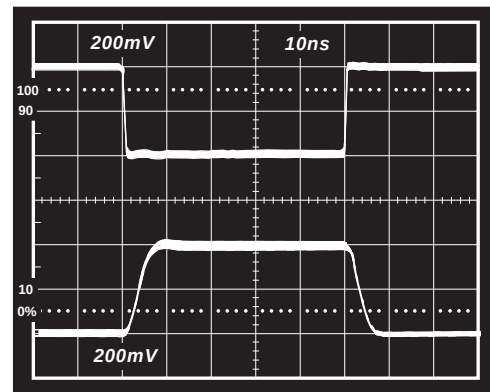
TPC 20. Closed-Loop Gain vs. Frequency ($G = +2$)



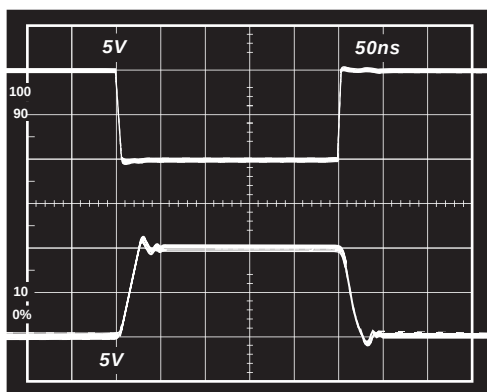
TPC 23. Inverter Large Signal Pulse Response; $V_S = \pm 5V$, $C_F = 1pF$, $R_L = 1k\Omega$



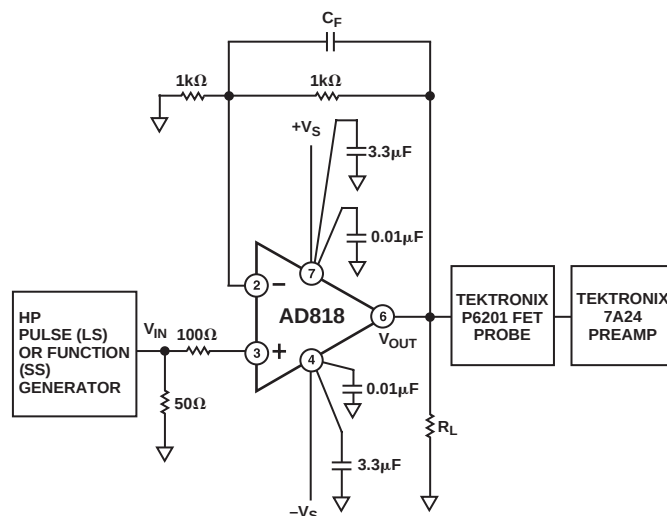
TPC 21. Closed-Loop Gain vs. Frequency ($G = -1$)



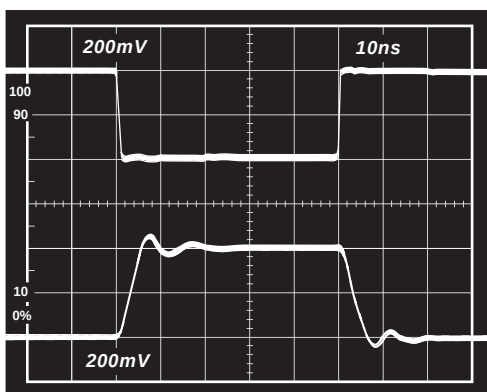
TPC 24. Inverter Small Signal Pulse Response; $V_S = \pm 5V$, $C_F = 1pF$, $R_L = 150\Omega$



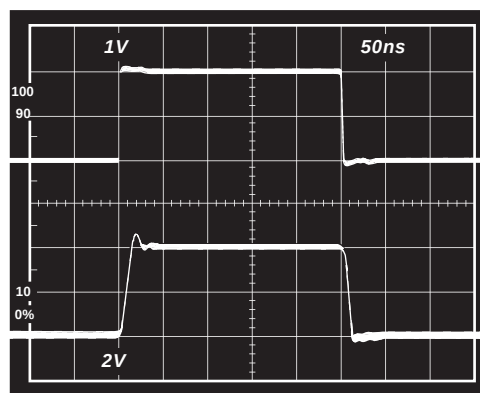
TPC 25. Inverter Large Signal Pulse Response; $V_S = \pm 15\text{ V}$, $C_F = 1\text{ pF}$, $R_L = 1\text{ kW}$



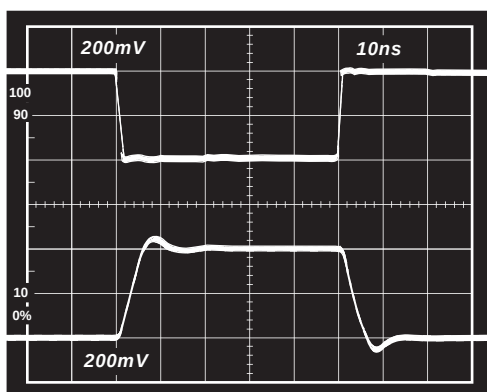
TPC 28. Noninverting Amplifier Connection



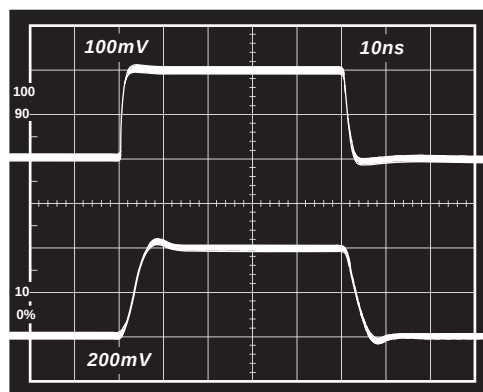
TPC 26. Inverter Small Signal Pulse Response; $V_S = \pm 15\text{ V}$, $C_F = 1\text{ pF}$, $R_L = 150\text{ W}$



TPC 29. Noninverting Large Signal Pulse Response; $V_S = \pm 5\text{ V}$, $C_F = 1\text{ pF}$, $R_L = 1\text{ kW}$

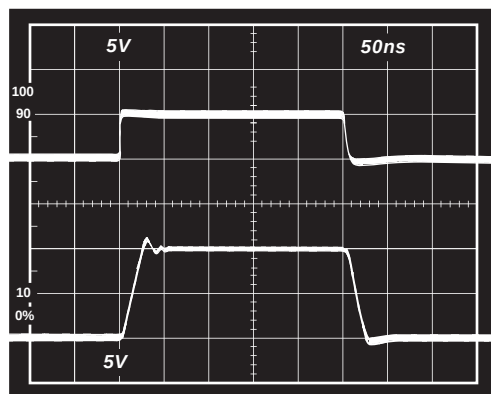


TPC 27. Inverter Small Signal Pulse Response; $V_S = \pm 5\text{ V}$, $C_F = 0\text{ pF}$, $R_L = 150\text{ W}$

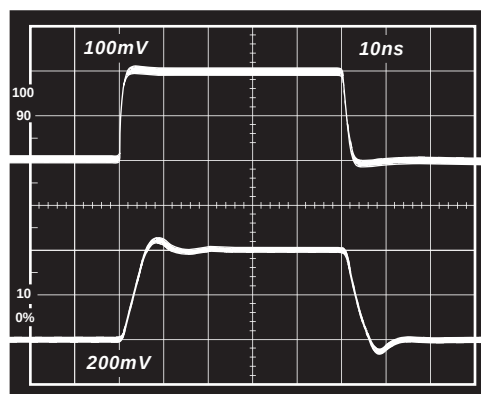


TPC 30. Noninverting Small Signal Pulse Response; $V_S = \pm 5\text{ V}$, $C_F = 1\text{ pF}$, $R_L = 150\text{ W}$

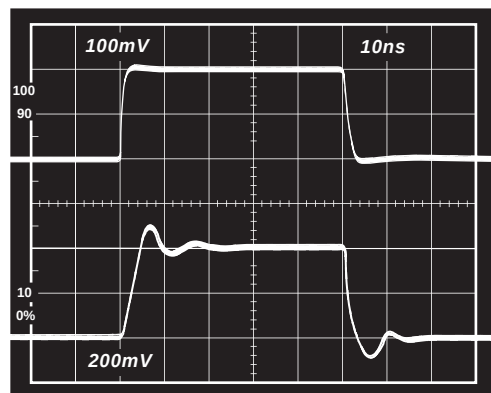
AD818



TPC 31. Noninverting Large Signal Pulse Response;
 $V_S = \pm 15\text{ V}$, $C_F = 1\text{ pF}$, $R_L = 1\text{ kW}$



TPC 33. Noninverting Small Signal Pulse Response;
 $V_S = \pm 5\text{ V}$, $C_F = 0\text{ pF}$, $R_L = 150\text{ W}$



TPC 32. Noninverting Small Signal Pulse Response;
 $V_S = \pm 15\text{ V}$, $C_F = 1\text{ pF}$, $R_L = 150\text{ W}$

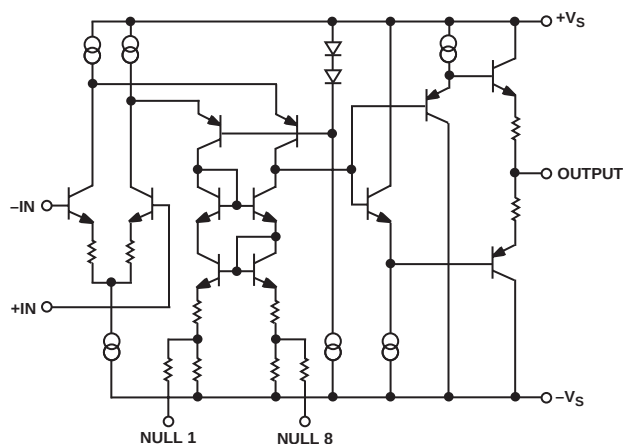


Figure 4. AD818 Simplified Schematic

THEORY OF OPERATION

The AD818 is a low cost video operational amplifier designed to excel in high performance, high output current video applications.

The AD818 (Figure 4) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier that delivers the necessary current to the load, while maintaining low levels of distortion.

The AD818 will drive terminated cables and capacitive loads of 10 pF or less. As the closed-loop gain is increased, the AD818 will drive heavier capacitive loads without oscillating.

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in TPC 28) is required in circuits where the input to the AD818 will be subjected to transients of continuous overload voltages exceeding the ± 6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a “balancing” resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

GROUNDING AND BYPASSING

When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnect leads. When wiring components, care should be taken to provide a low resistance, low inductance path to ground. Sockets should be avoided, since their increased interlead capacitance can degrade circuit bandwidth.

Feedback resistors should be of low enough value (≤ 1 k Ω) to ensure that the time constant formed with the inherent stray capacitance at the amplifier’s summing junction will not limit performance. This parasitic capacitance, along with the parallel resistance of $R_F \parallel R_{IN}$, forms a pole in the loop transmission, which

may result in peaking. A small capacitance (1 pF–5 pF) may be used in parallel with the feedback resistor to neutralize this effect.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 μ F are recommended.

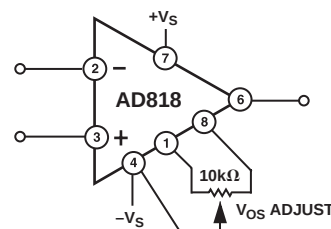


Figure 5. Offset Null Configuration

OFFSET NULLING

The input offset voltage of the AD818 is inherently very low. However, if additional nulling is required, the circuit shown in Figure 5 can be used. The null range of the AD818 in this configuration is ± 10 mV.

SINGLE SUPPLY OPERATION

Another exciting feature of the AD818 is its ability to perform well in a single supply configuration. The AD818 is ideally suited for applications that require low power dissipation and high output current.

Referring to Figure 6, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: $R_1 + R_3 \parallel R_2$ combine with C_1 to form a low frequency corner of approximately 10 kHz. C_4 was inserted in series with R_4 to maintain amplifier stability at high frequency.

Combining R_3 with C_2 forms a low-pass filter with a corner frequency of approximately 500 Hz. This is needed to maintain amplifier PSRR, since the supply is connected to V_{IN} through the input divider. The values for R_2 and C_2 were chosen to demonstrate the AD818’s exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C_3 was inserted in series with R_L .

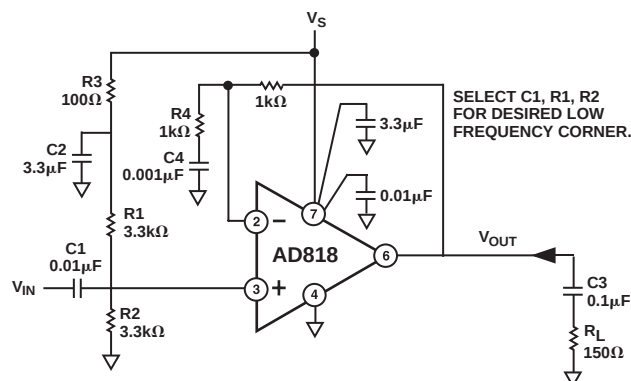
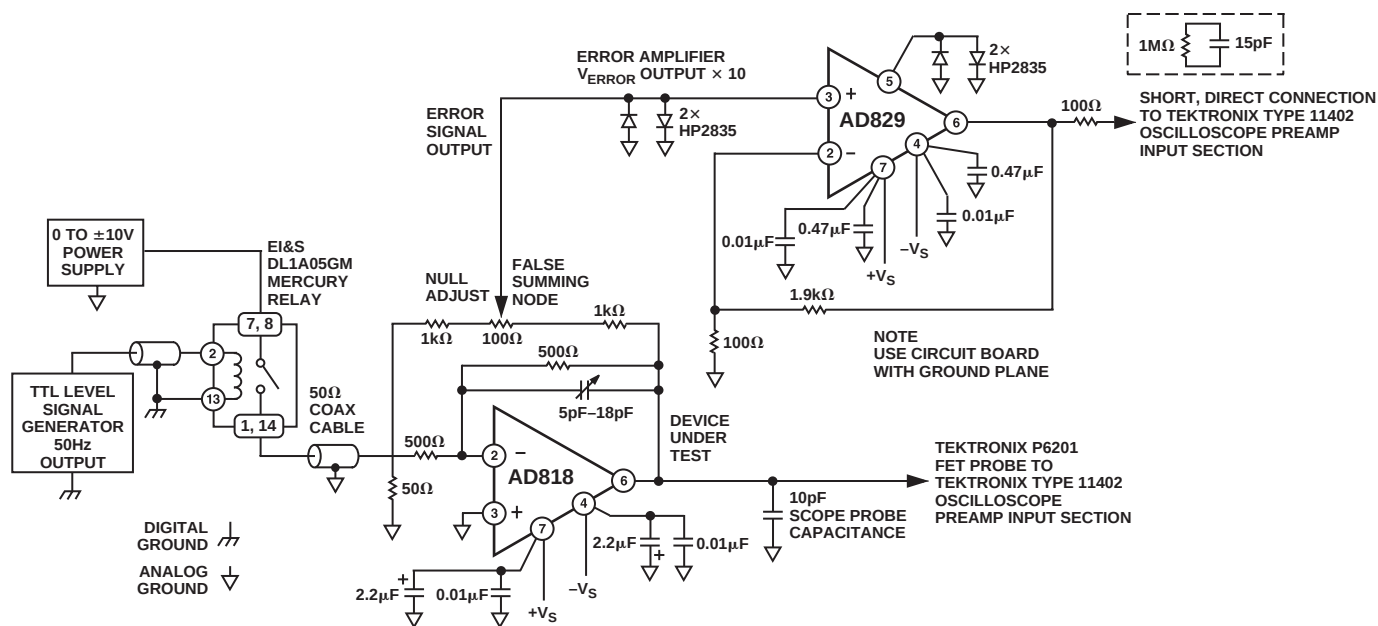


Figure 6. Single-Supply Amplifier Configuration



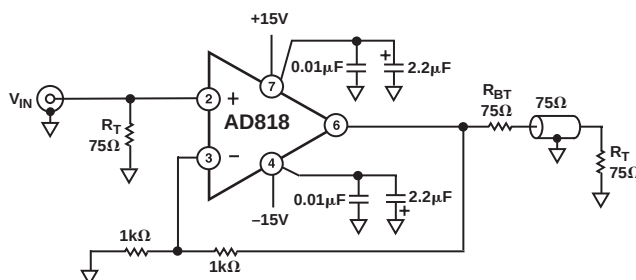
AD818 SETTLING TIME

Settling time primarily comprises two regions. The first is the slow time in which the amplifier is overdriven, where the output voltage rate of change is at its maximum. The second is the linear time period required for the amplifier to settle to within a specified percentage of the final value.

Measuring the rapid settling time of the AD818 (45 ns to 0.1% and 80 ns to 0.01%—10 V step) requires applying an input pulse with a very fast edge and an extremely flat top. With the AD818 configured in a gain of -1 , a clamped false summing junction responds when the output error is within the sum of two diode voltages (approximately 1 V). The signal is then amplified 20 times by a clamped amplifier whose output is connected directly to a sampling oscilloscope.

A High Performance Video Line Driver

The buffer circuit shown in Figure 8 will drive a back-terminated 75 W video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 55 MHz with only 0.05° and 0.01% differential phase and gain at the 3.58 MHz NTSC subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 7 mA quiescent current.



DIFFERENTIAL LINE RECEIVER

The differential receiver circuit of Figure 9 is useful for many applications—from audio to video. It allows extraction of a low level signal in the presence of common-mode noise, as shown in Figure 10.

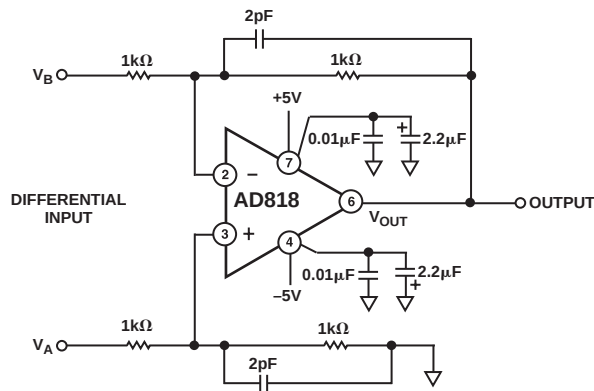


Figure 9. Differential Line Receiver

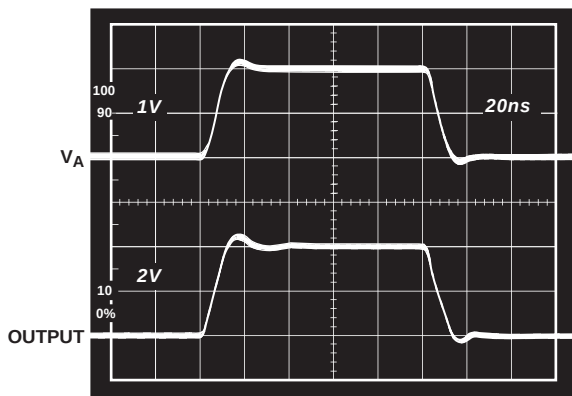
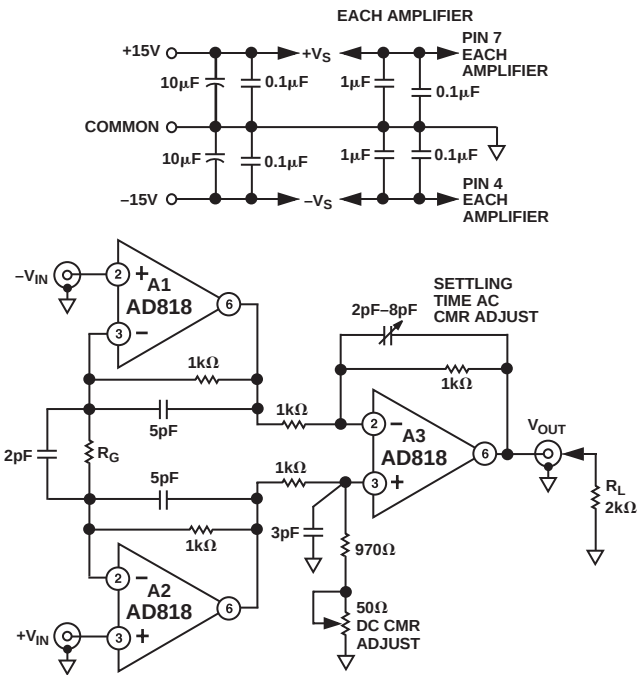


Figure 10. Performance of Line Receiver, $R_L = 150 \Omega$, $G = +2$

A HIGH SPEED, 3-OP AMP IN AMP

The circuit of Figure 11 uses three high speed op amps: two AD818s and an AD817. This high speed circuit lends itself well to CCD imaging and other video speed applications. It has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.



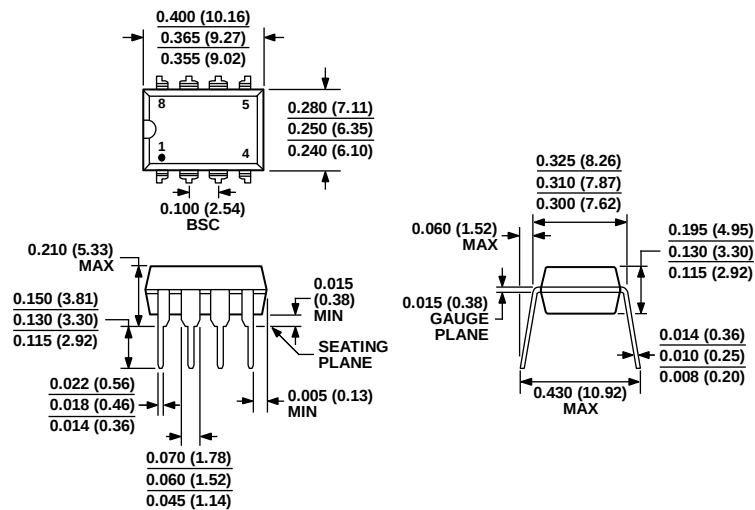
BANDWIDTH, SETTLING TIME, AND TOTAL HARMONIC DISTORTION VS. GAIN

GAIN	R_G	CADJ (pF)	SMALL SIGNAL BANDWIDTH	SETTLING TIME TO 0.1%	THD + NOISE BELOW INPUT LEVEL @ 10kHz
3	1k Ω	2–8	14.7MHz	200ns	82dB
10	222 Ω	2–8	4.5MHz	370ns	81dB
100	20 Ω	2–8	960kHz	2.5 μ s	71dB

Figure 11. High Speed 3-Op Amp In Amp

AD818

OUTLINE DIMENSIONS

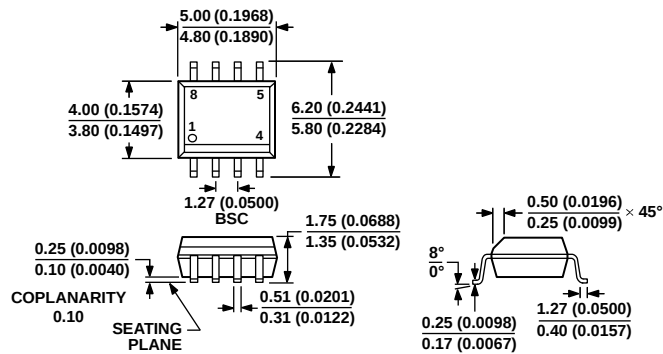


COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 12. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)

070606-A



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 13. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD818AN	–40°C to +85°C	8-Lead Plastic PDIP	N-8
AD818ANZ	–40°C to +85°C	8-Lead Plastic PDIP	N-8
AD818AR	–40°C to +85°C	8-Lead SOIC_N	R-8
AD818ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8
AD818AR-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD818ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD818AR-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD818ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD818AR-EBZ	–40°C to +85°C	Evaluation Board for 8-lead SOIC_N	

¹ Z = RoHS Compliant Part.

REVISION HISTORY**10/10—Rev. C to Rev. D**

Updated Outline Dimensions	14
Changes to Ordering Guide	15

5/03—Rev. B to Rev. C

Renumbered Figures and TPCs	Universal
Changes to Specifications	2
Changes to Ordering Guide	4
Changes to Figures 9 and 10	12
Updated Outline Dimensions	14

