

AD7677—SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise stated.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	–0.1		+3	V
Analog Input CMRR	$f_{IN} = 10$ kHz		85		dB
Input Current	1 MSPS Throughput		11		μA
Input Impedance		See Analog Input Section			
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1	μs
Throughput Rate	In Warp Mode	0.001		1	MSPS
Time Between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			1.25	μs
Throughput Rate	In Normal Mode	0		800	kSPS
Complete Cycle	In Impulse Mode			1.5	μs
Throughput Rate	In Impulse Mode	0		666	kSPS
DC ACCURACY					
Integral Linearity Error		–1		+1	LSB ^{1, 2}
Differential Linearity Error		–1		+1	LSB ²
No Missing Codes		16			Bits
Transition Noise			0.35		LSB
+Full-Scale Error ³	In Warp Mode	–25		+25	LSB
–Full Scale Error ³	In Warp Mode	–20		+20	LSB
Zero Error ³	In Warp Mode	–15		+15	LSB
+Full-Scale Error ³	In Impulse or Normal Mode	–40		+40	LSB
–Full Scale Error ³	In Impulse or Normal Mode	–20		+20	LSB
Zero Error ³	In Impulse or Normal Mode	–23		+23	LSB
Power Supply Sensitivity	AVDD = 5 V ± 5%		±1.4		LSB
AC ACCURACY					
Signal-to-Noise	$f_{IN} = 20$ kHz	92	94		dB ^{2, 4}
	$f_{IN} = 45$ kHz		94		dB
Spurious Free Dynamic Range	$f_{IN} = 20$ kHz	104.5	110		dB ²
	$f_{IN} = 45$ kHz		110		dB
Total Harmonic Distortion	$f_{IN} = 20$ kHz		–110	–103.5	dB ²
	$f_{IN} = 45$ kHz		–110		dB
Signal-to-(Noise+Distortion)	$f_{IN} = 20$ kHz	92	94		dB ²
	$f_{IN} = 45$ kHz		94		dB
	$f_{IN} = 45$ kHz, –60 dB Input		34		dB
–3 dB Input Bandwidth			15.8		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD – 1.85	V
External Reference Current Drain	1 MSPS Throughput		37		μA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		–1		+1	μA
I_{IH}		–1		+1	μA
DIGITAL OUTPUTS					
Data Format		Parallel or Serial 16-Bit Conversion			
Pipeline Delay		Results Available Immediately after Completed Conversion			
V_{OL}	$I_{SINK} = 1.6$ mA			0.4	V
V_{OH}	$I_{SOURCE} = -100$ μA			OVDD – 0.6	V

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25 ⁵	V
Operating Current ²	1 MSPS Throughput				
AVDD			16.7		mA
DVDD ⁶			6.4		mA
OVDD ⁶			69		μA
Power Dissipation ⁶	666 kSPS Throughput ⁷		87	98	mW
	100 SPS Throughput ⁷		15		μW
	1 MSPS Throughput ²		115	130	mW
In Power-Down Mode ⁸				7	μW
TEMPERATURE RANGE⁹					
Specified Performance	T _{MIN} to T _{MAX}	−40		+85	°C

NOTES

¹LSB means Least Significant Bit. With the ±2.5 V input range, one LSB is 76.3 μV.

²In Warp Mode.

³Tested with V_{REF} = 2.5 V. See Definition of Specifications section. These specifications do not include the error contribution from the external reference.

⁴All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full scale unless otherwise specified.

⁵The max should be the minimum of 5.25 V and DVDD + 0.3 V.

⁶Tested in Parallel Reading Mode.

⁷In Impulse Mode.

⁸With OVDD below DVDD + 0.3 V and all digital inputs forced to DVDD or DGND, respectively.

⁹Contact factory for extended temperature range.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise stated.)

	Symbol	Min	Typ	Max	Unit
Refer to Figures 11 and 12					
Convert Pulsewidth	t ₁	5			ns
Time Between Conversions (Warp Mode/Normal Mode/Impulse Mode)	t ₂	1/1.25/1.5		Note 1	μs
CNVST LOW to BUSY HIGH Delay	t ₃			30	ns
BUSY HIGH All Modes Except in Master Serial Read after Convert Mode (Warp Mode/Normal Mode/Impulse Mode)	t ₄			0.75/1/1.25	μs
Aperture Delay	t ₅		2		ns
End of Conversion to BUSY LOW Delay	t ₆	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t ₇			0.75/1/1.25	μs
Acquisition Time	t ₈	250			ns
RESET Pulsewidth	t ₉	10			ns
Refer to Figures 13, 14, and 15 (Parallel Interface Modes)					
CNVST LOW to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₁₀			0.75/1/1.25	μs
DATA Valid to BUSY LOW Delay	t ₁₁	45			ns
Bus Access Request to DATA Valid	t ₁₂			40	ns
Bus Relinquish Time	t ₁₃	5		15	ns
Refer to Figures 17 and 18 (Master Serial Interface Modes) ²					
CS LOW to SYNC Valid Delay	t ₁₄			10	ns
CS LOW to Internal SCLK Valid Delay	t ₁₅			10	ns
CS LOW to SDOUT Delay	t ₁₆			10	ns
CNVST LOW to SYNC Delay (Read During Convert) (Warp Mode/Normal Mode/Impulse Mode)	t ₁₇		25/275/525		ns
SYNC Asserted to SCLK First Edge Delay ³	t ₁₈	3			ns
Internal SCLK Period ³	t ₁₉	25		40	ns
Internal SCLK HIGH ³	t ₂₀	12			ns
Internal SCLK LOW ³	t ₂₁	7			ns
SDOUT Valid Setup Time ³	t ₂₂	4			ns
SDOUT Valid Hold Time ³	t ₂₃	2			ns
SCLK Last Edge to SYNC Delay ³	t ₂₄	3			ns
CS HIGH to SYNC HI-Z	t ₂₅			10	ns
CS HIGH to Internal SCLK HI-Z	t ₂₆			10	ns
CS HIGH to SDOUT HI-Z	t ₂₇			10	ns
BUSY HIGH in Master Serial Read After Convert ³	t ₂₈		See Table I		
CNVST LOW to SYNC Asserted Delay (Warp Mode/Normal Mode/Impulse Mode)	t ₂₉		0.75/1/1.25		μs
SYNC Deasserted to BUSY LOW Delay	t ₃₀		25		ns
Refer to Figures 19 and 20 (Slave Serial Interface Modes)					
External SCLK Setup Time	t ₃₁	5			ns
External SCLK Active Edge to SDOUT Delay	t ₃₂	3		18	ns
SDIN Setup Time	t ₃₃	5			ns
SDIN Hold Time	t ₃₄	5			ns
External SCLK Period	t ₃₅	25			ns
External SCLK HIGH	t ₃₆	10			ns
External SCLK LOW	t ₃₇	10			ns

NOTES

¹In Warp Mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.

²In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

³In serial master read during convert mode. See Table I for serial master read after convert mode.

Specifications subject to change without notice.

Table I. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]		0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
Busy High Width Maximum (Warp)	t_{24}	1.5	2	3	5.25	μ s
Busy High Width Maximum (Normal)	t_{24}	1.75	2.25	3.25	5.55	μ s
Busy High Width Maximum (Impulse)	t_{24}	2	2.5	3.5	5.75	μ s

ABSOLUTE MAXIMUM RATINGS¹

Analog Inputs

IN⁺², IN⁻², REF, REFGND AVDD + 0.3 V to AGND – 0.3 V

Ground Voltage Differences

AGND, DGND, OGND ± 0.3 V

Supply Voltages

AVDD, DVDD, OVDD –0.3 V to +7 V

AVDD to DVDD, AVDD to OVDD ± 7 V

DVDD to OVDD –0.3 V to +7 V

Digital Inputs –0.3 V to DVDD + 0.3 V

Internal Power Dissipation³ 700 mW

Internal Power Dissipation⁴ 2.5 W

Junction Temperature 150°C

Storage Temperature Range –65°C to +150°C

Lead Temperature Range

(Soldering 10 sec) 300°C

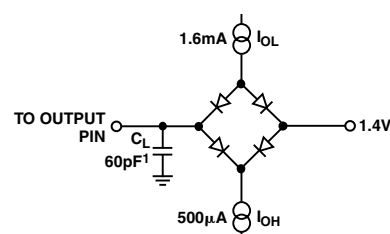
NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²See Analog Input section.

³Specification is for device in free air: 48-Lead LQFP: $\theta_{JA} = 91^\circ\text{C/W}$, $\theta_{JC} = 30^\circ\text{C/W}$.

⁴Specification is for device in free air: LFCSP: $\theta_{JA} = 26^\circ\text{C/W}$



NOTE

¹IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

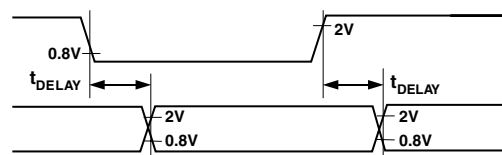
Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, $C_L = 10$ pF

Figure 2. Voltage Reference Levels for Timings

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7677AST	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7677ASTRL	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7677ACP	–40°C to +85°C	Chip Scale (LFCSP)	CP-48
AD7677ACPRL	–40°C to +85°C	Chip Scale (LFCSP)	CP-48
EVAL-AD7677CB ¹		Evaluation Board	
EVAL-CONTROL BRD ²		Controller Board	

NOTES

¹This board can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.

²This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7677 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1	AGND	P	Analog Power Ground Pin
2	AVDD	P	Analog Power Pin. Nominally 5 V.
3, 40–42, 44–48	NC		No Connect
4	BYTESWAP	DI	Parallel Mode Selection (8-bit/16-bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/ $\overline{2C}$	DI	Straight Binary/Binary Two's Complement. When OB/ $\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
6	WARP	DI	Mode Selection. When HIGH and IMPULSE LOW, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Mode Selection. When HIGH and WARP LOW, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/ \overline{PAR}	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	DATA[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, these outputs are in high impedance.
11, 12	DATA[2:3] or DIVSCLK[0:1]	DI/O	When SER/ \overline{PAR} is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, EXT/ \overline{INT} is LOW and RDC/SDIN is LOW, which is the serial master read after convert mode. These inputs, part of the serial port, are used to slow down if desired the internal serial clock which clocks the data output. In the other serial modes, these pins are high impedance outputs.
13	DATA[4] or EXT/ \overline{INT}	DI/O	When SER/ \overline{PAR} is LOW, this output is used as the Bit 4 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/ \overline{INT} tied LOW, the internal clock is selected on SCLK output. With EXT/ \overline{INT} set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	DATA[5] or INVSCLK	DI/O	When SER/ \overline{PAR} is LOW, this output is used as the Bit 5 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	DATA[6] or INVSCLK	DI/O	When SER/ \overline{PAR} is LOW, this output is used as the Bit 6 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	DATA[7] or RDC/SDIN	DI/O	When SER/ \overline{PAR} is LOW, this output is used as the Bit 7 of the Parallel Port Data Output Bus. When SER/ \overline{PAR} is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/ \overline{INT} . When EXT/ \overline{INT} is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/ \overline{INT} is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data is output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).

PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Type	Description
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground
21	DATA[8] or SDOUT	DO	When $\overline{\text{SER}/\overline{\text{PAR}}}$ is LOW, this output is used as the Bit 8 of the Parallel Port Data Output Bus. When $\overline{\text{SER}/\overline{\text{PAR}}}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7677 provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of $\text{OB}/\overline{2\text{C}}$. In serial mode, when $\text{EXT}/\overline{\text{INT}}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when $\text{EXT}/\overline{\text{INT}}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	DATA[9] or SCLK	DI/O	When $\overline{\text{SER}/\overline{\text{PAR}}}$ is LOW, this output is used as the Bit 9 of the Parallel Port Data Output Bus. When $\overline{\text{SER}/\overline{\text{PAR}}}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the $\text{EXT}/\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	DATA[10] or SYNC	DO	When $\overline{\text{SER}/\overline{\text{PAR}}}$ is LOW, this output is used as the Bit 10 of the Parallel Port Data Output Bus. When $\overline{\text{SER}/\overline{\text{PAR}}}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock ($\text{EXT}/\overline{\text{INT}} = \text{Logic LOW}$). When a read sequence is initiated and INVSCLK is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSCLK is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	DATA[11] or RDERROR	DO	When $\overline{\text{SER}/\overline{\text{PAR}}}$ is LOW, this output is used as the Bit 11 of the Parallel Port Data Output Bus. When $\overline{\text{SER}/\overline{\text{PAR}}}$ is HIGH and $\text{EXT}/\overline{\text{INT}}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	DATA[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. These pins are always outputs regardless of the state of $\overline{\text{SER}/\overline{\text{PAR}}}$.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must be tied to digital ground.
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{\text{CS}}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7677. Current conversion if any is aborted.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion. In impulse mode (IMPULSE HIGH and WARP LOW), if $\overline{\text{CNVST}}$ is held low when the acquisition phase (t_s) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must be Tied to Analog Ground.
37	REF	AI	Reference Input Voltage
38	REFGND	AI	Reference Input Analog Ground
39	IN–	AI	Differential Negative Analog Input
43	IN+	AI	Differential Positive Analog Input

NOTES

AI = Analog Input

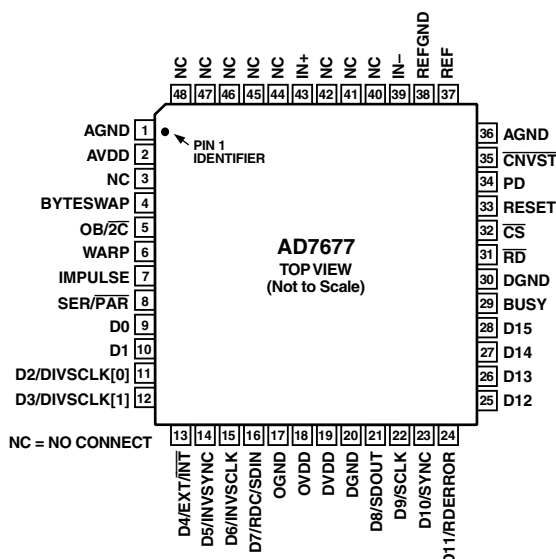
DI = Digital Input

DI/O = Bidirectional Digital

DO = Digital Output

P = Power

PIN CONFIGURATION
48-Lead LQFP
(ST-48)



DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a best-fit line drawn from “negative full scale” through “positive full scale.” The point used as “negative full scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a level 1 1/2 LSB beyond the last code transition.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

+FULL-SCALE ERROR

The last transition (from 011...10 to 011...11 in two’s complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal +full scale (2.499886 V for the ± 2.5 V range). The +full-scale error is the deviation of the actual level of the last transition from the ideal level.

–FULL-SCALE ERROR

The first transition (from 100...00 to 100...01 in two’s complement coding) should occur for an analog voltage 1/2 LSB above the nominal –full scale (–2.499962 V for the ± 2.5 V range). The –full-scale error is the deviation of the actual level of the first transition from the ideal level.

ZERO ERROR

The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to $S/(N+D)$ by the following formula:

$$ENOB = \left(S / [N + D] \right)_{dB} - 1.76 / 6.02$$

and is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

SIGNAL-TO-(NOISE + DISTORTION) RATIO (S/[N+D])

$S/(N+D)$ is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for $S/(N+D)$ is expressed in decibels.

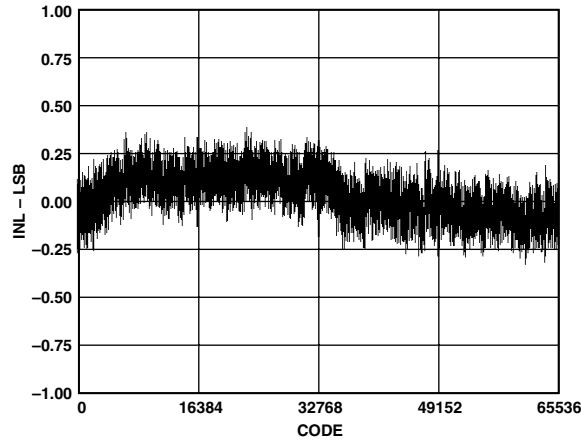
APERTURE DELAY

Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the \overline{CNVST} input to when the input signal is held for a conversion.

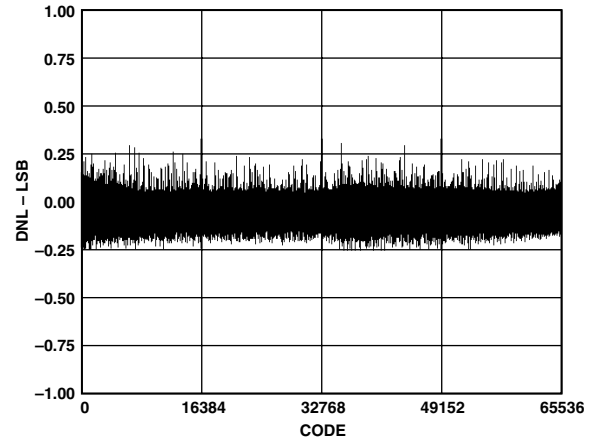
TRANSIENT RESPONSE

The time required for the AD7677 to achieve its rated accuracy after a full-scale step function is applied to its input.

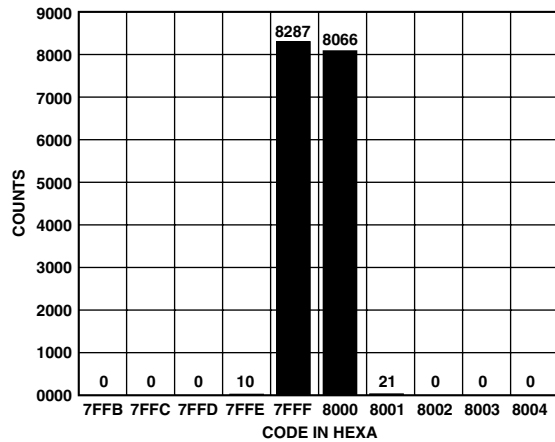
Typical Performance Characteristics—AD7677



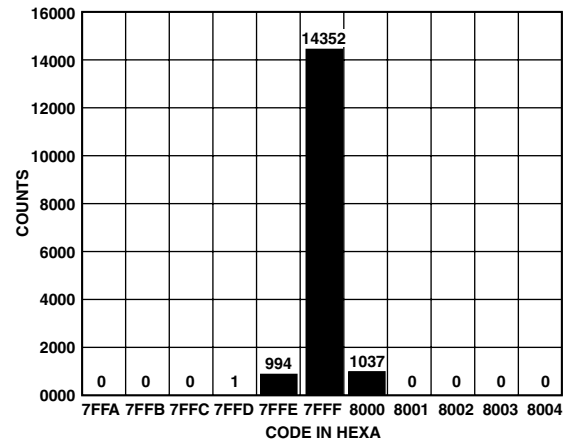
TPC 1. Integral Nonlinearity vs. Code



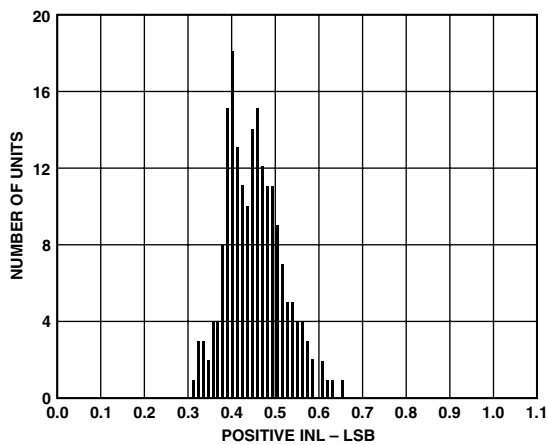
TPC 4. Differential Nonlinearity vs. Code



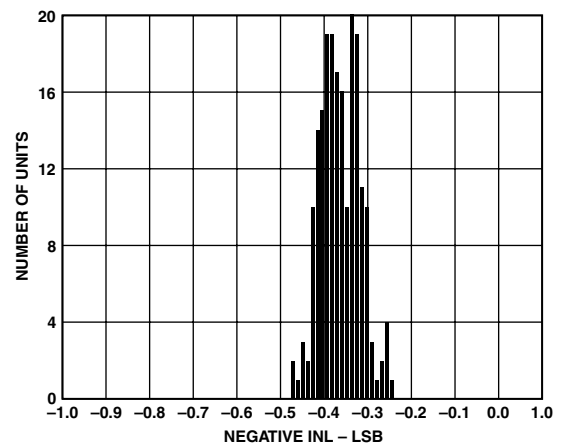
TPC 2. Histogram of 16,384 Conversions of a DC Input at the Code Transition



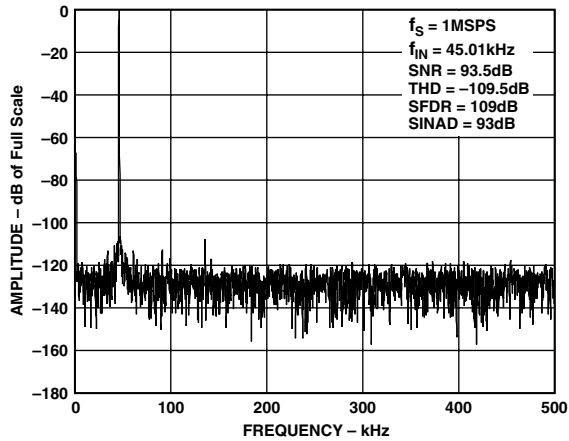
TPC 5. Histogram of 16,384 Conversions of a DC Input at the Code Center



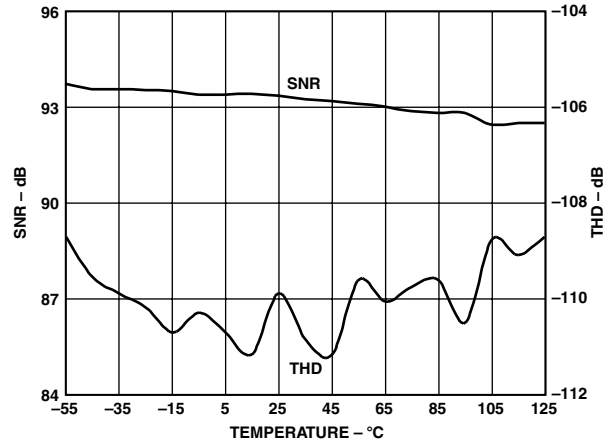
TPC 3. Typical Positive INL Distribution (199 Units)



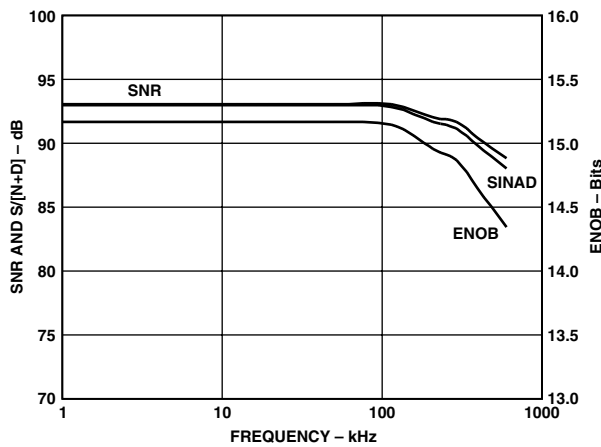
TPC 6. Typical Negative INL Distribution (199 Units)



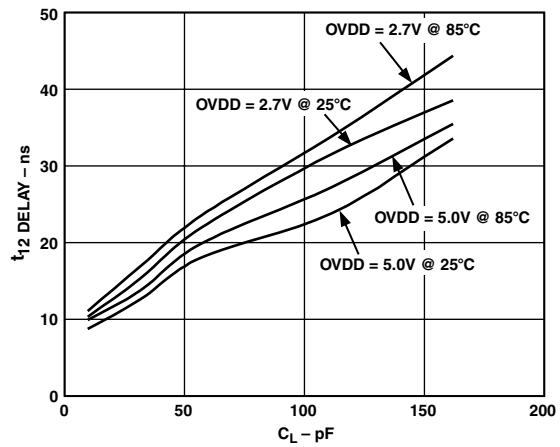
TPC 7. FFT Plot



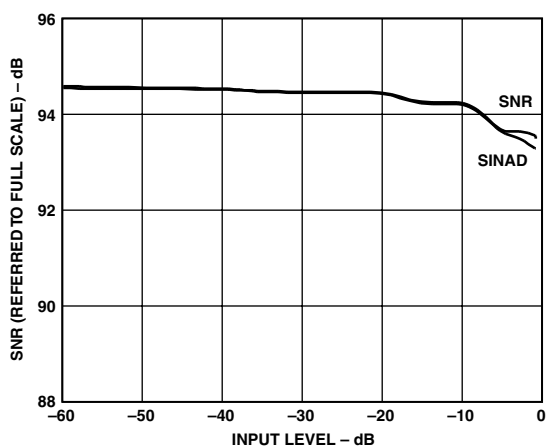
TPC 10. SNR, THD vs. Temperature



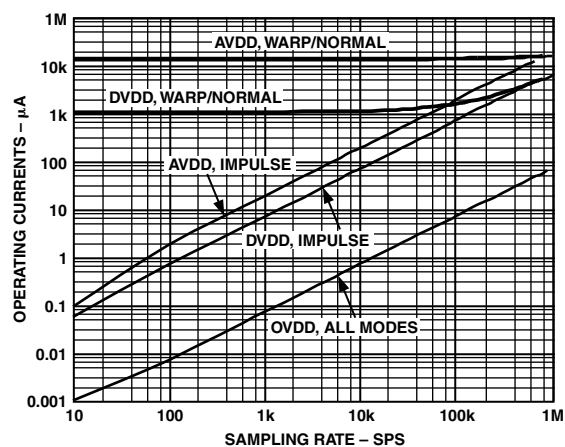
TPC 8. SNR, $S/(N+D)$, and ENOB vs. Frequency



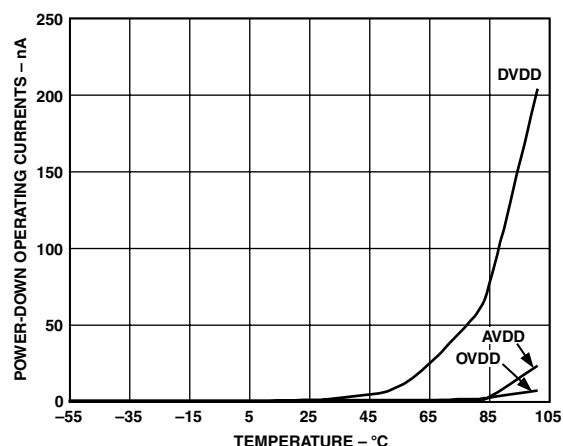
TPC 11. Typical Delay vs. Load Capacitance C_L



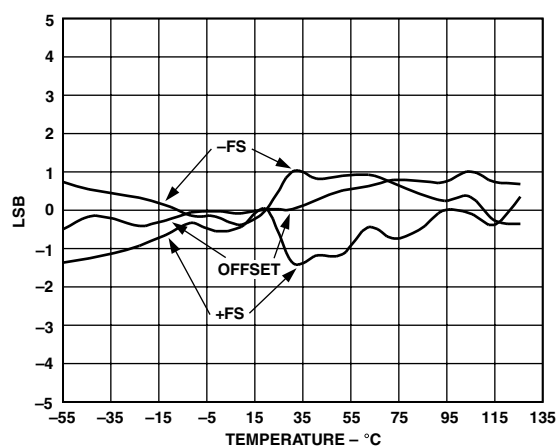
TPC 9. SNR and $S/(N+D)$ vs. Input Level



TPC 12. Operating Currents vs. Sample Rate



TPC 13. Power-Down Operating Currents vs. Temperature



TPC 14. Drift vs. Temperature

CIRCUIT INFORMATION

The AD7677 is a very fast, low power, single-supply, precise, 16-bit analog-to-digital converter (ADC). The AD7677 features different modes to optimize performances according to the applications.

In Warp Mode, the AD7677 is capable of converting 1,000,000 samples per second (1 MSPS).

The AD7677 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7677 can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP package that combines space savings and flexible configurations as either serial or parallel interface. The AD7677 is a pin-to-pin compatible upgrade of the AD7664, AD7675, and AD7676.

CONVERTER OPERATION

The AD7677 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW_+ and SW_- . All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN_+ and IN_- inputs. When the acquisition phase is complete and the $CNVST$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW_+ and SW_- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the $REFGND$ input. Therefore, the differential voltage between the inputs IN_+ and IN_- captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between $REFGND$ or REF , the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 \dots V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings $BUSY$ output low.

Modes of Operation

The AD7677 features three modes of operations, Warp, Normal, and Impulse. Each of these modes is more suitable for specific applications.

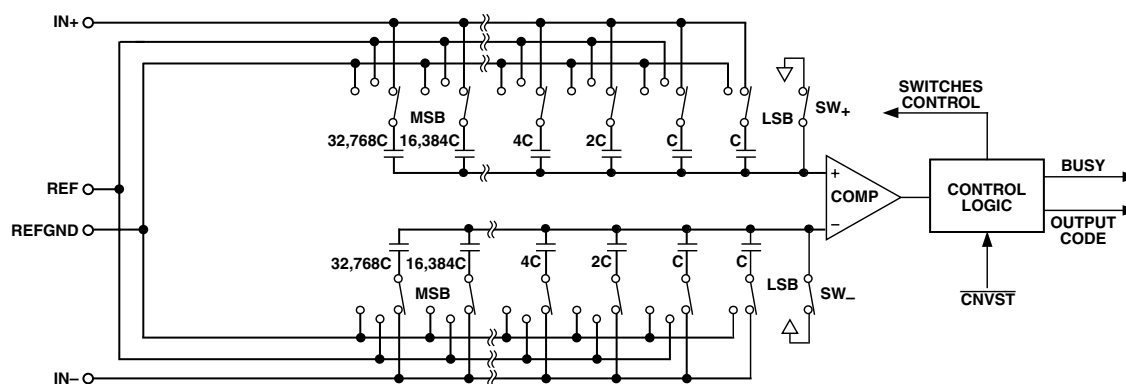


Figure 3. ADC Simplified Schematic

AD7677

The Warp Mode allows the fastest conversion rate up to 1 MSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7677 ideal for applications where fast sample rates are required.

The Normal Mode is the fastest mode (800 kSPS) without any limitation about the time between conversions. This mode makes the AD7677 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

The Impulse Mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 666 kSPS. When operating at 100 SPS, for example, it typically consumes only 15 μ W. This feature makes the AD7677 ideal for battery-powered applications.

Transfer Functions

Using the OB/2C digital input, the AD7677 offers two output codings: straight binary and two's complement. The ideal transfer characteristic for the AD7677 is shown in Figure 4.

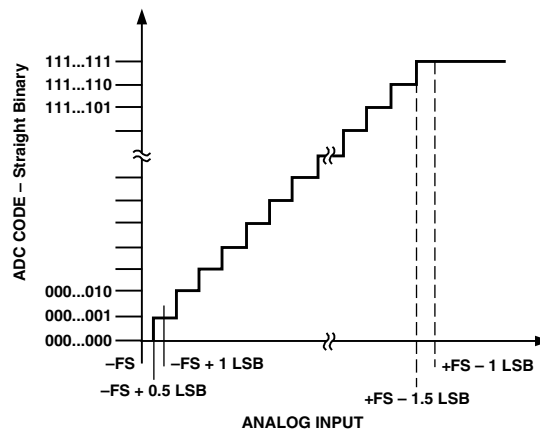


Figure 4. ADC Ideal Transfer Function

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7677. Different circuitry shown on this diagram is optional and is discussed below.

Analog Inputs

Figure 6 shows a simplified analog input section of AD7677.

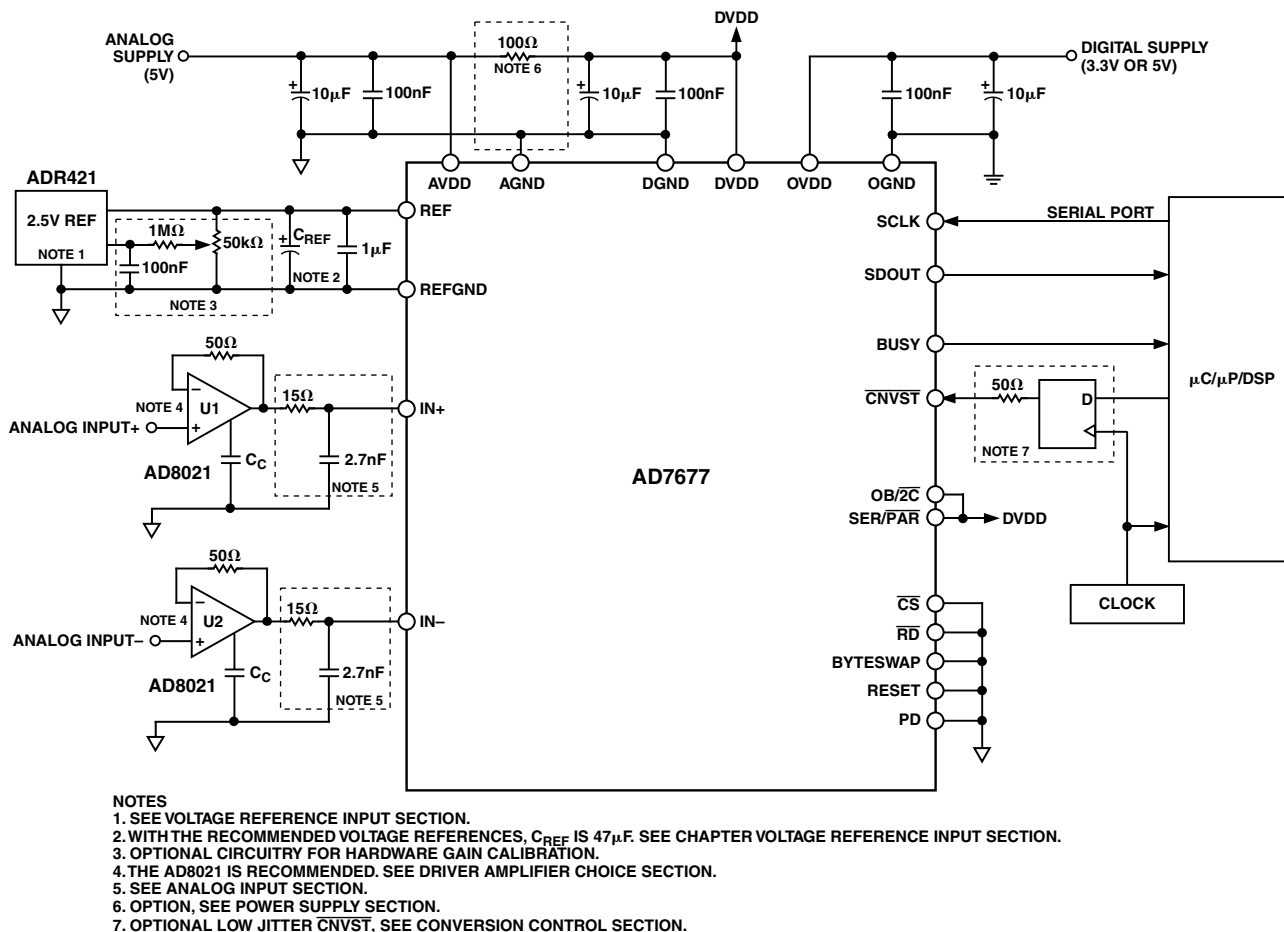


Figure 5. Typical Connection Diagram

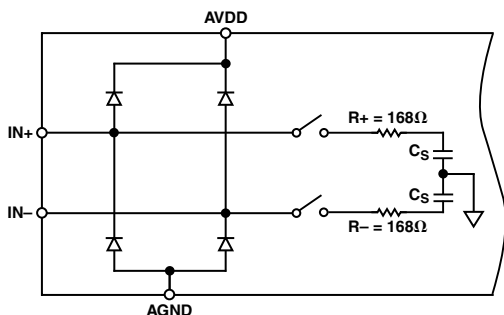


Figure 6. Simplified Analog Input

The diodes shown in Figure 6 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. This condition could eventually occur when the input buffer's (U1) or (U2) supplies are different from AVDD. In such case, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure is a true differential structure. By using these differential inputs, signals common to both inputs are rejected as shown in Figure 7, which represents the typical CMRR over frequency.

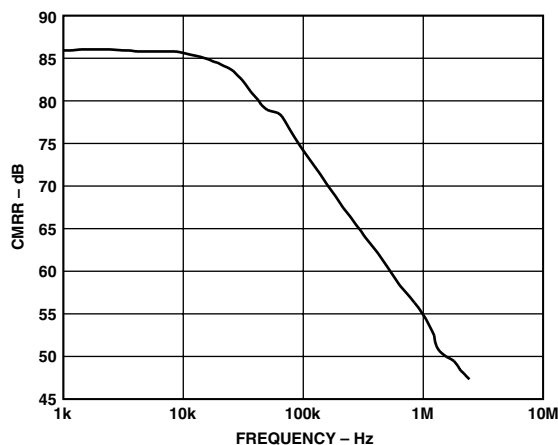


Figure 7. Analog Input CMRR vs. Frequency

During the acquisition phase, for ac signals, the AD7677 behaves like a one-pole RC filter consisting of the equivalent resistance R_+ , R_- , and C_S . The resistors R_+ and R_- are typically 168 Ω and are lumped components made up of some serial resistors and the on resistance of the switches. The capacitor C_S is typically 60 pF and is mainly the ADC sampling capacitor. This one-pole filter with a typical -3 dB cutoff frequency of 15.8 MHz reduces undesirable aliasing effect and limits the noise coming from the inputs.

Because the input impedance of the AD7677 is very high, the AD7677 can be driven directly by a low impedance source without gain error. That allows the user to input, as shown in Figure 5, an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the AD7677 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion. The maximum source impedance depends

on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades proportionally to the source impedance.

Single to Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver will allow for a differential input into the part. The schematic is shown in Figure 8.

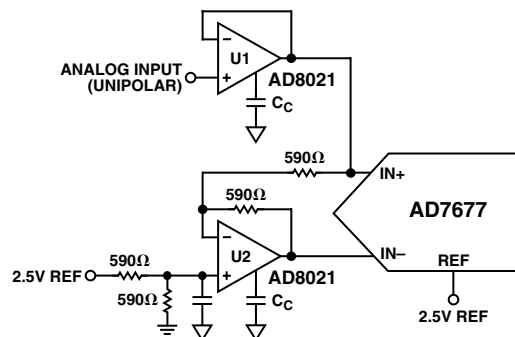


Figure 8. Single-Ended-to-Differential Driver Circuit

This configuration, when provided an input signal of 0 to V_{REF} , will produce a differential ± 2.5 V with midscale at 1.25 V.

If the application can tolerate more noise, the AD8138 can be used.

Driver Amplifier Choice

Although the AD7677 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7677 analog input circuit have to be able together to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, the settling at 0.1% or 0.01% is more commonly specified. It could significantly differ from the settling time at a 16-bit level and, therefore, it should be verified prior to the driver selection. The tiny op-amp, AD8021, which combines ultralow noise and a high gain bandwidth, meets this settling time requirement even when used with a high gain up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7677. The noise coming from the driver is filtered by the AD7677 analog input circuit one-pole, low-pass filter made by R_+ , R_- , and C_S . The SNR degradation due to the amplifier is:

$$SNR_{LOSS} = 20 \text{ LOG} \left(\frac{28}{\sqrt{784 + \frac{\pi}{4} f_{-3dB}^2 (N e_N)^2}} \right)$$

where

f_{-3dB} is the -3 dB input bandwidth in MHz of the AD7677 (15.8 MHz) or the cutoff frequency of the input filter if any used.

N is the noise factor of the amplifiers (1 if in buffer configuration).

e_N is the equivalent input noise voltage of each opamp in $nV/(\text{Hz})^{1/2}$.

AD7677

For instance, a driver with an equivalent input noise of $2 \text{ nV}/\sqrt{\text{Hz}}$ (like the AD8021) and configured as a buffer, thus with a noise gain of +1, the SNR degrades by only 0.07 dB with the filter in Figure 5, and 0.27 dB without.

- The driver needs to have a THD performance suitable to that of the AD7677.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where a dual version is needed and gain of 1 is used.

The AD8132 or the AD8138 could also be used to generate a differential signal from a single-ended signal.

The AD829 is another alternative where high frequency (above 1 MHz) performance is not required. In gain of 1, it requires an 82 pF compensation capacitor.

The AD8610 is also another option where low bias current is needed in low frequency applications.

Voltage Reference Input

The AD7677 uses an external 2.5 V voltage reference. The voltage reference input REF of the AD7677 has a dynamic input impedance. Therefore, it should be driven by a low impedance source with an efficient decoupling between REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a 1 μF ceramic capacitor and a low ESR tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance. 47 μF is an appropriate value for the tantalum capacitor when used with one of the recommended reference voltages:

- The low noise, low temperature drift ADR421 and AD780 voltage references
- The low power ADR291 voltage reference
- The low cost AD1582 voltage reference

For applications using multiple AD7677s, it is more effective to buffer the reference voltage with a low noise, very stable op amp like the AD8031.

Care should also be taken with the reference temperature coefficient of the voltage reference, which directly affects the full-scale accuracy if this parameter matters. For instance, a $\pm 15 \text{ ppm}/^\circ\text{C}$ tempco of the reference changes the full scale by $\pm 1 \text{ LSB}/^\circ\text{C}$.

Note that V_{REF} , as mentioned in the specification table, could be increased to $\text{AVDD} - 1.85 \text{ V}$. Since the input range is defined in terms of V_{REF} , this would essentially increase the range to make it a $\pm 3 \text{ V}$ input range with a reference voltage of 3 V. One of the benefits here is the increased SNR obtained as a result of this increase. The theoretical improvement as a result of this increase in reference is 1.58 dB ($20 \log [3/2.5]$). Due to the theoretical quantization noise however, the observed improvement is approximately 1 dB. The AD780 can be selected with a 3 V reference voltage.

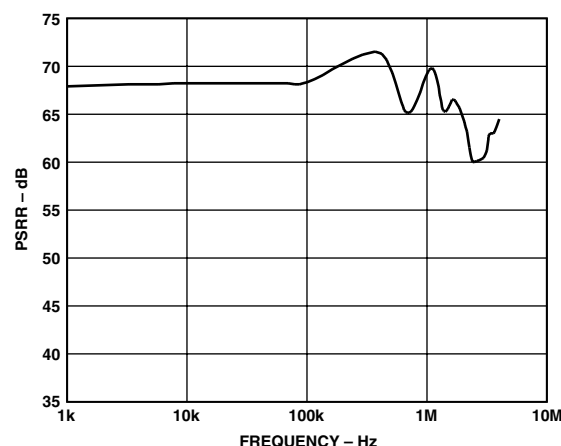


Figure 9. PSRR vs. Frequency

Power Supply

The AD7677 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7677 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3 V, and thus is free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 9.

POWER DISSIPATION

In Impulse Mode, the AD7677 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power saving when the conversion rate is reduced as shown in Figure 10. This feature makes the AD7677 ideal for very low power battery applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND) and OVDD should not exceed DVDD by more than 0.3 V.

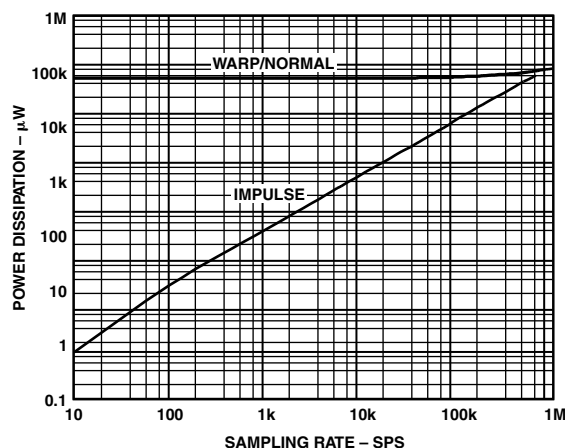


Figure 10. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 11 shows the detailed timing diagrams of the conversion process. The AD7677 is controlled by the signal $\overline{\text{CNVST}}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

In Impulse Mode, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held low when BUSY is low, the AD7677 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ low, the AD7677 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{\text{CNVST}}$ should be brought low once to initiate the conversion process. In this mode, the AD7677 could sometimes run slightly faster than the guaranteed limits in the Impulse Mode of 666 kSPS. This feature does not exist in warp or Normal modes.

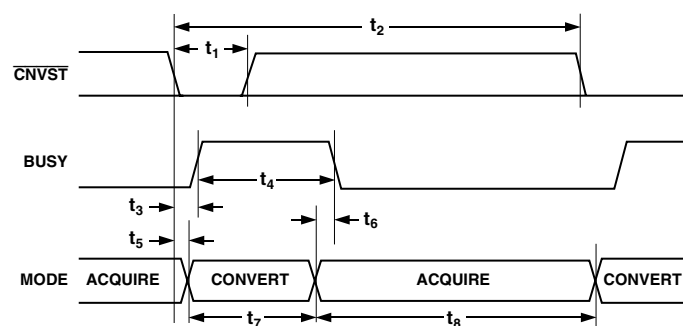


Figure 11. Basic Conversion Timing

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with this special care with fast, clean edges and levels, with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{\text{CNVST}}$ signal should have a very low jitter. Some solutions to achieve that are to use a dedicated oscillator for $\overline{\text{CNVST}}$ generation or, at least, to clock it with a high frequency low jitter clock as shown in Figure 5.

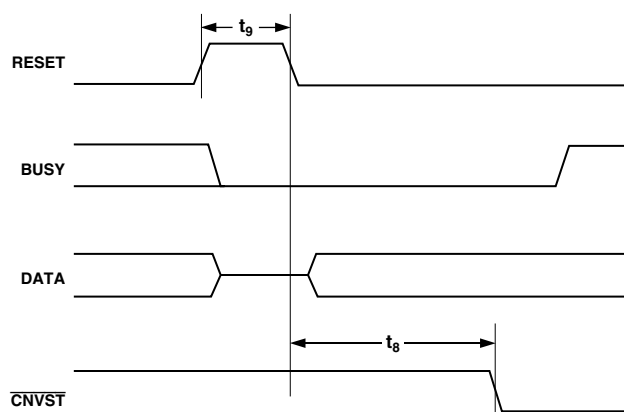


Figure 12. RESET Timing

DIGITAL INTERFACE

The AD7677 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel databus. The AD7677 digital interface also accommodates both 3 V or 5 V

logic by simply connecting the OVDD supply pin of the AD7677 to the host system interface digital supply. Finally, by using the $\text{OB}/2\overline{\text{C}}$ input pin, both two's complement or straight binary coding can be used.

The two signals, $\overline{\text{CS}}$ and $\overline{\text{RD}}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{\text{CS}}$ allows the selection of each AD7677 in multicircuits applications and is held low in a single AD7677 design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the databus.

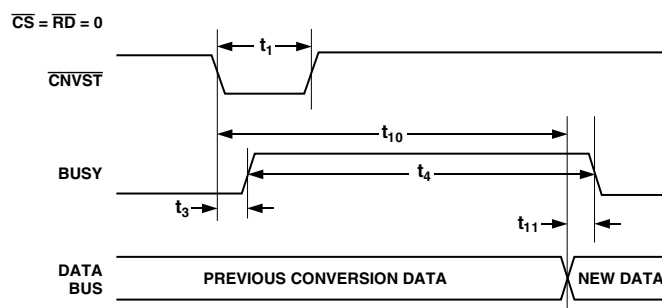


Figure 13. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7677 is configured to use the parallel interface (Figure 13) when the $\text{SER}/\overline{\text{PAR}}$ is held low. The data can either be read after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figure 14 and Figure 15. When the data is read during the conversion however, it is recommended that it is a read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

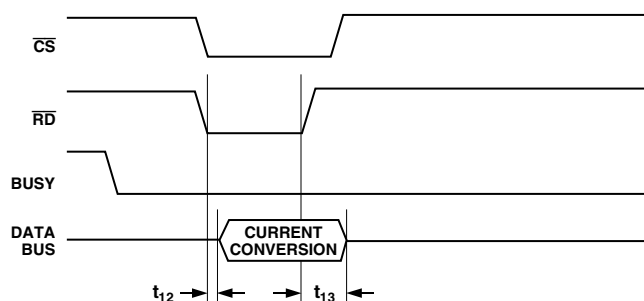


Figure 14. Slave Parallel Data Timing for Reading (Read After Convert)

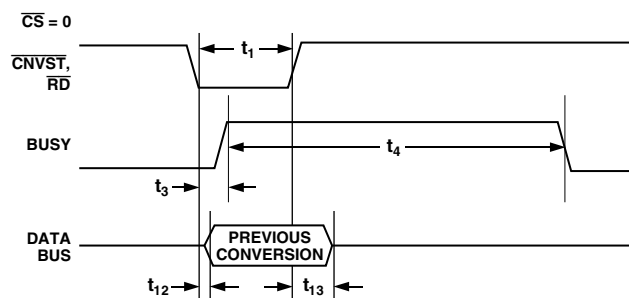


Figure 15. Slave Parallel Data Timing for Reading (Read During Convert)

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The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 16, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is low. When BYTESWAP is high, the LSB and MSB bytes are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16 bits of data can be read in 2 bytes on either D[15:8] or D[7:0].

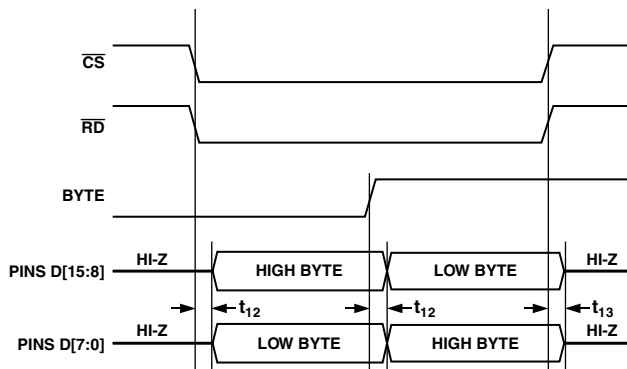


Figure 16. 8-Bit Parallel Interface

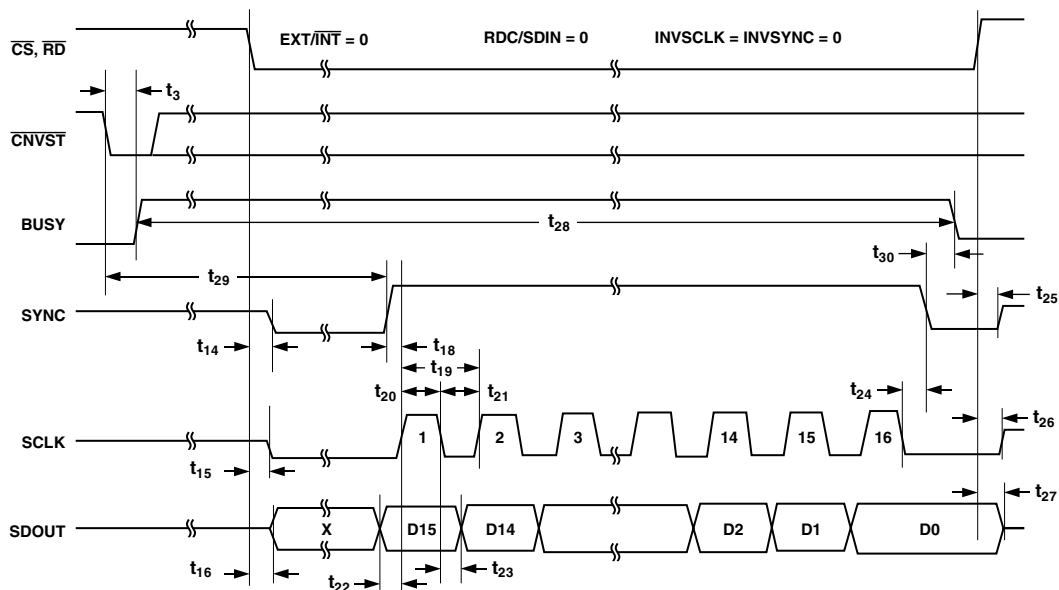


Figure 17. Master Serial Data Timing for Reading (Read After Convert)

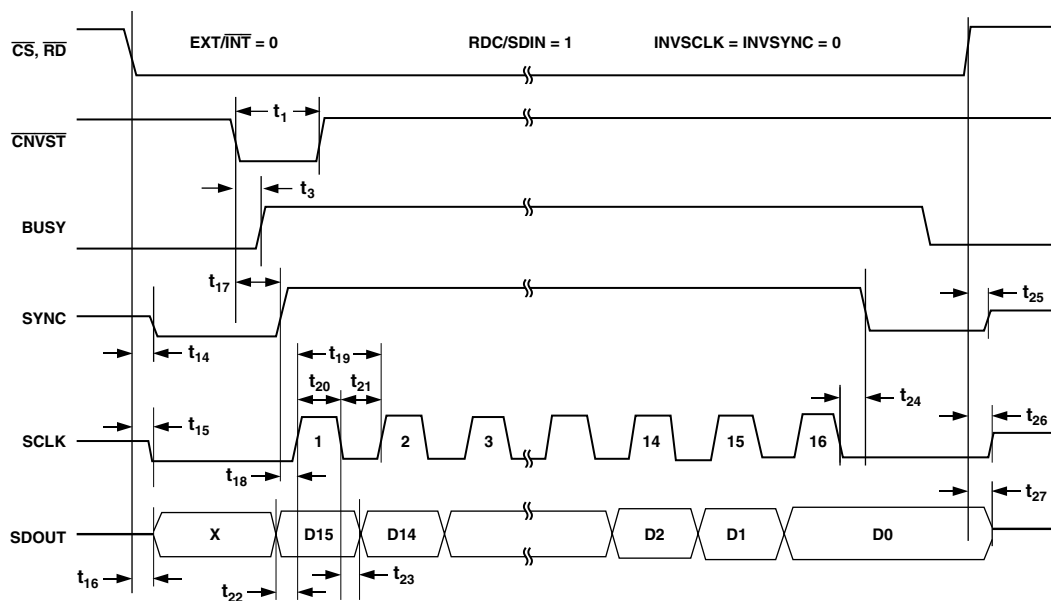


Figure 18. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SERIAL INTERFACE

The AD7677 is configured to use the serial interface when the SER/PAR is held high. The AD7677 outputs 16 bits of data, MSB first, on the SDOUT Pin. This data is synchronized with the 16 clock pulses provided on the SCLK Pin.

MASTER SERIAL INTERFACE

Internal Clock

The AD7677 is configured to generate and provide the serial data clock SCLK when the EXT/INT Pin is held low. The AD7677 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. The output data is valid on both the rising and falling edge of the data clock. Depending on RDC/SDIN input, the data can be read after each conversion, or during the following conversion.

Figure 17 and Figure 18 show the detailed timing diagrams of these two modes.

Usually, because the AD7677 is used with a fast throughput, the mode master, read during conversion, is the most recommended serial mode when it can be used.

In read-after-conversion mode, unlike in other modes, it should be noted that the signal BUSY returns low after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

In read-during-conversion mode, the serial clock and data toggle at appropriate instances minimizes potential feedthrough between digital activity and the critical conversion decisions.

To accommodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK.

SLAVE SERIAL INTERFACE

External Clock

The AD7677 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/INT pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by \overline{CS} and the data are output when both \overline{CS} and \overline{RD} are low. Thus, depending on \overline{CS} , the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either

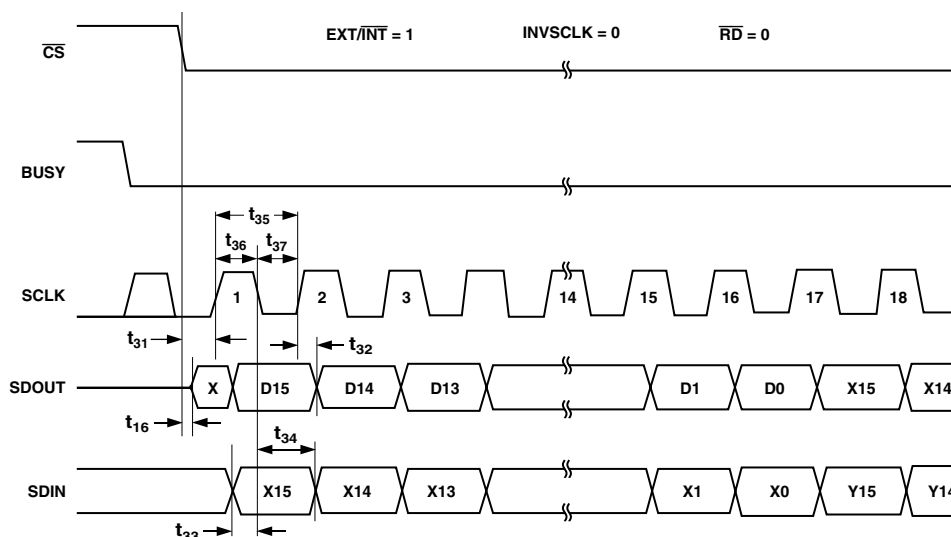


Figure 19. Slave Serial Data Timing for Reading (Read After Convert)

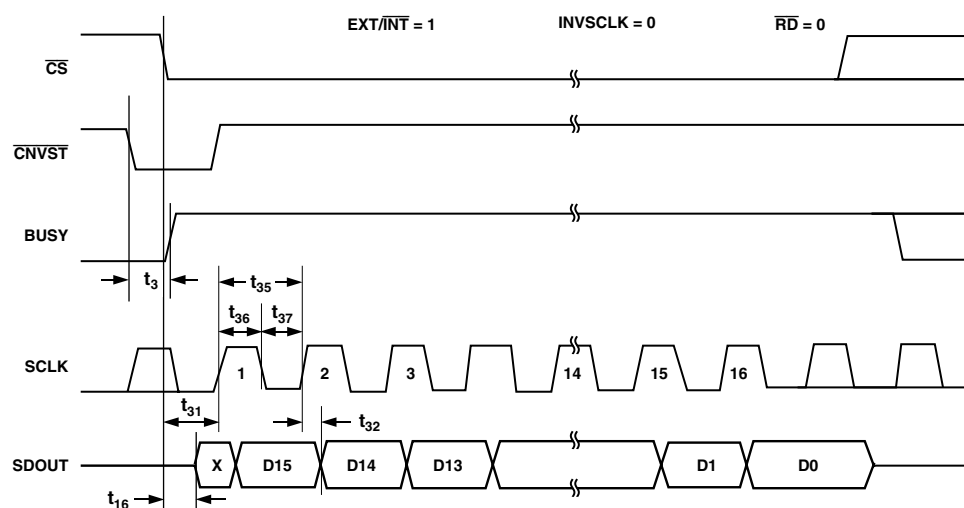


Figure 20. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

AD7677

normally high or normally low when inactive. Figure 19 and Figure 20 show the detailed timing diagrams of these methods.

While the AD7677 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7677 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read after Conversion

This mode is the most recommended of the serial slave modes. Figure 19 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both \overline{CS} and \overline{RD} are low. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7677 provides a “daisy chain” feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when it is desired as it is, for instance, in isolated multiconverters applications.

An example of the concatenation of two devices is shown in Figure 21. Simultaneous sampling is possible by using a common \overline{CNVST} signal. It should be noted that the RDC/SDIN input is latched on the opposite edge of SCLK of the one used to shift out the data on SDOUT. Hence, the MSB of the “upstream” converter just follows the LSB of the “downstream” converter on the next SCLK cycle.

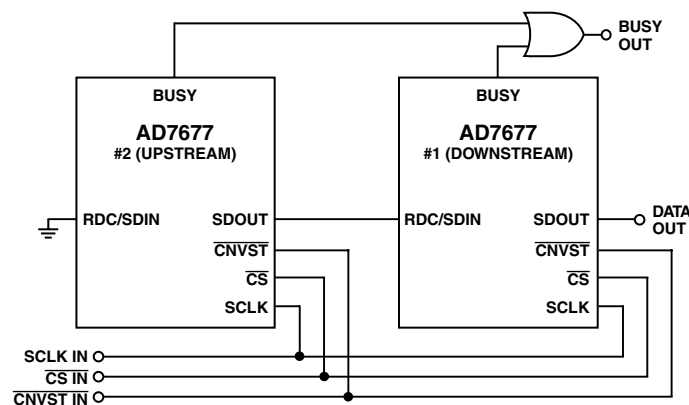


Figure 21. Two AD7677s in a “Daisy Chain” Configuration

External Clock Data Read During Conversion

Figure 20 shows the detailed timing diagrams of this method. During a conversion, while both CS and RD are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses, and is valid on both rising and falling edges of the clock. The 16 bits have to be read before the

current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no “daisy chain” feature in this mode, and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 25 MHz, when Impulse Mode is used, 32 MHz when normal, or 40 MHz when Warp Mode is used, is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated. That allows the use of a slower clock speed like 18 MHz in Impulse Mode, 21 MHz in Normal Mode, and 26 MHz in Warp Mode.

MICROPROCESSOR INTERFACING

The AD7677 is ideally suited for traditional dc measurement applications supporting a microprocessor and ac signal processing applications interfacing to a digital signal processor. The AD7677 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7677 to prevent digital noise from coupling into the ADC. The following sections illustrate the use of the AD7677 with an SPI equipped microcontroller, the ADSP-21065L and ADSP-218x signal processors.

SPI Interface (MC68HC11)

Figure 22 shows an interface diagram between the AD7677 and an SPI-equipped microcontroller like the MC68HC11. To accommodate the slower speed of the microcontroller, the AD7677 acts as a slave device and data must be read after conversion. This mode also allows the “daisy chain” feature. The convert command could be initiated in response to an internal timer interrupt. The reading of output data, one byte at a time, if necessary, could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the microcontroller. The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1, and SPI interrupt enable (SPIE) = 1 by writing to the SPI Control Register (SPCR). The IRQ is configured for edge-sensitive-only operation (IRQE = 1 in OPTION Register).

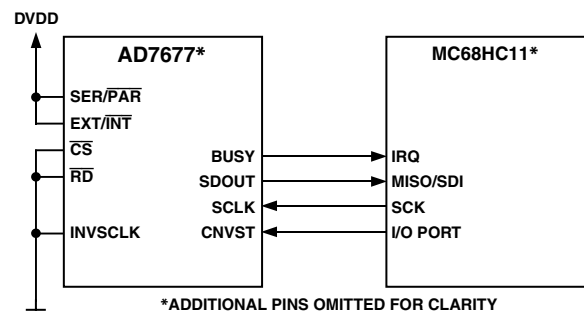


Figure 22. Interfacing the AD7677 to SPI Interface

ADSP-21065L in Master Serial Interface

As shown in Figure 23, the AD7677 can be interfaced to the ADSP-21065L using the serial interface in master mode without any glue logic required. This mode combines the advantages of reducing the wire connections and the ability to read the data during or after conversion maximum speed transfer (DIVSCLK [0:1] both low).

The AD7677 is configured for the internal clock mode ($\overline{\text{EXT/INT}}$ low) and acts, therefore, as the master device. The convert command can be generated by either an external low jitter oscillator or, as shown, by a FLAG output of the ADSP-21065L, or by a frame output TFS of one serial port of the ADSP-21065L that can be used like a timer. The serial port on the ADSP-21065L is configured for external clock ($\text{IRFS} = 0$), rising edge active ($\text{CKRE} = 1$), external late framed sync signals ($\text{IRFS} = 0$, $\text{LAFS} = 1$, $\text{RFSR} = 1$), and active high ($\text{LRFS} = 0$). The serial port of the ADSP-21065L is configured by writing to its receive control register (SRCTL)—see ADSP-2106x SHARC User's Manual. Because the serial port within the ADSP-21065L will be seeing a discontinuous clock, an initial word reading has to be done after the ADSP-21065L has been reset to ensure that the serial port is properly synchronized to this clock during each following data read operation.

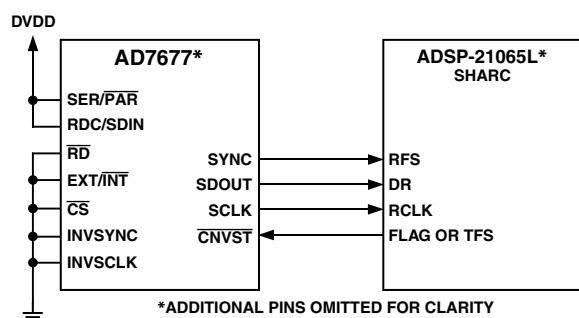


Figure 23. Interfacing to the ADSP-21065L Using the Serial Master Mode

APPLICATION HINTS

Layout

The AD7677 has very good immunity to noise on the power supplies as can be seen in Figure 9. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7677 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7677, or at least as close as possible to the AD7677. If the AD7677 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7677.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground

plane should be allowed to run under the AD7677 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7677 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply's impedance presented to the AD7677 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply's pins, AVDD, DVDD, and OVDD, close to and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 μF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7677 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 5, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high-frequency spikes.

The AD7677 has four different ground pins; REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

Evaluating the AD7677 Performance

A recommended layout for the AD7677 is outlined in the evaluation board for the AD7677. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control BRD2.

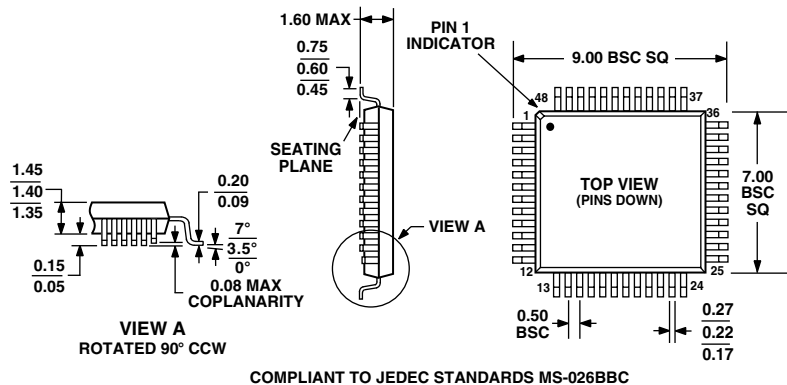
OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]

1.4 mm Thick

(ST-48)

Dimensions shown in millimeters

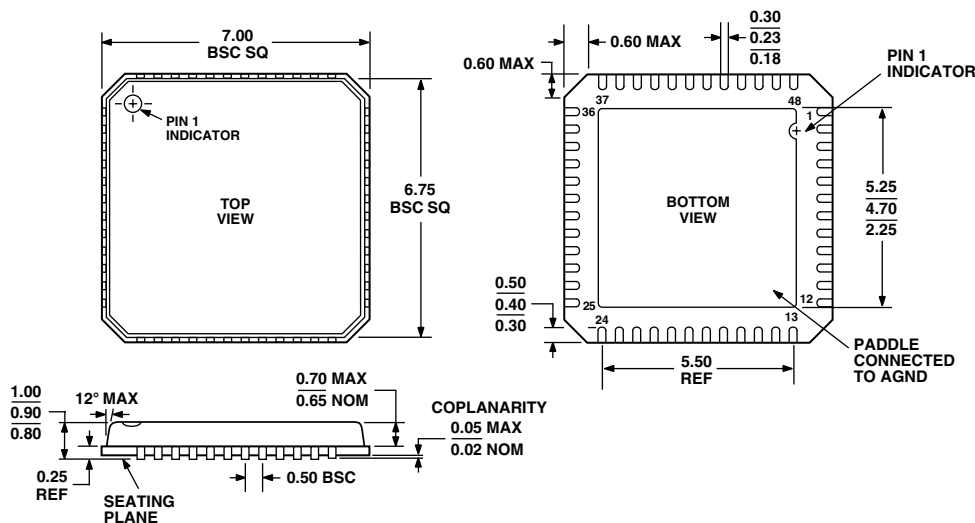


48-Lead Frame Chip Scale Package [LFCSP]

7 mm × 7 mm Body

(CP-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Revision History

Location	Page
7/02—Data Sheet changed from REV. 0 to REV. A.	
Added 48-Lead LFCSP to FEATURES and GENERAL DESCRIPTION	1
Added PulSAR Selection table	1
Edits to NOTES	3
Changes to ABSOLUTE MAXIMUM RATINGS	5
Additions to ORDERING GUIDE	5
Edits to PIN FUNCTION DESCRIPTIONS	6
Changes to Power Supply section	14
Added 48-Lead Frame Chip Scale Package (LFCSP)	20