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REVISION HISTORY

1/11—Rev. B to Rev. C
Added Automotive Model and Information ... Throughout

12/09—Rev. A to Rev. B
Changes to Ordering Guide ... 21

6/06—Rev. 0 to Rev. A
Updated Format ... Universal
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Ordering Guide ... 21

11/00—Revision 0: Initial Version

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SPECIFICATIONS

AD7398 12-BIT VOLTAGE OUTPUT DAC

V_{DD} = 5 V, V_{SS} = 0 V; or V_{DD} = +5 V, V_{SS} = −5 V, V_{REF} = +2.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	3 V to 5 V ± 10%	±5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL		±1.5	±1.5	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	7	±2.5	mV max
Full-Scale Voltage Error	V_{FSE}	Data = FFF_H	±2.5	±2.5	mV max
Full-Scale Tempco[3]	TCV_{FS}		1.5	1.5	ppm/°C typ
REFERENCE INPUT					
V_{REF}IN Range[4]	V_{REF}		0/V_{DD}	V_{SS}/V_{DD}	V min/max
Input Resistance[5]	R_{REF}	Data = 555_H, worst case	35	35	kΩ typ[6]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Voltage Range	V_{OUT}		0 to V_{REF}	0 to V_{REF}	V
Output Current	I_{OUT}	Data = 800_H, ΔV_{OUT} = 4 LSBs	±5	±5	mA typ
Capacitive Load[3]	C_L	No oscillation	200	400	pF max
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}	V_{DD} = 3 V	0.5		V max
		V_{DD} = 5 V	0.8	0.8	V max
Logic Input High Voltage	V_{IH}	CLK only	80% V_{DD}	4.0	V min
			2.1 to 2.4	2.4	V min
Input Leakage Current	I_{IL}		1	1	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 7]					
Clock Frequency	f_{CLK}		11	16.6	MHz max
Clock Width High	t_{CH}		45	30	ns min
Clock Width Low	t_{CL}		45	30	ns min
$\overline{CS}$ to Clock Setup	t_{CSS}		10	5	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		20	15	ns min
Load DAC Pulse Width	t_{LDAC}		45	30	ns min
Data Setup	t_{DS}		15	10	ns min
Data Hold	t_{DH}		10	5	ns min
Load Setup to $\overline{CS}$	t_{LDS}		0	0	ns min
Load Hold to $\overline{CS}$	t_{LDH}		20	15	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	2	2	V/µs typ
Settling Time[8]	t_S	To ±0.1% of full scale	6	6	µs typ
Shutdown Recovery	t_{SDR}		6	6	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	150	150	nVs typ
Digital Feedthrough	Q_{DF}		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} 1 V p-p, data = 000_H, f = 100 kHz	−63	−63	dB typ

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Parameter	Symbol	Condition	3 V to 5 V ± 10%	±5 V ± 10%	Unit
SUPPLY CHARACTERISTICS					
Shutdown Supply Current	I_{DD_SD}	No load	30/60	30/60	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, no load, −40°C < T_A < +125°C	1.5/2.8	1.6/3	mA typ/max
	I_{DD}	V_{IL} = 0 V, no load, −40°C < T_A < +85°C	1.5/2.6	1.6/2.8	mA typ/max
Negative Supply Current	I_{SS}	V_{IL} = 0 V, no load	1.5/2.5	1.6/2.7	mA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, no load	5	16	mW typ
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

[1] One LSB = V_{REF}/4096 V for the 12-bit AD7398.
[2] The first eight codes (000_H to 007_H) are excluded from the linearity error measurement in single-supply operation.
[3] These parameters are guaranteed by design and not subject to production testing.
[4] When V_{REF} is connected to either the V_{DD} or the V_{SS} power supply, the corresponding V_{OUT} voltage programs between ground and the supply voltage minus the offset voltage of the output buffer, which is the same as the V_{ZSE} error specification. See additional information in the Theory of Operation section.
[5] Input resistance is code dependent.
[6] Typicals represent average readings measured at 25°C.
[7] All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[8] The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

AD7399 10-BIT VOLTAGE OUTPUT DAC

V_{DD} = 5 V, V_{SS} = 0 V; or V_{DD} = +5 V, V_{SS} = −5 V; V_{REF} = +2.5 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Condition	3 V to 5 V ± 10%	±5 V ± 10%	Unit
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL		±1	±1	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	7	±4	mV max
Full-Scale Voltage Error	V_{FSE}	Data = $3FF_H$	±15	±15	mV max
Full-Scale Tempco[3]	TCV_{FS}		1.5	1.5	ppm/°C typ
REFERENCE INPUT					
V_{REF}IN Range[4]	V_{REF}		0/V_{DD}	V_{SS}/V_{DD}	V min/max
Input Resistance[5]	R_{REF}	Data = 155_H, worst case	40	40	kΩ typ[6]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Voltage Range	V_{OUT}		0 to V_{REF}	0 to V_{REF}	V
Output Current	I_{OUT}	Data = 200_H, ΔV_{OUT} = 1 LSB	±5	±5	mA typ
Capacitive Load[3]	C_L	No oscillation	200	400	pF max
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}	V_{DD} = 3 V	0.5		V max
		V_{DD} = 5 V	0.8	0.8	V max
Logic Input High Voltage	V_{IH}	CLK only	80% V_{DD}	4.0	V min
			2.1 to 2.4	2.4	V min
Input Leakage Current	I_{IL}		1	1	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 7]					
Clock Frequency	f_{CLK}		11	16.6	MHz max
Clock Width High	t_{CH}		45	30	ns min
Clock Width Low	t_{CL}		45	30	ns min
$\overline{CS}$ to Clock Setup	t_{CSS}		10	5	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		20	15	ns min
Load DAC Pulse Width	t_{LDAC}		45	30	ns min
Data Setup	t_{DS}		15	10	ns min
Data Hold	t_{DH}		10	5	ns min
Load Setup to $\overline{CS}$	t_{LDS}		0	0	ns min
Load Hold to $\overline{CS}$	t_{LDH}		20	15	ns min

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Parameter	Symbol	Condition	3 V to 5 V ± 10%	±5 V ± 10%	Unit
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	2	2	V/µs typ
Settling Time[8]	t_S	To ±0.1% of full scale	6	6	µs typ
Shutdown Recovery	t_{SDR}		6	6	µs typ
DAC Glitch	Q	Code $1FF_H$ to 200_H to $1FF_H$	150	150	nVs typ
Digital Feedthrough	Q_{DF}		15	15	nVs typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} + 1 V p-p, data = 000_H, f = 100 kHz	−63	−63	dB typ
SUPPLY CHARACTERISTICS					
Shutdown Supply Current	I_{DD_SD}	No load	30/60	30/60	µA typ/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, no load, −40°C < T_A < +125°C	1.5/2.8	1.6/3	mA typ/max
	I_{DD}	V_{IL} = 0 V, no load, −40°C < T_A < +85°C	1.5/2.6	1.6/2.8	mA typ/max
Negative Supply Current	I_{SS}	V_{IL} = 0 V, no load	1.5/2.5	1.6/2.7	mA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, no load	5	16	mW typ
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

[1] One LSB = V_{REF}/1024 V for the 10-bit AD7399.
[2] The first two codes (000_H and 001_H) are excluded from the linearity error measurement in single-supply operation.
[3] These parameters are guaranteed by design and not subject to production testing.
[4] When V_{REF} is connected to either the V_{DD} or the V_{SS} power supply, the corresponding V_{OUT} voltage programs between ground and the supply voltage minus the offset voltage of the output buffer, which is the same as the V_{ZSE} error specification. See additional discussion in the Theory of Operation section.
[5] Input resistance is code dependent.
[6] Typicals represent average readings measured at 25°C.
[7] All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[8] The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

TIMING DIAGRAMS

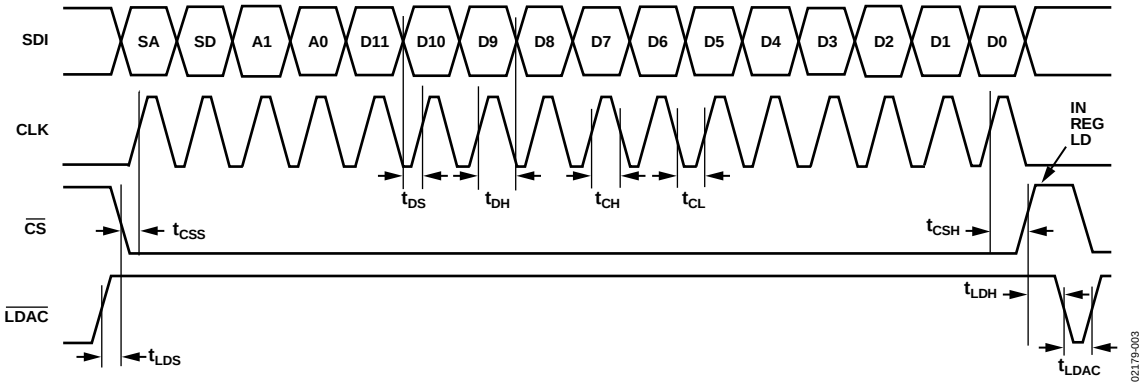

Figure 3. AD7398 Timing Diagram (AD7399 with SDI = 14 Bits Only)

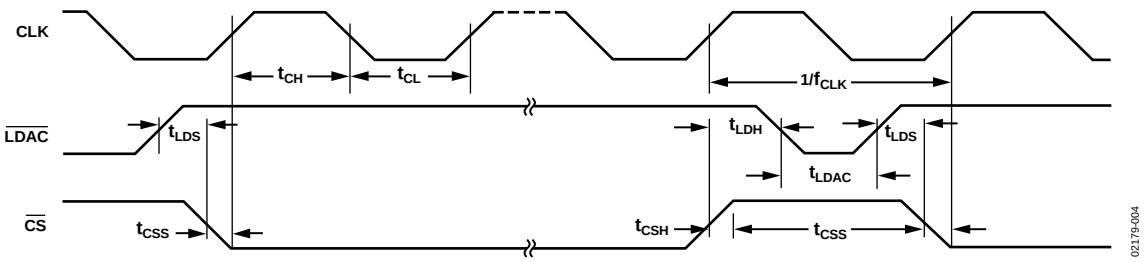

Figure 4. Continuous Clock Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +7 V
V_{SS} to GND	+0.3 V, −7 V
V_{REF} to GND	V_{SS}, V_{DD}
Logic Inputs to GND	−0.3 V, +8 V
V_{OUT} to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND	50 mA
Thermal Resistance (θ_{JA})	
16-Lead SOIC_W Package (RW-16)	158°C/W
16-Lead TSSOP Package (RU-16)	180°C/W
Maximum Junction Temperature (T_J Max)	150°C
Package Power Dissipation	(T_J Max − T_A)/θ_{JA}
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

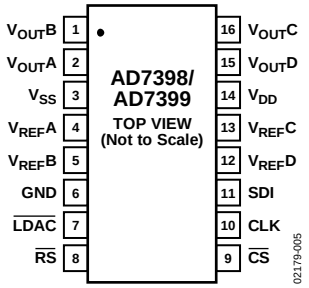

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{OUT}B$	DAC B Voltage Output.
2	$V_{OUT}A$	DAC A Voltage Output.
3	V_{SS}	Negative Power Supply Input. Specified range of operation 0 V to −5.5 V.
4	$V_{REF}A$	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. Pin can be tied to V_{DD} pin or V_{SS} pin.
5	$V_{REF}B$	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. Pin can be tied to V_{DD} pin or V_{SS} pin.
6	GND	Ground Pin.
7	$\overline{LDAC}$	Load DAC Register Strobe. Level sensitive active low. Transfers all input register data to DAC registers. Asynchronous active low input. See Table 5 for operation.
8	$\overline{RS}$	Resets Input and DAC Registers to All Zero Codes. Shift register contents unchanged.
9	$\overline{CS}$	Chip Select. Active low input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}$ returns high. Does not effect $\overline{LDAC}$ operation.
10	CLK	Schmitt Triggered Clock Input. Positive edge clocks data into shift register.
11	SDI	Serial Data Input. Input data loads directly into the shift register.
12	$V_{REF}D$	DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. Pin can be tied to V_{DD} pin or V_{SS} pin.
13	$V_{REF}C$	DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. Pin can be tied to V_{DD} pin or V_{SS} pin.
14	V_{DD}	Positive Power Supply Input. Specified range of operation 3 V to 5 V ± 10%.
15	$V_{OUT}D$	DAC D Voltage Output.
16	$V_{OUT}C$	DAC C Voltage Output.

Table 5. Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	No effect	No effect	No effect
L	L	H	No effect	No effect	No effect
L	↑+	H	Shift register data advanced one bit	Latched	No effect
L	H	H	No effect	Latched	No effect
↑+	L/H	H	No effect	Updated with shift register contents	No effect
H	X	L	No effect	Latched	Transparent
H	X	↑+	No effect	Latched	Latched

NOTES
1. ↑+ = Positive logic transition; ↓− = Negative logic transition; X = Don't Care.
2. At power-on, both the input register and the DAC register are loaded with all zeros.
3. During power shutdown, reprogramming of any internal registers can take place, but the output amplifiers do not produce the new values until the part is taken out of shutdown mode.
4. The $\overline{LDAC}$ input is a level-sensitive input that controls the four DAC registers.

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INPUT REGISTERS

AD7398 SERIAL INPUT REGISTER DATA FORMAT

Data is loaded in the MSB first format.

MSB **LSB**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SA	SD	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE
Bit Position B14 and Bit Position B15 are the SD and SA power shutdown control bits. If SA is set to Logic 1, all DACs are placed in the power shutdown mode. If SD is set to Logic 1, the address decoded by Bit B12 and Bit B13 (A0 and A1) determine the DAC channel that is placed in the power shutdown state.

AD7399 SERIAL INPUT REGISTER DATA FORMAT

Data is loaded in the MSB first format.

MSB **LSB**

B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
SA	SD	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE
Bit Position B12 and Bit Position B13 are the SD and SA power shutdown control bits. If SA is set to Logic 1, all DACs are placed in the power shutdown mode. If SD is set to Logic 1, the address decoded by Bit B10 and Bit B11 (A0 and A1) determine the DAC channel that is placed in the power shutdown state.

Table 6. AD7398/AD7399 Address Decode Control

SA	SD	A1	A0	DAC Channel Affected
1	X	X	X	All DACs shutdown
0	1	0	0	DAC A shutdown
0	1	0	1	DAC B shutdown
0	1	1	0	DAC C shutdown
0	1	1	1	DAC D shutdown
0	0	0	0	DAC A input register decoded
0	0	0	1	DAC B input register decoded
0	0	1	0	DAC C input register decoded
0	0	1	1	DAC D input register decoded

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TERMINOLOGY

Relative Accuracy (INL)
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Figure 6 illustrates a typical INL vs. code plot.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. Figure 8 illustrates a typical DNL vs. code plot.

Zero-Scale Error (V_{ZSE})
Zero-scale error is a measure of the output voltage error from zero voltage when zero code is loaded to the DAC register.

Full-Scale Error (V_{FSE})
Full-scale error is a measure of the output voltage error from full-scale voltage when full-scale code is loaded to the DAC register.

Full-Scale Temperature Coefficient (TC_{VFS})
This is a measure of the change in full-scale error with a change in temperature. It is expressed in ppm/°C or mV/°C.

DAC Glitch Impulse (Q)
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV s and is measured when the digital input code is changed by 1 LSB at the major carry transition (midscale transition). A plot of the glitch impulse is shown in Figure 15.

Digital Feedthrough (Q_{DF})
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{CS}$ is held high while the CLK and SDI signals are toggled. It is specified in nV – s, and is measured with a full-scale code change on the data bus, such as from all 0s to all 1s and vice versa. A typical plot of digital feedthrough is shown in Figure 16.

Power Supply Sensitivity (PSS)
This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply sensitivity is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough (V_{OUT}/V_{REF})
This is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in dB or mV p-p.

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TYPICAL PERFORMANCE CHARACTERISTICS

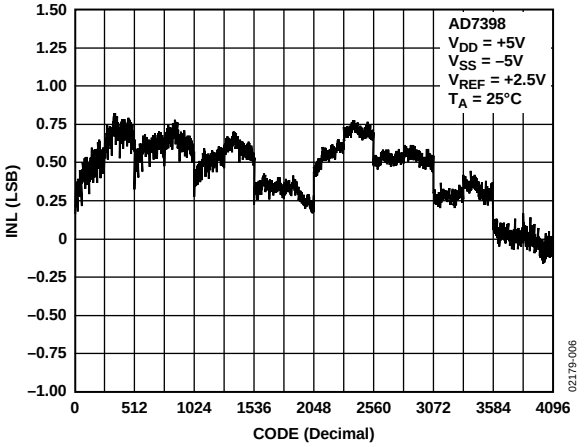

Figure 6. AD7398 INL vs. Code (T_A = 25°C)

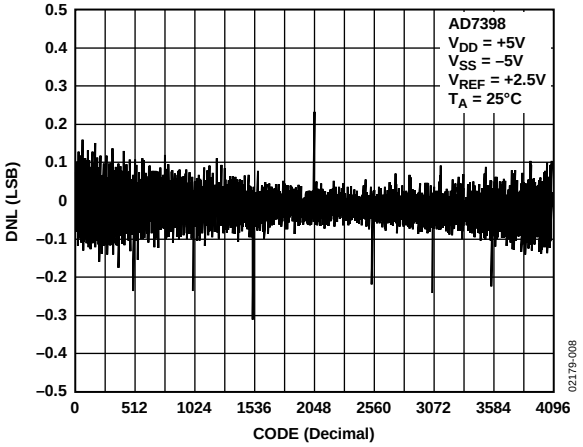

Figure 8. AD7398 DNL vs. Code (T_A = 25 °C)

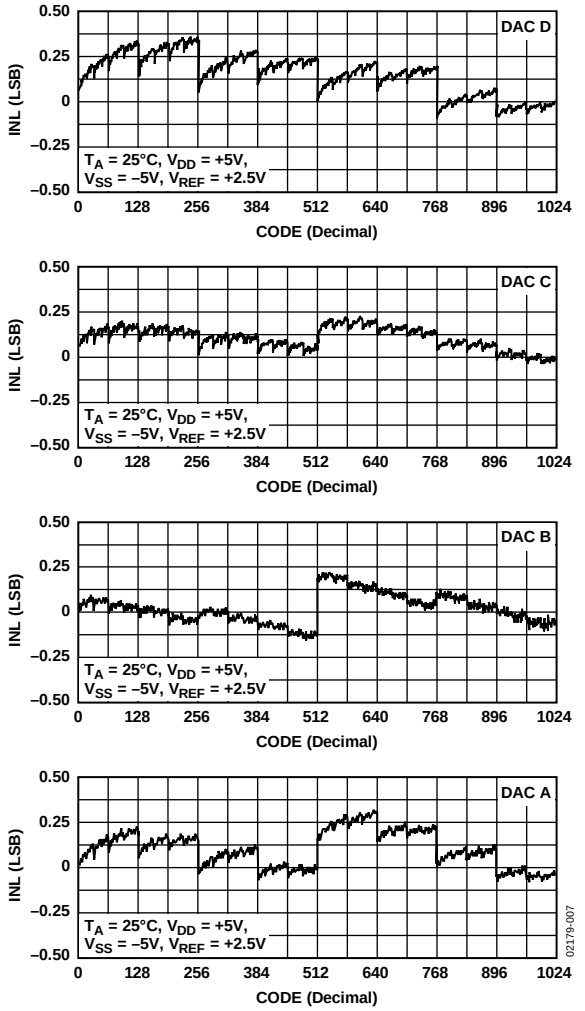

Figure 7. AD7399 INL vs. Code (T_A = 25°C)

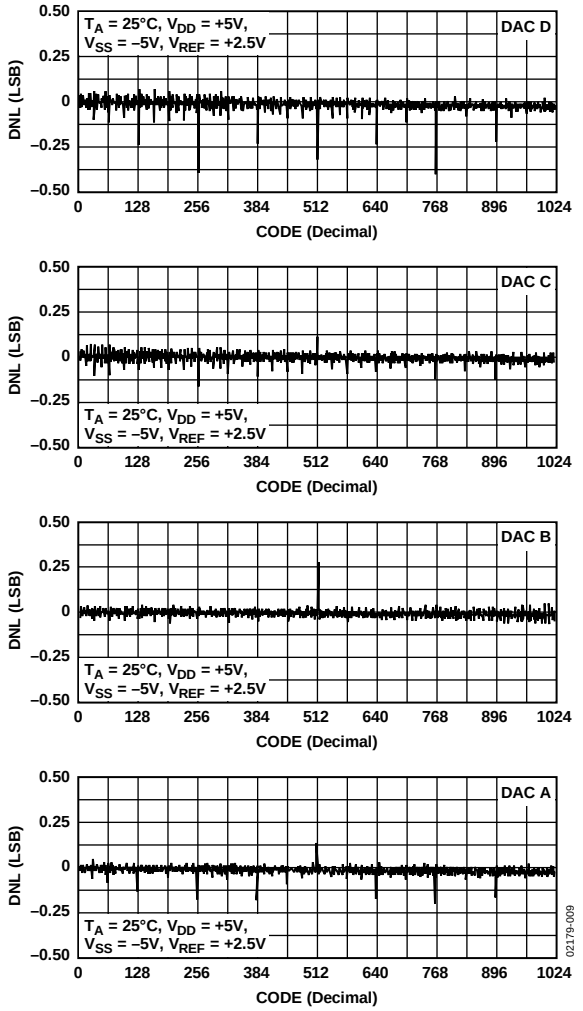

Figure 9. AD7399 DNL vs. Code (T_A = 25 °C)

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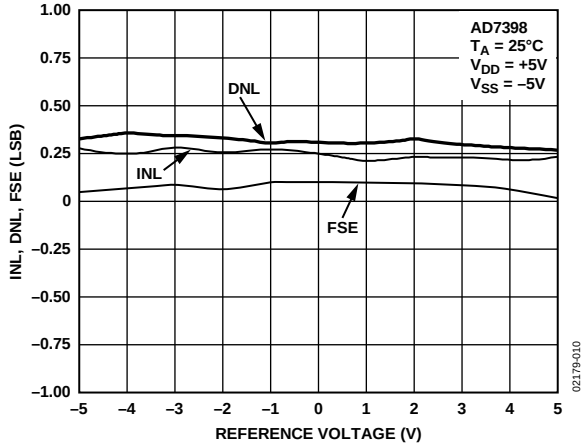

Figure 10. AD7398 INL, DNL, FSE vs. Reference Voltage

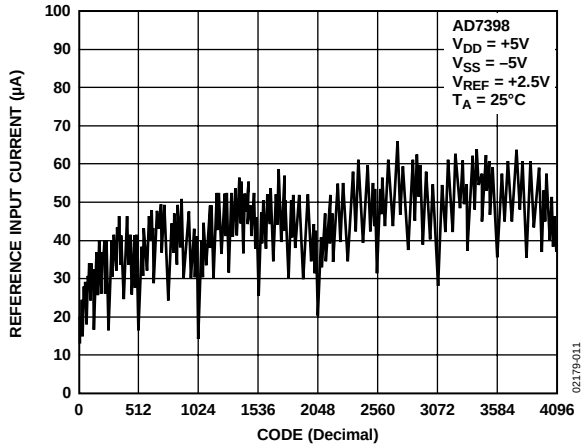

Figure 11. AD7398 Reference Input Current vs. Code

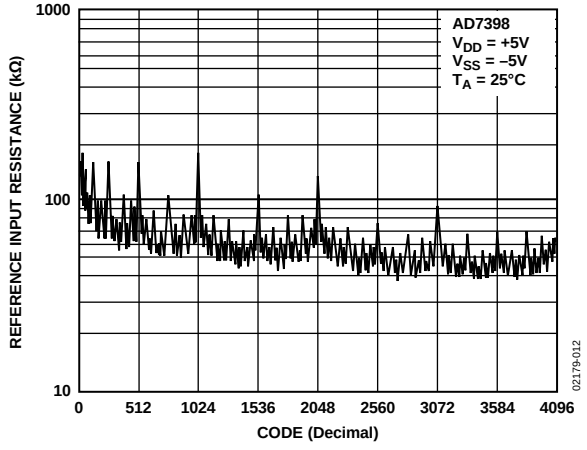

Figure 12. AD7398 Reference Input Resistance vs. Code

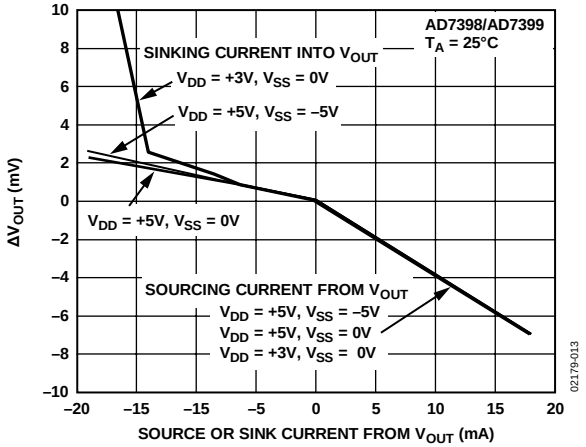

Figure 13. ΔV_{OUT} vs. Load Current

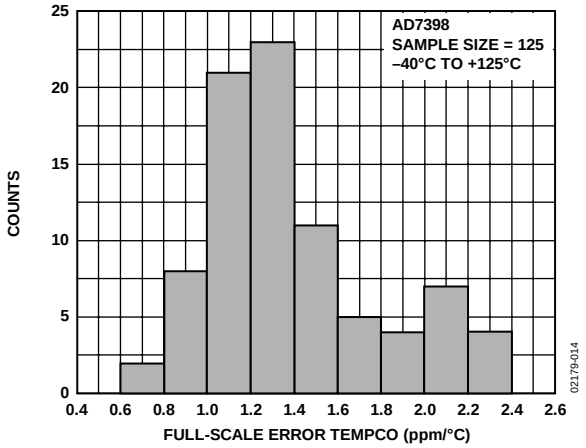

Figure 14. AD7398 Full-Scale Error Tempco

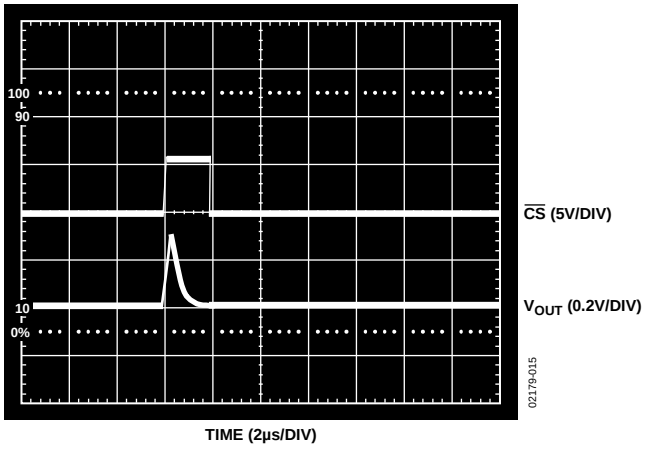

Figure 15. AD7398 Midscale Glitch

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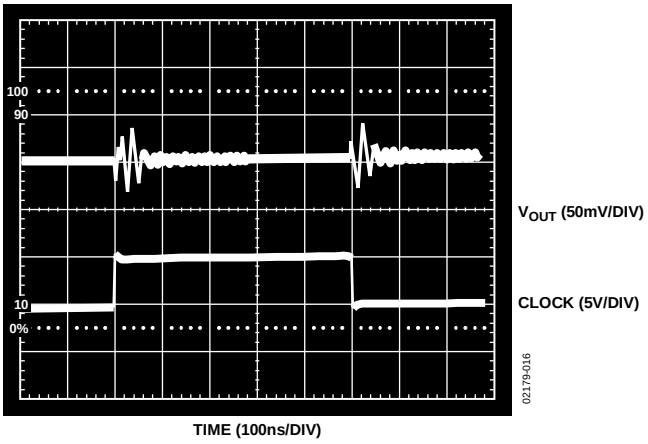

Figure 16. AD7398 Digital Feedthrough

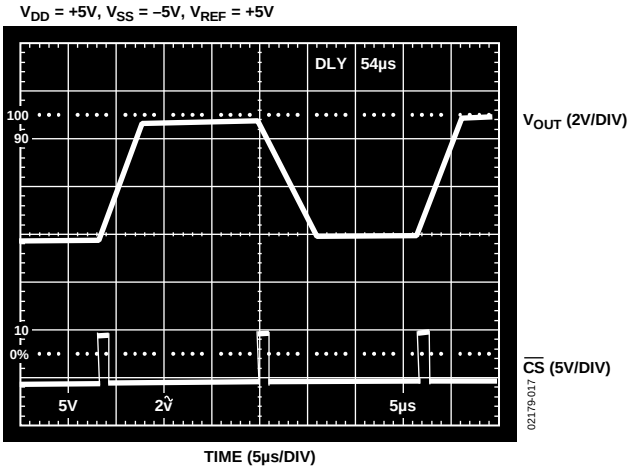

Figure 17. AD7398 Large Signal Settling Time

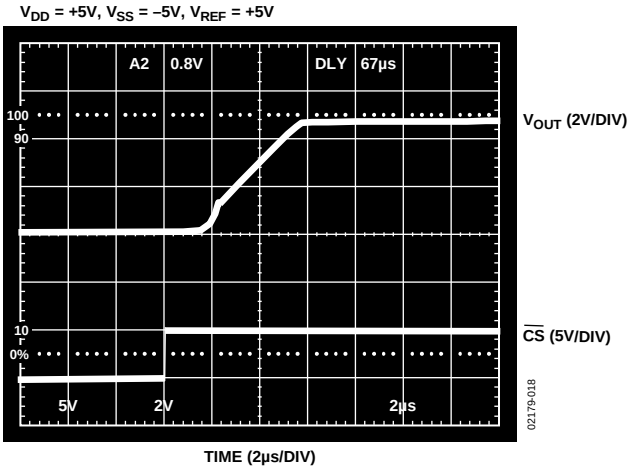

Figure 18. AD7398 Shutdown Recovery

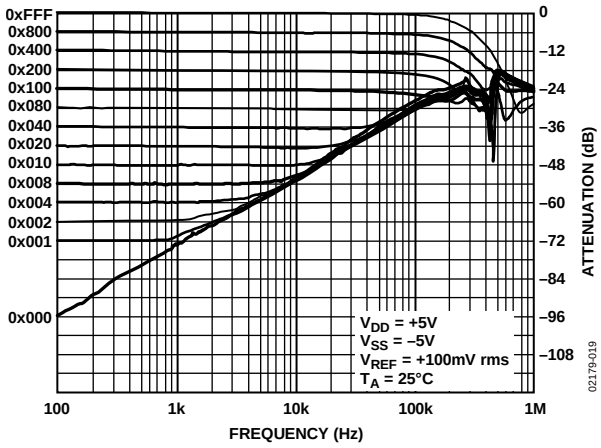

Figure 19. AD7398 Multiplying Gain vs. Frequency

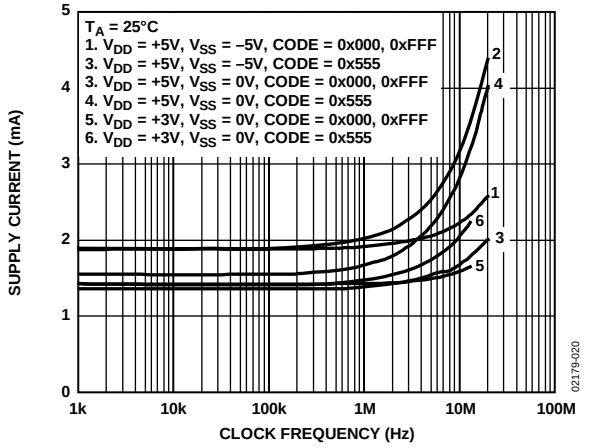

Figure 20. AD7398 Supply Current vs. Clock Frequency

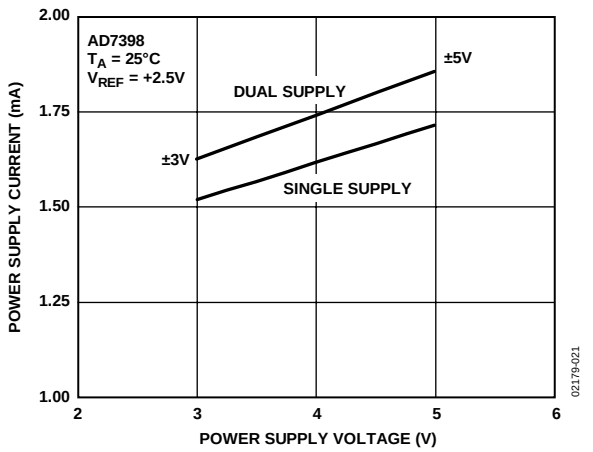

Figure 21. AD7398 Supply Current vs. Supply Voltage

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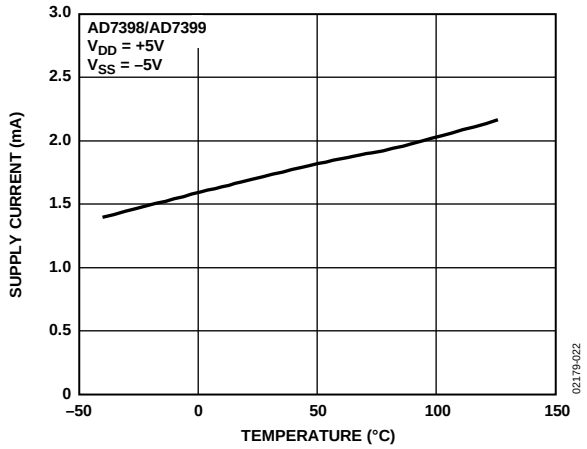

Figure 22. Supply Current vs. Temperature

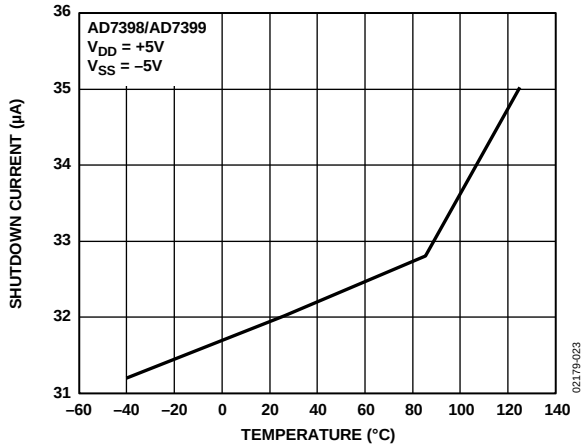

Figure 23. Shutdown Current vs. Temperature

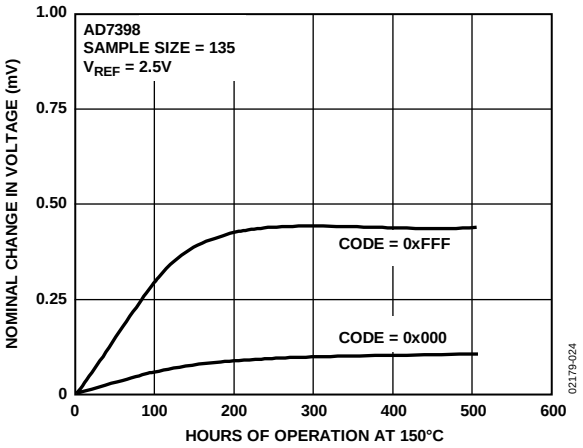

Figure 24. AD7398 Long-Term Drift

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THEORY OF OPERATION

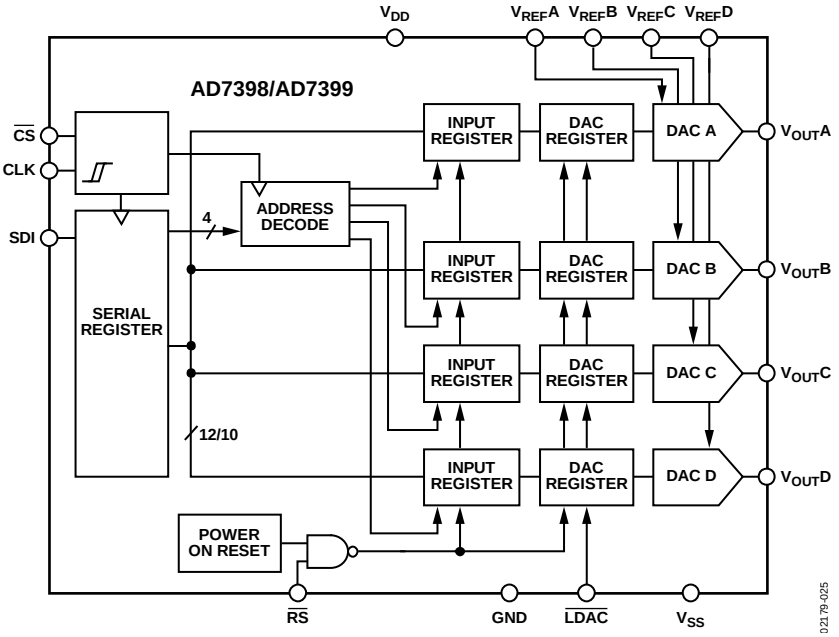

Figure 25. Simplified Block Diagram

The AD7398/AD7399 contain four 12-bit and 10-bit, respectively, voltage output, digital-to-analog converters. Each DAC has its own independent multiplying reference input. Both the AD7398 and AD7399 use a 3-wire, SPI-compatible serial data interface, with an asynchronous $\overline{RS}$ pin for zero-scale reset. In addition, an $\overline{LDAC}$ strobe enables four-channel simultaneous updates for hardware-synchronized output voltage changes.

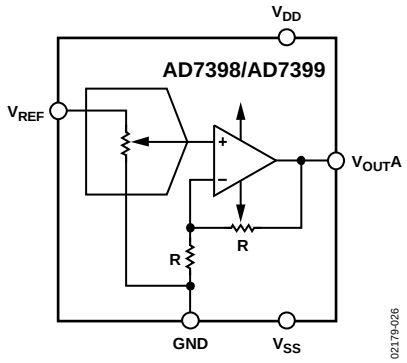

Figure 26. Simplified DAC Channel

DAC OPERATION

The internal R-2R ladder of the AD7398/AD7399 operates in the voltage switching mode, maintaining an output voltage that is the same polarity as the input reference voltage. A proprietary scaling technique is used to attenuate the input reference voltage in the DAC. The output buffer amplifies the internal DAC output to achieve a V_{REF} to V_{OUT} gain of unity.

The nominal DAC output voltage is determined by the externally applied V_{REF} and the digital data (D) as

$$V_{OUT} = V_{REF} \times D/4096 \text{ (For AD7398)} \quad (1)$$

$$V_{OUT} = V_{REF} \times D/1024 \text{ (For AD7399)} \quad (2)$$

where:

D is the 12-bit or 10-bit decimal equivalent of the data word.
V_{REF} is the externally applied reference voltage.

In order to maintain good analog performance, the user should bypass power supplies with 0.01 µF ceramic capacitors (mount them close to the supply pins) and 1 µF to 10 µF tantalum capacitors in parallel. In addition, clean power supplies with low ripple voltage capability should be used. Switching power supplies can be used for this application, but beware of its higher ripple voltage and PSS frequency-dependent characteristics. It is also best to supply power to the AD7398/AD7399 from the system's analog supply voltages. Do not use the digital 5 V supply.

The reference input resistance is code dependent, exhibiting worst case 35 kΩ for AD7398 when the DAC is loaded with alternating codes 010101010101. Similarly, the reference input resistance is 40 kΩ for AD7399 when the DAC is loaded with 0101010101.

Downloaded from Arrow.com.

OPERATION WITH V_{REF} EQUAL TO THE SUPPLY

The AD7398/AD7399 are designed to approach the full output voltage swing from ground to V_{DD} or V_{SS}. The maximum output swing is achieved when the corresponding V_{REF} input pin is tied to the same power supply. This power supply should be low noise and low ripple, preferably operated by a suitable reference voltage source such as ADR292 or REF02. The output swing is limited by the internal buffer offset voltage and the output drive current capability of the output stage. Users should at least budget the V_{ZSE} offset voltage as the closest the output voltage can get to either supply voltage under a no load condition. Under a loaded output, degrade the headroom by a factor of 2 mV per 1 mA of load current. Also note that the internal op amp has an offset voltage so that the first eight codes of AD7398 may not respond at the supply voltage or at ground until the internal DAC voltage exceeds the offset voltage of the output buffers. Similarly, the first two codes of AD7399 should not be used.

POWER SUPPLY SEQUENCING

V_{DD}/V_{SS} of AD7398/AD7399 should be powered from the system analog supplies. The external reference input can be supplied from the same supply to avoid a possible latch-up when the reference is powered on prior to V_{DD}/V_{SS}, or powered off subsequent to V_{DD}/V_{SS}. If V_{DD}/V_{SS} and V_{REF} have separate power sources, ensure the power-up sequence is GND, V_{DD}, V_{SS}, V_{REF}/digital input/digital output. The reverse sequence applies to the power-down sequence. The order of V_{REF} and digital input/digital output is not important. In addition, V_{REF} pins of the unused DACs should be connected to GND or some other power sources to ensure a similar power-up/power-down sequence.

PROGRAMMABLE POWER SHUTDOWN

The two MSBs of the serial input register, SA and SD, are used to program various shutdown modes. If SA is set to Logic 1, all DACs are placed in shutdown mode. If SA = 0 and SD = 1, a corresponding DAC is shutdown addressed by Bit A0 and Bit A1 (see the Input Registers section).

WORST CASE ACCURACY

Assuming a perfect reference, the worst-case output voltage can be calculated from the following equation:

$$V_{OUT} = \frac{D}{2^N} \times (V_{REF} + V_{FSE}) + V_{ZSE} + INL \quad (3)$$

where:

D = decimal code loaded to DAC ranges $0 \le D \le 2^N - 1$.

N = number of bits.

V_{REF} = applied reference voltage.

V_{FSE} = full-scale error in volts.

V_{ZSE} = zero-scale error in volts.

INL = integral nonlinearity in volts. INL is 0 at full scale or zero scale.

SERIAL DATA INTERFACE

The AD7398/AD7399 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI-compatible serial data interface. Serial data of the AD7398 and AD7399 is clocked into the serial input register in a 16-bit and 14-bit data-word format, respectively. MSBs are loaded first. The Input Registers section defines the 16 data-word bits for AD7398 and the 14 data-word bits for the AD7399. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK, subject to the data setup and data hold time requirements specified in the Specifications section. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. For the AD7398, only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state, and extra data bits are ignored. For the AD7399, only the last 14 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state. Because most microcontrollers output serial data is in eight-bit bytes, two right-justified data bytes can be written to the AD7398 and AD7399. Keeping the $\overline{CS}$ line low between the first and second byte transfers results in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of Address Bit A1 and Address Bit A0. For the AD7398, Table 5, Table 6, the Input Registers section, Figure 3, and Figure 4 define the characteristics of the serial interface. For the AD7399, Table 5, Table 6, the Input Registers section, and Figure 4 (with a 14-bit exception) define the characteristics of the serial interface. Figure 27 and Figure 28 show the equivalent logic interface for the key digital control pins for AD7398 and AD7399.

An asynchronous $\overline{RS}$ provides hardware control reset to zero-code state over the preset function and DAC register loading. If this function is not needed, the $\overline{RS}$ pin can be tied to logic high.

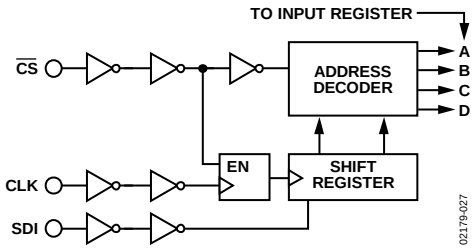

Figure 27. Equivalent Logic Interface

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POWER-ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the input and DAC registers to the zero-code state. The V_{DD} power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.2 V. The V_{SS} supply has no effect on the power-on reset performance. The DAC register data stays at zero until a valid serial register data load takes place.

ESD Protection Circuits

All logic input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD} as shown in Figure 28.

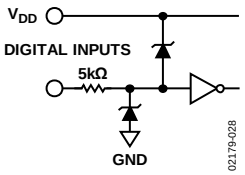

Figure 28. Equivalent ESD Protection Circuits

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7398/AD7399 is via a serial bus that uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD7398/AD7399 require a 16-bit/14-bit data word with data valid on the rising edge of CLK. The DAC update can be done automatically when all the data is clocked in, or it can be done under control of $\overline{\text{LDAC}}$.

ADSP-2101 to AD7398/AD7399 Interface

Figure 29 shows a serial interface between the AD7398/AD7399 and the ADSP-2101. The ADSP-2101 is set to operate in the serial port (SPORT) transmit alternate framing mode. The ADSP-2101 is programmed through the SPORT control register and should be configured as follows: Internal clock operation, active low framing, 16-bit-word length. For the AD7398, transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. For the AD7399, the first two bits are don't care as the AD7399 keeps the last 14 bits. Similarly, transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. Because of the edge-triggered difference, an inverter is required at the SCLKs between the DSP and the DAC.

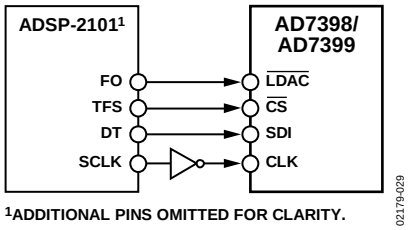

Figure 29. ADSP-2101 to AD7398/AD7399 Interface

68HC11/68L11 to AD7398/AD7399 Interface

Figure 30 shows a serial interface between the AD7398/AD7399 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the CLK of the DAC, and the MOSI output drives the serial data lines SDI. $\overline{\text{CS}}$ signal is driven from one of the port lines. The 68HC11/68L11 are configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

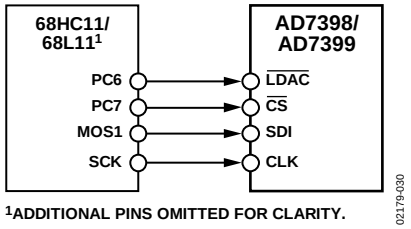

Figure 30. 68HC11/68L11 to AD7398/AD7399 Interface

MICROWIRE™ to AD7398/AD7399 Interface

Figure 31 shows an interface between the AD7398/AD7399 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the AD7398/AD7399 on the rising edge of the serial clock. No glue logic is required as the DAC clocks data into the input shift register on the rising edge.

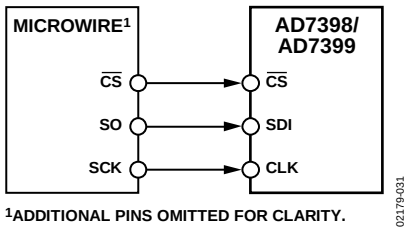

Figure 31. MICROWIRE to AD7398/AD7399 Interface

80C51/80L51 to AD7398/AD7399 Interface

A serial interface between the AD7398/AD7399 and the 80C51/80L51 microcontroller is shown in Figure 32. TxD of the microcontroller drives the CLK of the AD7398/AD7399, and RxD drives the serial data line of the DAC. P3.3 is a bit-programmable pin on the serial port that is used to drive $\overline{\text{CS}}$.

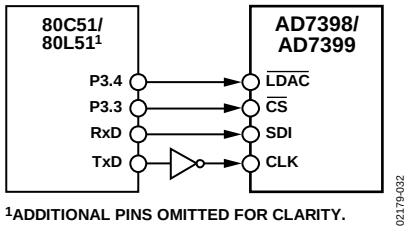

Figure 32. 80C51/80L51 to AD7398/AD7399 Interface

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Note that the 80C51/80L51 provide the LSB first, although the AD7398/AD7399 expect the MSB of the 16-bit/14-bit word first. Care should be taken to ensure the transmit routine takes this into account. This can usually be done with software by shifting out and accumulating the bits in the correct order before inputting to the DAC. In addition, 80C51 outputs two byte words/16 bits of data. Thus for AD7399, the first two bits, after rearrangement, should be don't care as they are dropped from the 14-bit word of the AD7399.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmit their data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the AD7399 requires a 14-bit word, P3.3 (or any one of the other programmable bits) is the $\overline{CS}$ input signal to the DAC; therefore P3.3 should be brought low at the beginning of the 16-bit write cycle 2 × 8 bit-words, and held low until the 16-bit 2 × 8 cycle is completed. After that, P3.3 is brought high again and the new data loads to the DAC. Again, the first two bits, after rearranging, should be don't care. $\overline{LDAC}$ on the AD7398/AD7399 can also be controlled by the 80C51/80L51 serial port output by using another bit-programmable pin, P3.4.

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APPLICATIONS INFORMATION

STAIRCASE WINDOWS COMPARATOR

Many applications need to determine whether voltage levels are within predetermined limits. Some requirements are for nonoverlapping windows and others for overlapping windows. Both circuit configurations are shown in Figure 33 and Figure 34, respectively.

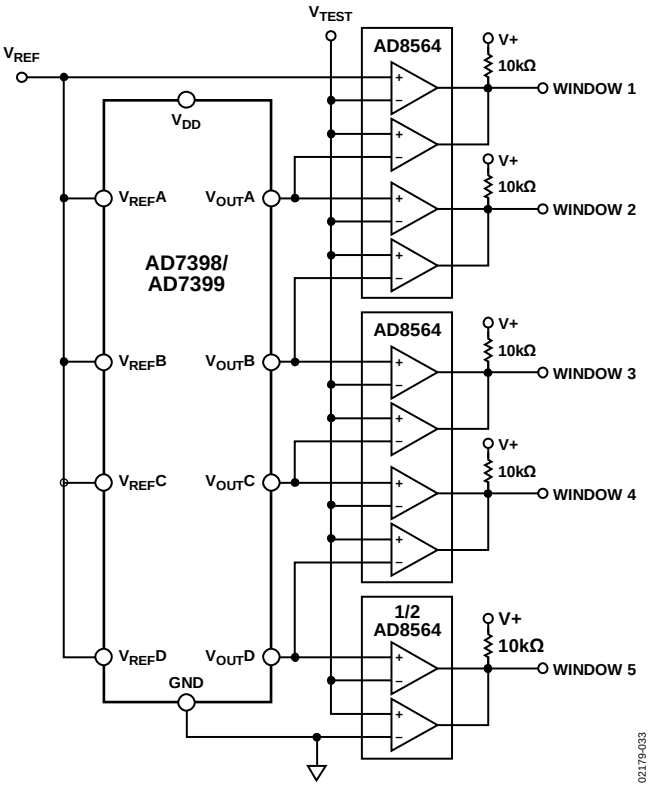

Figure 33. Nonoverlapping Windows Comparator

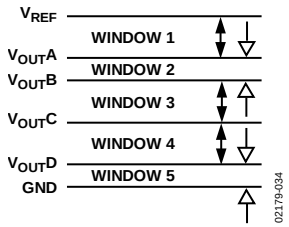

Figure 34. Nonoverlapping Windows Range

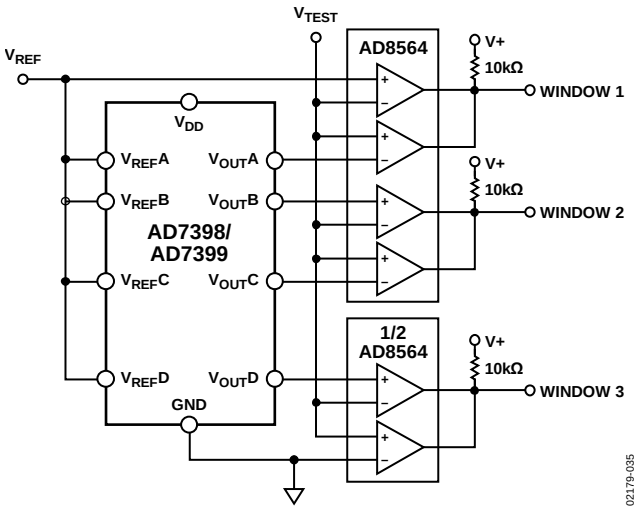

Figure 35. Overlapping Windows Comparator

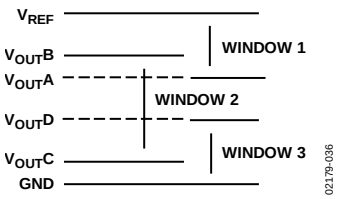

Figure 36. Overlapping Windows Range

The nonoverlapping circuit employs one AD7398/AD7399 and ten comparators to achieve five voltage windows. These windows range between V_{REF} and analog ground as shown in Figure 34. Similarly, the overlapping circuit employs six comparators to achieve three overlapping windows (see Figure 36).

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PROGRAMMABLE DAC REFERENCE VOLTAGE

With the flexibility of the AD7398/AD7399, one of the internal DACs can be used to control a common programmable V_{REFX} for the remainder of the DACs.

The circuit configuration is shown in Figure 37. The relationship of V_{REFX} to V_{REF} is dependent upon the digital code and the ratio of R1 and R2, and is given by

$$V_{REFX} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) - V_{REFX} \times \frac{D}{2^N} \times \frac{R2}{R1} \quad (4)$$

$$V_{REFX} = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \quad (5)$$

where:

D = decimal equivalent of input code.

N = number of bits.

V_{REF} = applied external reference.

V_{REFX} = reference voltage for DAC A to DAC D.

Table 7. V_{REFX} vs. R1 and R2

R1, R2	Digital Code	V_{REFX}
R1 = R2	0000 0000 0000	2 V_{REF}
R1 = R2	1000 0000 0000	1.3 V_{REF}
R1 = R2	1111 1111 1111	V_{REF}
R1 = 3R2	0000 0000 0000	4 V_{REF}
R1 = 3R2	1000 0000 0000	1.6 V_{REF}
R1 = 3R2	1111 1111 1111	V_{REF}

The accuracy of V_{REFX} is affected by the quality of R1 and R2. Therefore, tight tolerance, low tempco, thin film resistors should be used.

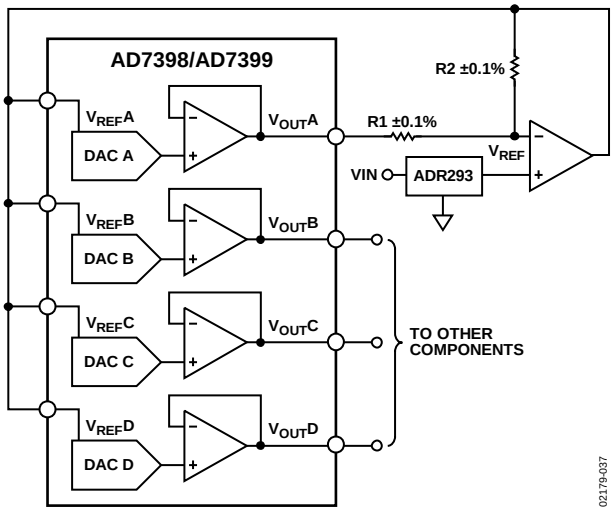

Figure 37. Programmable DAC Reference

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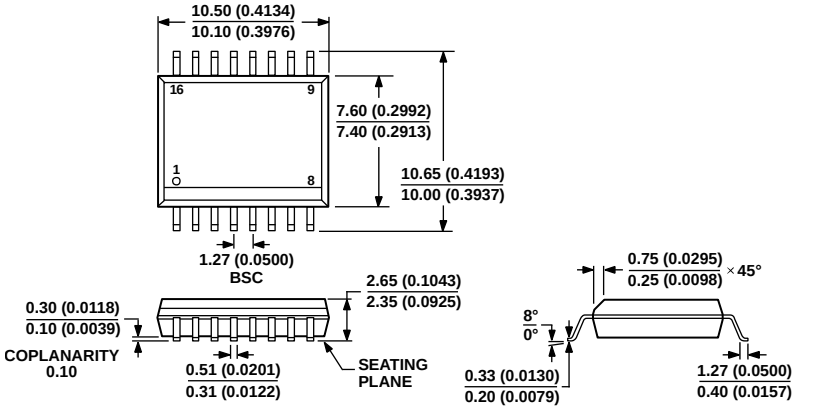
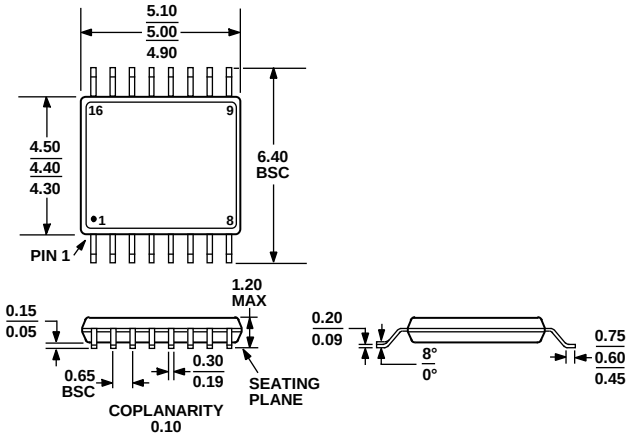
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 38. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 39. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

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ORDERING GUIDE

Model[1, 2]	Resolution (Bits)	Temperature Range	Package Description	Package Option	Ordering Quantity
AD7398BR	12	−40°C to +125°C	16-Lead SOIC_W	RW-16	47
AD7398BR-REEL	12	−40°C to +125°C	16-Lead SOIC_W	RW-16	1,000
AD7398BRZ	12	−40°C to +125°C	16-Lead SOIC_W	RW-16	47
AD7398BRZ-REEL	12	−40°C to +125°C	16-Lead SOIC_W	RW-16	1,000
AD7398BRU	12	−40°C to +125°C	16-Lead TSSOP	RU-16	96
AD7398BRU-REEL7	12	−40°C to +125°C	16-Lead TSSOP	RU-16	1,000
AD7398BRUZ	12	−40°C to +125°C	16-Lead TSSOP	RU-16	96
AD7398BRUZ-REEL7	12	−40°C to +125°C	16-Lead TSSOP	RU-16	1,000
AD7398WBRUZ-RL7	12	−40°C to +125°C	16-Lead TSSOP	RU-16	1,000
AD7399BR	10	−40°C to +125°C	16-Lead SOIC_W	RW-16	47
AD7399BR-REEL	10	−40°C to +125°C	16-Lead SOIC_W	RW-16	1,000
AD7399BRZ	10	−40°C to +125°C	16-Lead SOIC_W	RW-16	47
AD7399BRZ-REEL	10	−40°C to +125°C	16-Lead SOIC_W	RW-16	1,000
AD7399BRU	10	−40°C to +125°C	16-Lead TSSOP	RU-16	96
AD7399BRU-REEL7	10	−40°C to +125°C	16-Lead TSSOP	RU-16	1,000
AD7399BRUZ	10	−40°C to +125°C	16-Lead TSSOP	RU-16	96
AD7399BRUZ-REEL7	10	−40°C to +125°C	16-Lead TSSOP	RU-16	1,000

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

The AD7398 contains 3254 transistors. The die size measures 108 mils × 144 mils.

AUTOMOTIVE PRODUCTS

The AD7398WBRUZ-RL7 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

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