

# AD5245\* Product Page Quick Links

Last Content Update: 08/30/2016

---

## [Comparable Parts](#)

View a parametric search of comparable parts

## [Evaluation Kits](#)

- [AD5245 Evaluation Board](#)

## [Documentation](#)

### **Application Notes**

- [AN-1291: Digital Potentiometers: Frequently Asked Questions](#)
- [AN-686: Implementing an I2C® Reset](#)

### **Data Sheet**

- [AD5245: 256-Position I<sup>2</sup>C Compatible Digital Potentiometer Data Sheet](#)

### **User Guides**

- [UG-628: Evaluation Board for the AD5245 Digital Potentiometer](#)

## [Software and Systems Requirements](#)

- [Digital Potentiometer Linux Driver](#)

## [Design Resources](#)

- [AD5245 Material Declaration](#)
- [PCN-PDN Information](#)
- [Quality And Reliability](#)
- [Symbols and Footprints](#)

## [Discussions](#)

View all AD5245 EngineerZone Discussions

## [Sample and Buy](#)

Visit the product page to see pricing options

## [Technical Support](#)

Submit a technical question or find your regional support number

---

\* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

## TABLE OF CONTENTS

Features .....	1	Test Circuits.....	12
Applications.....	1	Theory of Operation .....	13
Functional Block Diagram .....	1	Programming the Variable Resistor.....	13
Pin Configuration.....	1	Programming the Potentiometer Divider .....	14
General Description.....	1	ESD Protection .....	14
Revision History .....	2	Terminal Voltage Operating Range .....	14
Electrical Characteristics .....	3	Power-Up Sequence .....	14
5 k $\Omega$ Version.....	3	Layout and Power Supply Bypassing .....	14
10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$ Versions .....	4	Constant Bias to Retain Resistance Setting.....	15
Timing Characteristics.....	5	Evaluation Board.....	15
5 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$ Versions.....	5	I <sup>2</sup> C Interface .....	16
Absolute Maximum Ratings.....	6	I <sup>2</sup> C-Compatible 2-Wire Serial Bus.....	16
ESD Caution.....	6	Outline Dimensions.....	19
Pin Configuration and Function Descriptions.....	7	Ordering Guide .....	19
Typical Performance Characteristics .....	8		
<b>REVISION HISTORY</b>			
<b>1/06—Rev. A to Rev. B</b>		Added Figure 37 .....	14
Changes to Table 3.....	5	Changes to Equation 4.....	14
Changes to Ordering Guide .....	19	Deleted Readback RDAC Value Section .....	14
<b>3/04—Rev. 0 to Rev. A</b>		Deleted Level Shifting for Bidirectional Interface Section .....	14
Updated Format.....	Universal	Moved ESD Protection Section to Page .....	14
Changes to Features.....	1	Changes to Figure 38 and Figure 39.....	14
Changes to Applications .....	1	Moved Terminal Voltage Operating Range Section to Page....	14
Changes to Figure 1.....	1	Changes to Figure 40.....	14
Changes to Electrical Characteristics—5 k $\Omega$ Version .....	3	Moved Power-Up Sequence Section to Page .....	14
Changes to Electrical Characteristics—10 k $\Omega$ , 50 k $\Omega$ , and 100 k $\Omega$ Versions .....	4	Moved Layout and Power Supply Bypassing Section to Page .	15
Changes to Timing Characteristics .....	5	Added Constant Bias to Retain Resistance Setting Section.....	15
Changes to Absolute Maximum Ratings .....	6	Added Figure 42 .....	15
Moved ESD Caution to Page .....	6	Added Evaluation Board Section .....	15
Changes to Pin Configuration and Function Descriptions .....	7	Added Figure 43 .....	15
Changes to Figures 22 and 23 .....	11	Moved I <sup>2</sup> C Interface Section to Page.....	16
Moved Figure 25 to Figure 26 .....	11	Changes to I <sup>2</sup> C Compatible 2-Wire Serial Bus Section .....	16
Moved Figure 26 to Figure 27 .....	11	Moved Table 5 and Table 6 to Page .....	17
Moved Figure 27 to Figure 25 .....	11	(Renumbered as Table 8 and Table 9)	
Deleted Figures 31 and 32 .....	12	Moved Figure 36, Figure 37, and Figure 38 to Page.....	17
Changes to Figure 32, Figure 33 and Figure 34 .....	12	(Renumbered as Figure 44, Figure 45, and Figure 46)	
Changes to Rheostat Operation Section.....	13	Moved Multiply Devices on One Bus Section to Page .....	18
Added Figure 35.....	13	Updated Ordering Guide .....	19
Changes to Equation 1 and Equation 2 .....	13	Updated Outline Dimensions.....	19
Changes to Table 6 and Table 7.....	13	Moved I <sup>2</sup> C Disclaimer to Page.....	20
		<b>5/03—Revision 0: Initial Version</b>	

# ELECTRICAL CHARACTERISTICS

## 5 kΩ VERSION

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	-4	±0.75	+4	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$	$T_A = 25^\circ\text{C}$	-30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	$V_{AB} = V_{DD}$ , wiper = no connect		45		ppm/°C
Wiper Resistance	$R_W$			50	120	Ω
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)</b>						
Differential Nonlinearity <sup>4</sup>	DNL		-1.5	±0.1	+1.5	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = 0x80		15		ppm/°C
Full-Scale Error	$V_{WFSE}$	Code = 0xFF	-6	-2.5	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = 0x00	0	2	6	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	$V_A, V_B, V_W$		GND		$V_{DD}$	V
Capacitance A, B <sup>6</sup>	$C_A, C_B$	$f = 1\text{ MHz}$ , measured to GND, code = 0x80		90		pF
Capacitance W <sup>6</sup>	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = 0x80		95		pF
Shutdown Supply Current <sup>7</sup>	$I_{A\_SD}$	$V_{DD} = 5.5\text{ V}$		0.01	1	μA
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		1		nA
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High	$V_{IH}$	$V_{DD} = 5\text{ V}$	2.4			V
Input Logic Low	$V_{IL}$	$V_{DD} = 5\text{ V}$			0.8	V
Input Logic High	$V_{IH}$	$V_{DD} = 3\text{ V}$	2.1			V
Input Logic Low	$V_{IL}$	$V_{DD} = 3\text{ V}$			0.6	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$			±1	μA
Input Capacitance <sup>6</sup>	$C_{IL}$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD\text{ RANGE}}$		2.7		5.5	V
Supply Current	$I_{DD}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$		3	8	μA
Power Dissipation <sup>8</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V}$ or $V_{IL} = 0\text{ V}$ , $V_{DD} = 5\text{ V}$			44	μW
Power Supply Sensitivity	PSS	$V_{DD} = +5\text{ V} \pm 10\%$ , code = midscale		±0.02	±0.05	%/%
<b>DYNAMIC CHARACTERISTICS<sup>6,9</sup></b>						
Bandwidth -3 dB	BW_5K	$R_{AB} = 5\text{ k}\Omega$ , code = 0x80		1.2		MHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1\text{ V rms}$ , $V_B = 0\text{ V}$ , $f = 1\text{ kHz}$		0.1		%
$V_W$ Settling Time	$t_s$	$V_A = 5\text{ V}$ , $V_B = 0\text{ V}$ , ±1 LSB error band		1		μs
Resistor Noise Voltage Density	$e_{N\_WB}$	$R_{WB} = 2.5\text{ k}\Omega$ , $R_S = 0$		6		nV/√Hz

<sup>1</sup> Typical specifications represent average readings at  $25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ .

<sup>2</sup> Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup>  $V_{AB} = V_{DD}$ , wiper ( $V_W$ ) = no connect.

<sup>4</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter.  $V_A = V_{DD}$  and  $V_B = 0\text{ V}$ . DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.

<sup>6</sup> Guaranteed by design and not subject to production test.

<sup>7</sup> Measured at the A terminal. The A terminal is open circuited in shutdown mode.

<sup>8</sup>  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD})$ . CMOS logic level inputs result in minimum power dissipation.

<sup>9</sup> All dynamic characteristics use  $V_{DD} = 5\text{ V}$ .

# AD5245

## 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

$V_{DD} = 5 V \pm 10\%$  or  $3 V \pm 10\%$ ,  $V_A = V_{DD}$ ,  $V_B = 0 V$ ,  $-40^\circ C < T_A < +125^\circ C$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS—RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = \text{no connect}$	-1	$\pm 0.1$	+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , $V_A = \text{no connect}$	-2	$\pm 0.25$	+2	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}$	$T_A = 25^\circ C$	-30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	$V_{AB} = V_{DD}$ , wiper = no connect		45		ppm/ $^\circ C$
Wiper Resistance	$R_W$	$V_{DD} = 5 V$		50	120	$\Omega$
<b>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)</b>						
Differential Nonlinearity <sup>4</sup>	DNL		-1	$\pm 0.1$	+1	LSB
Integral Nonlinearity <sup>4</sup>	INL		-1	$\pm 0.3$	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = 0x80		15		ppm/ $^\circ C$
Full-Scale Error	$V_{WFSE}$	Code = 0xFF	-3	-1	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = 0x00	0	1	3	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>5</sup>	$V_A, V_B, V_W$		GND		$V_{DD}$	V
Capacitance A, B <sup>6</sup>	$C_A, C_B$	$f = 1 \text{ MHz}$ , measured to GND, code = 0x80		90		pF
Capacitance W <sup>6</sup>	$C_W$	$f = 1 \text{ MHz}$ , measured to GND, code = 0x80		95		pF
Shutdown Supply Current	$I_{A\_SD}$	$V_{DD} = 5.5 V$		0.01	1	$\mu A$
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_{DD}/2$		1		nA
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Logic High	$V_{IH}$	$V_{DD} = 5 V$	2.4			V
Input Logic Low	$V_{IL}$	$V_{DD} = 5 V$			0.8	V
Input Logic High	$V_{IH}$	$V_{DD} = 3 V$	2.1			V
Input Logic Low	$V_{IL}$	$V_{DD} = 3 V$			0.6	V
Input Current	$I_{IL}$	$V_{IN} = 0 V$ or $5 V$			$\pm 1$	$\mu A$
Input Capacitance <sup>6</sup>	$C_{IL}$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD \text{ RANGE}}$		2.7		5.5	V
Supply Current	$I_{DD}$	$V_{IH} = 5 V$ or $V_{IL} = 0 V$		3	8	$\mu A$
Power Dissipation <sup>7</sup>	$P_{DISS}$	$V_{IH} = 5 V$ or $V_{IL} = 0 V$ , $V_{DD} = 5 V$			44	$\mu W$
Power Supply Sensitivity	PSS	$V_{DD} = 5 V \pm 10\%$ , code = midscale		$\pm 0.02$	$\pm 0.05$	%/%
<b>DYNAMIC CHARACTERISTICS<sup>6,8</sup></b>						
Bandwidth -3 dB	BW	$R_{AB} = 10 \text{ k}\Omega/50 \text{ k}\Omega/100 \text{ k}\Omega$ , code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1 V$ rms, $V_B = 0 V$ , $f = 1 \text{ kHz}$ , $R_{AB} = 10 \text{ k}\Omega$		0.1		%
$V_W$ Settling Time (10 kΩ/50 kΩ/100 kΩ)	$t_S$	$V_A = 5 V$ , $V_B = 0 V$ , $\pm 1$ LSB error band		2		$\mu s$
Resistor Noise Voltage Density	$e_{N\_WB}$	$R_{WB} = 5 \text{ k}\Omega$ , $R_S = 0$		9		nV/ $\sqrt{\text{Hz}}$

<sup>1</sup> Typical specifications represent average readings at  $25^\circ C$  and  $V_{DD} = 5 V$ .

<sup>2</sup> Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup>  $V_{AB} = V_{DD}$ , wiper ( $V_W$ ) = no connect.

<sup>4</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter.  $V_A = V_{DD}$  and  $V_B = 0 V$ .

DNL specification limits of  $\pm 1$  LSB maximum are guaranteed monotonic operating conditions.

<sup>5</sup> Resistor Terminals A, B, W have no limitations on polarity with respect to each other.

<sup>6</sup> Guaranteed by design and not subject to production test.

<sup>7</sup>  $P_{DISS}$  is calculated from ( $I_{DD} \times V_{DD}$ ). CMOS logic level inputs result in minimum power dissipation.

<sup>8</sup> All dynamic characteristics use  $V_{DD} = 5 V$ .

## TIMING CHARACTERISTICS

### 5 K $\Omega$ , 10 K $\Omega$ , 50 K $\Omega$ , 100 K $\Omega$ VERSIONS

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
I <sup>2</sup> C INTERFACE TIMING CHARACTERISTICS <sup>2,3,4</sup> (Specifications Apply to All Parts)						
SCL Clock Frequency	$f_{SCL}$				400	kHz
$t_{BUF}$ Bus Free Time Between STOP and START	$t_1$	After this period, the first clock pulse is generated.	1.3			$\mu\text{s}$
$t_{HD,STA}$ Hold Time (Repeated START)	$t_2$		0.6			$\mu\text{s}$
$t_{LOW}$ Low Period of SCL Clock	$t_3$		1.3			$\mu\text{s}$
$t_{HIGH}$ High Period of SCL Clock	$t_4$		0.6			$\mu\text{s}$
$t_{SU,STA}$ Setup Time for Repeated START Condition	$t_5$		0.6			$\mu\text{s}$
$t_{HD,DAT}$ Data Hold Time	$t_6$				0.9	$\mu\text{s}$
$t_{SU,DAT}$ Data Setup Time	$t_7$		100			ns
$t_F$ Fall Time of Both SDA and SCL Signals	$t_8$				300	ns
$t_R$ Rise Time of Both SDA and SCL Signals	$t_9$				300	ns
$t_{SU,STO}$ Setup Time for STOP Condition	$t_{10}$		0.6			$\mu\text{s}$

<sup>1</sup> Typical specifications represent average readings at 25°C and  $V_{DD} = 5\text{ V}$ .

<sup>2</sup> Guaranteed by design and not subject to production test.

<sup>3</sup> See timing diagram (Figure 44) for locations of measured values.

<sup>4</sup> Standard I<sup>2</sup>C mode operation guaranteed by design.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Value
$V_{DD}$ to GND	-0.3 V to +7 V
$V_A, V_B, V_W$ to GND	$V_{DD}$
Terminal Current, A to B, A to W, B to W <sup>1</sup>	
Pulsed	$\pm 20$ mA
Continuous	$\pm 5$ mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Maximum Junction Temperature ( $T_{JMAX}$ )	$150^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$245^\circ\text{C}$
Thermal Resistance <sup>2</sup> $\theta_{JA}$ : SOT-23-8	$230^\circ\text{C}/\text{W}$

<sup>1</sup> Maximum terminal current is bound by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Package power dissipation =  $(T_{JMAX} - T_A)/\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	W	W Terminal. $GND \leq V_W \leq V_{DD}$ .
2	V <sub>DD</sub>	Positive Power Supply.
3	GND	Digital Ground.
4	SCL	Serial Clock Input. Positive edge triggered. Pull-up resistor required.
5	SDA	Serial Data Input/Output. Pull-up resistor required.
6	AD0	Programmable Address Bit 0 for Two-Device Decoding.
7	B	B Terminal. $GND \leq V_B \leq V_{DD}$ .
8	A	A Terminal. $GND \leq V_A \leq V_{DD}$ .

TYPICAL PERFORMANCE CHARACTERISTICS

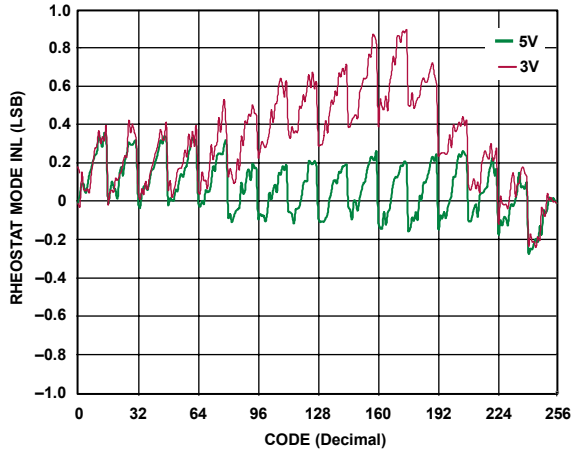


Figure 4. R-INL vs. Code vs. Supply Voltages

03436-003

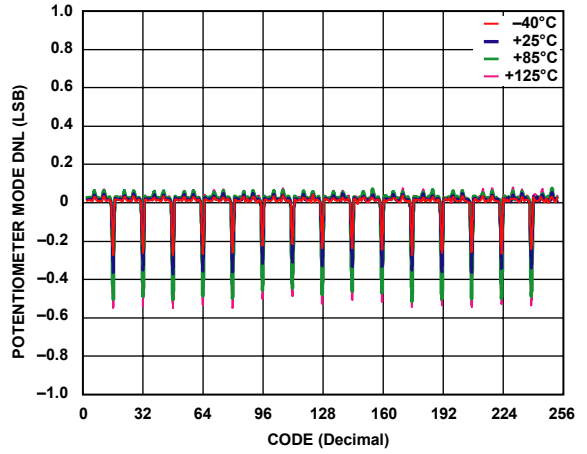


Figure 7. DNL vs. Code vs. Temperature,  $V_{DD} = 5 V$

03436-006

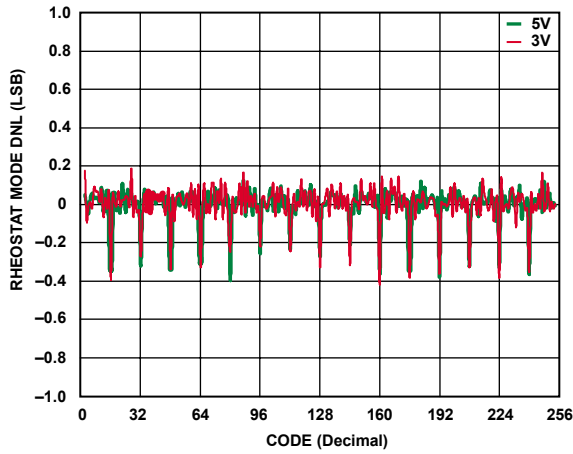


Figure 5. R-DNL vs. Code vs. Supply Voltages

03436-004

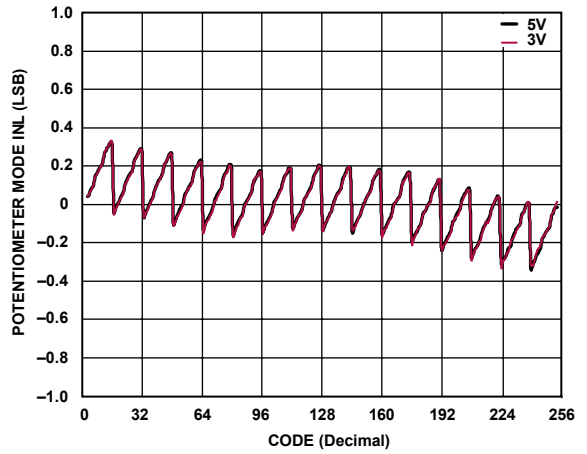


Figure 8. INL vs. Code vs. Supply Voltages

03436-007

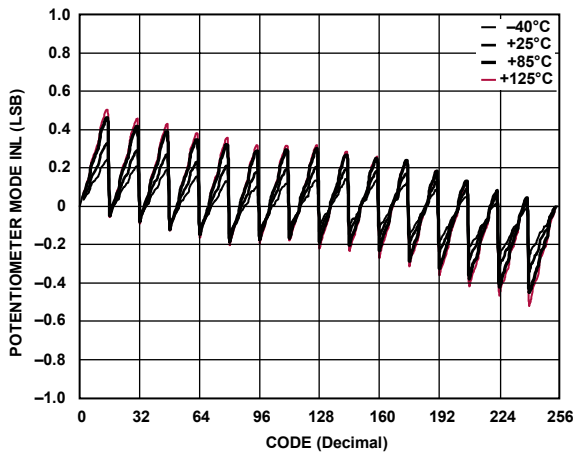


Figure 6. INL vs. Code vs. Temperature,  $V_{DD} = 5 V$

03436-005

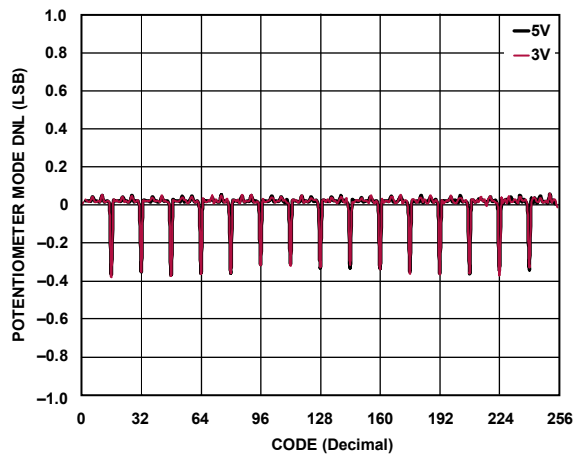


Figure 9. DNL vs. Code vs. Supply Voltages

03436-008





Figure 10. R-INL vs. Code vs. Temperature,  $V_{DD} = 5\text{ V}$

03436-009



Figure 13. Zero-Scale Error vs. Temperature

03436-012



Figure 11. R-DNL vs. Code vs. Temperature,  $V_{DD} = 5\text{ V}$

03436-010

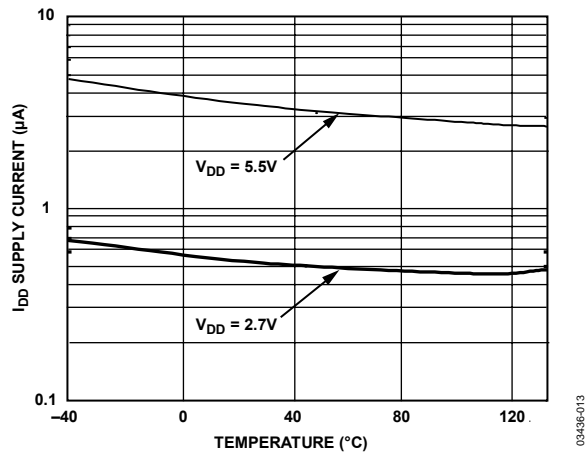


Figure 14. Supply Current vs. Temperature

03436-013



Figure 12. Full-Scale Error vs. Temperature

03436-011



Figure 15. Shutdown Current vs. Temperature

03436-014

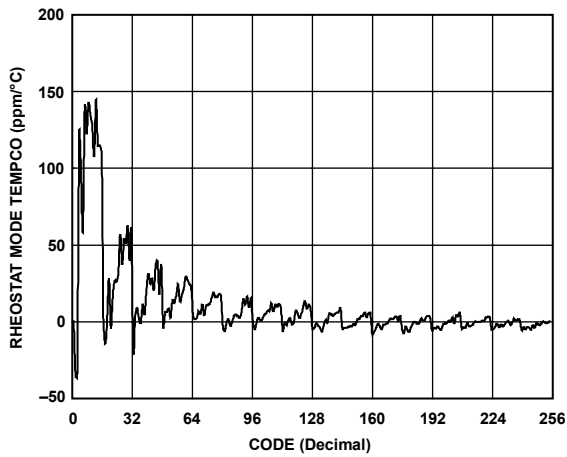


Figure 16. Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

03436-015



Figure 19. Gain vs. Frequency vs. Code,  $R_{AB} = 10\text{ k}\Omega$

03436-018

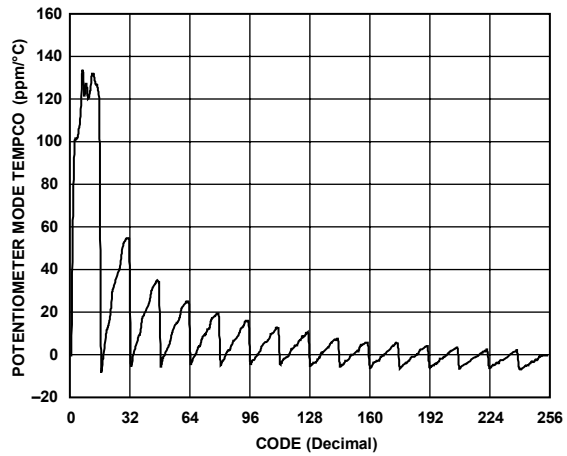


Figure 17. Potentiometer Mode Tempco  $\Delta V_{WB}/\Delta T$  vs. Code

03436-016



Figure 20. Gain vs. Frequency vs. Code,  $R_{AB} = 50\text{ k}\Omega$

03436-019

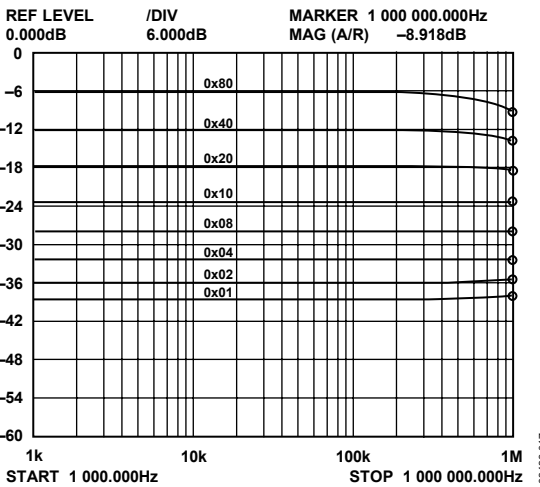


Figure 18. Gain vs. Frequency vs. Code,  $R_{AB} = 5\text{ k}\Omega$

03436-017



Figure 21. Gain vs. Frequency vs. Code,  $R_{AB} = 100\text{ k}\Omega$

03436-020



Figure 22. -3 dB Bandwidth @ Code = 0x80

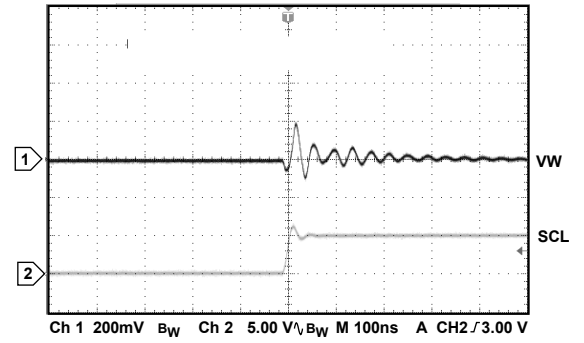


Figure 25. Large Signal Settling Time, Code 0xFF ≥ 0x00



Figure 23. PSRR vs. Frequency



Figure 26. Digital Feedthrough



Figure 24.  $I_{DD}$  vs. Frequency



Figure 27. Midscale Glitch, Code 0x80 ≥ 0x7F

## TEST CIRCUITS

Figure 28 to Figure 34 illustrate the test circuits that define the test conditions used in the product specification tables (Table 1 through Table 3).

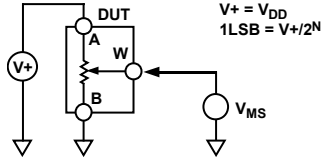


Figure 28. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)



Figure 32. Test Circuit for Gain vs. Frequency

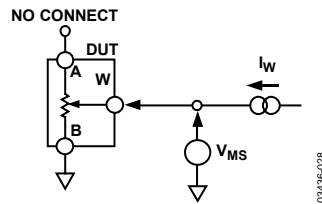


Figure 29. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)



Figure 33. Test Circuit for Incremental On Resistance

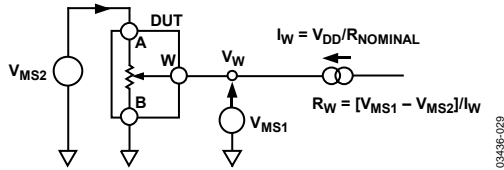


Figure 30. Test Circuit for Wiper Resistance

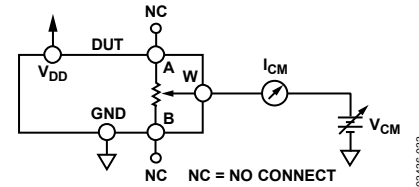


Figure 34. Test Circuit for Common-Mode Leakage Current

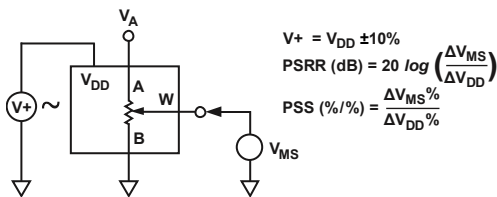


Figure 31. Test Circuit for Power Supply Sensitivity (PSS, PSSH)

## THEORY OF OPERATION

The AD5245 is a 256-position digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

### PROGRAMMING THE VARIABLE RESISTOR

#### Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance ( $R_{AB}$ ) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

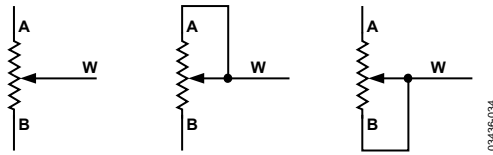


Figure 35. Rheostat Mode Configuration

Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for Data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω ( $2 \times 50 \Omega$ ) resistance between Terminals W and B. The second connection is the first tap point, which corresponds to 139 Ω ( $R_{WB} = R_{AB}/256 + 2 \times R_W = 39 \Omega + 2 \times 50 \Omega$ ) for Data 0x01. The third connection is the next tap point, representing 178 Ω ( $2 \times 39 \Omega + 2 \times 50 \Omega$ ) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω ( $R_{AB} + 2 \times R_W$ ).

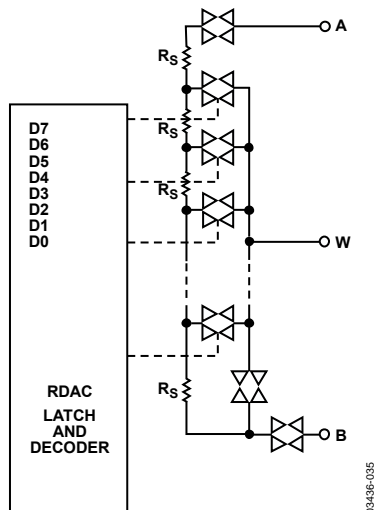


Figure 36. AD5245 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

$D$  is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.

$R_{AB}$  is the end-to-end resistance.

$R_W$  is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if  $R_{AB} = 10 \text{ k}\Omega$  and the A terminal is open circuited, then the following output resistance  $R_{WB}$  is set for the indicated RDAC latch codes.

Table 6. Codes and Corresponding  $R_{WB}$  Resistance

D (Dec.)	$R_{WB}$ (Ω)	Output State
255	9,961	Full Scale ( $R_{AB} - 1 \text{ LSB} + R_W$ )
128	5,060	Midscale
1	139	1 LSB
0	100	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a digitally controlled complementary resistance,  $R_{WA}$ . When these terminals are used, the B terminal can be opened. Setting the resistance value for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

For  $R_{AB} = 10 \text{ k}\Omega$  and the B terminal open circuited, the following output resistance  $R_{WA}$  is set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding  $R_{WA}$  Resistance

D (Dec.)	$R_{WA}$ (Ω)	Output State
255	139	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

Typical device-to-device matching is process lot dependent and can vary by up to  $\pm 30\%$ . Because the resistance element is processed in thin film technology, the change in  $R_{AB}$  with temperature has a very low 45 ppm/°C temperature coefficient.

## PROGRAMMING THE POTENTIOMETER DIVIDER

### Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A to B. Unlike the polarity of  $V_{DD}$  to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

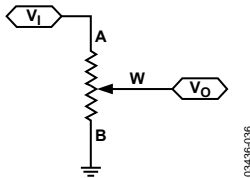


Figure 37. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, then connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at  $V_W$  with respect to ground for any valid input voltage applied to Terminals A and B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256-D}{256} V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance,  $V_W$ , is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors,  $R_{WA}$  and  $R_{WB}$ , not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

## ESD PROTECTION

All digital inputs are protected with a series of input resistors and parallel Zener ESD structures, shown in Figure 38 and Figure 39. This applies to the digital input pins SDA, SCL, and AD0.

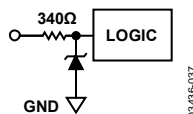


Figure 38. ESD Protection of Digital Pins

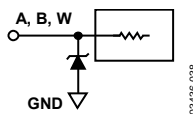


Figure 39. ESD Protection of Resistor Terminals

## TERMINAL VOLTAGE OPERATING RANGE

The AD5245  $V_{DD}$  and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminals A, B, and W that exceed  $V_{DD}$  or GND are clamped by the internal forward-biased diodes (see Figure 40).



Figure 40. Maximum Terminal Voltages Set by  $V_{DD}$  and GND

## POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminals A, B, and W (see Figure 40), it is important to power  $V_{DD}$  and GND before applying any voltage to Terminals A, B, and W; otherwise, the diode is forward biased such that  $V_{DD}$  is powered unintentionally and can affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND,  $V_{DD}$ , digital inputs, and then  $V_A$ ,  $V_B$ , and  $V_W$ . The relative order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and the digital inputs is not important as long as they are powered after  $V_{DD}$  and GND.

## LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disk or chip ceramic capacitors of 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ . Low ESR 1  $\mu\text{F}$  to 10  $\mu\text{F}$  tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 41). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.



Figure 41. Power Supply Bypassing

## CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost for the EEMEM, the AD5245 can be considered a low cost alternative by maintaining a constant bias to retain the wiper setting. The AD5245 is designed specifically with low power in mind, which allows low power consumption even in battery-operated systems. Figure 42 demonstrates the power consumption from a 3.4 V, 450 mA-hr Li-Ion cell phone battery that is connected to the AD5245. The measurement over time shows that the device draws approximately 1.3  $\mu$ A and consumes negligible power. Over a course of 30 days, the battery is depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

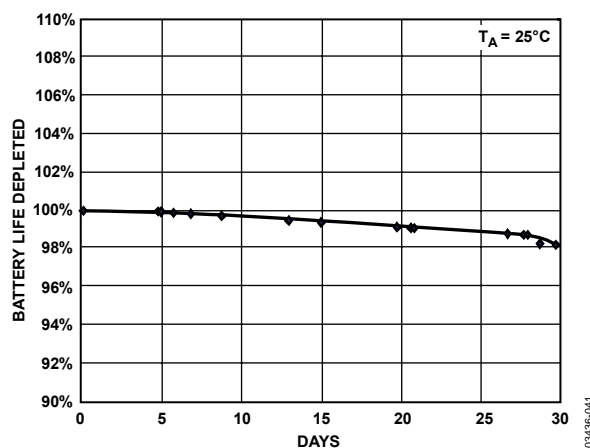


Figure 42. Battery Operating Life Depletion

This demonstrates that constantly biasing the potentiometer can be a practical approach. Most portable devices do not require the removal of batteries for charging.

Although the resistance setting of the AD5245 is lost when the battery needs replacement, such events occur rather infrequently so that this inconvenience is justified by the lower cost and smaller size offered by the AD5245. If total power is lost, then the user should be provided with a means to adjust the setting accordingly.

## EVALUATION BOARD

An evaluation board, along with all necessary software, is available to program the AD5245 from any PC running Windows® 98/2000/XP. The graphical user interface, as shown in Figure 43, is straightforward and easy to use. More detailed information is available in the user manual, which is provided with the board.

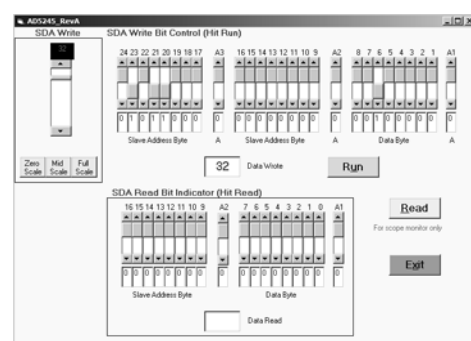


Figure 43. AD5245 Evaluation Board Software

The AD5245 starts at midscale upon power-up. To increment or decrement the resistance, the user can simply move the scroll-bars on the left. To write a specific value, the user should use the bit pattern in the upper screen and click the **Run** button. The format of writing data to the device is shown in Table 8. To read the data from the device, the user can simply click the **Read** button. The format of the read bits is shown in Table 9.

## I<sup>2</sup>C INTERFACE

### I<sup>2</sup>C-COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I<sup>2</sup>C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 45). The next byte is the slave address byte, which consists of the 7-bit slave address followed by an  $\overline{R/W}$  bit (this bit determines whether data is read from or written to the slave device). The AD5245 has one configurable address bit, AD0 (see Table 8).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the  $\overline{R/W}$  bit is high, the master reads from the slave device. On the other hand, if the  $\overline{R/W}$  bit is low, the master writes to the slave device.

2. In write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is a don't care.

The second MSB, RS, is the midscale reset. A logic high on this bit moves the wiper to the center tap, where  $R_{WA} = R_{WB}$ . This feature effectively overwrites the contents of the register; therefore, when taken out of reset mode, the RDAC remains at midscale.

The third MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0  $\Omega$  in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. Also during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

The remainder of the bits in the instruction byte are don't cares (see Table 8).

3. After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 45).
4. In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with write mode, in which eight data bits are followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 46).
5. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10<sup>th</sup> clock pulse to establish a STOP condition (see Figure 45). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10<sup>th</sup> clock pulse, which goes high to establish a STOP condition (see Figure 46).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output updates on each successive byte. If different instructions are needed, then the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.



**Table 8. Write Mode**

<b>S</b>	0	1	0	1	1	0	<b>AD0</b>	<b><math>\overline{W}</math></b>	<b>A</b>	<b>X</b>	<b>RS</b>	<b>SD</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>A</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>A</b>	<b>P</b>
Slave Address Byte								Instruction Byte								Data Byte												

**Table 9. Read Mode**

<b>S</b>	0	1	0	1	1	0	<b>AD0</b>	<b>R</b>	<b>A</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>A</b>	<b>P</b>
Slave Address Byte										Data Byte									

S = START condition  
P = STOP condition  
A = Acknowledge  
X = Don't care  
 $\overline{W}$  = Write

R = Read  
RS = Reset wiper to midscale 0x80  
SD = Shutdown connects wiper to B terminal and open circuits A terminal, but does not change contents of wiper register  
D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits

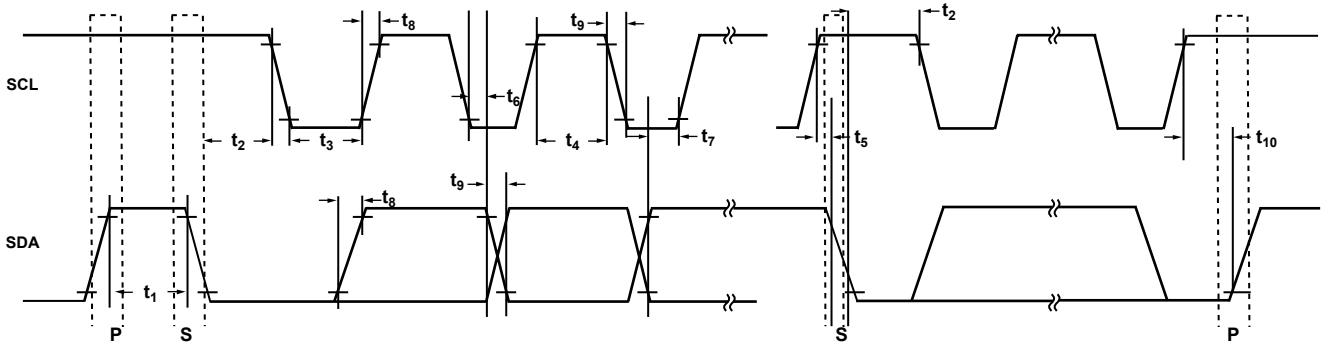


Figure 44. I<sup>2</sup>C Interface Detailed Timing Diagram



Figure 45. Writing to the RDAC Register



Figure 46. Reading Data from a Previously Selected RDAC Register in Write Mode

# AD5245

## Multiple Devices on One Bus

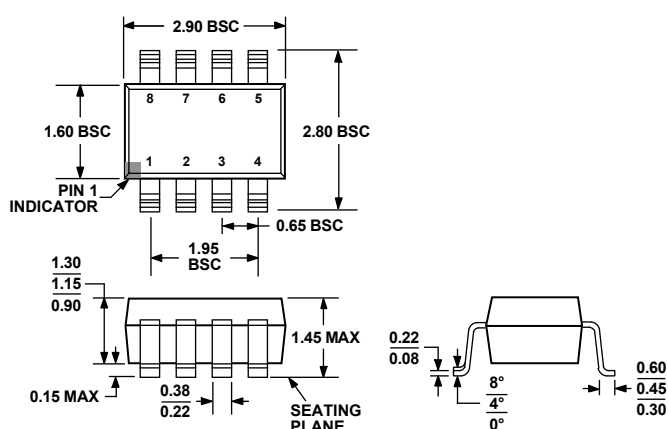
Figure 47 shows two AD5245 devices on the same serial bus. Each has a different slave address because the states of their AD0 pins are different. This allows the RDAC within each device to be written to or read from independently. The master device's output bus line drivers are open-drain pull-downs in a fully I<sup>2</sup>C-compatible interface.



Figure 47. Multiple AD5245 Devices on One I<sup>2</sup>C Bus

03498-046

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 48. 8-Lead Small Outline Transistor Package [SOT-23]  
(RJ-8)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	R <sub>AB</sub> (Ω)	Ordering Quantity
AD5245BRJ5-R2	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0G	5 k	250
AD5245BRJ5-RL7	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0G	5 k	3,000
AD5245BRJZ5-R2 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0G	5 k	250
AD5245BRJZ5-RL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0G	5 k	3,000
AD5245BRJ10-R2	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0H	10 k	250
AD5245BRJ10-RL7	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0H	10 k	3,000
AD5245BRJZ10-R2 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0H	10 k	250
AD5245BRJZ10-RL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0H	10 k	3,000
AD5245BRJ50-R2	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0J	50 k	250
AD5245BRJ50-RL7	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0J	50 k	3,000
AD5245BRJZ50-R2 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0J	50 k	250
AD5245BRJZ50-RL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0J	50 k	3,000
AD5245BRJ100-R2	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0K	100 k	250
AD5245BRJ100-RL7	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0K	100 k	3,000
AD5245BRJZ100-R2 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0K	100 k	250
AD5245BRJZ100-RL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	D0K	100 k	3,000
AD5245EVAL <sup>2</sup>		Evaluation Board				

<sup>1</sup> Z = Pb-free part.

<sup>2</sup> The evaluation board is shipped with the 10 kΩ R<sub>AB</sub> resistor option; however, the board is compatible with all available resistor value options.

**AD5245**

## NOTES

Purchase of licensed I<sup>2</sup>C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

©2006 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.  
C03436-0-1/06(B)



[www.analog.com](http://www.analog.com)

Rev. B | Page 20 of 20