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5/12—Rev. B to Rev. C

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Removed Evaluation Board Section 15
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8/09—Rev. A to Rev. B

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7/05—Rev. 0 to Rev. A

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9/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

V_{DD} = 5 V ± 10% or 3 V ± 10%; $V_A = +V_{DD}$; −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}	−4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	Wiper = no connect		45		ppm/°C
R_{WB}	R_{WB}	Code = 0x00, V_{DD} = 5 V		75	150	Ω
		Code = 0x00, V_{DD} = 2.7 V		150	400	Ω
RESISTOR TERMINALS						
Voltage Range[4]	$V_{B, W}$		GND		V_{DD}	V
Capacitance[5] B	C_B	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance[5] W	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	I_{CM}			1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		3	7	µA
		V_{DD} = 5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		2.5	5.2	µA
		V_{DD} = 3.3 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		0.9	2	µA
Power Dissipation[6]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	µW
Power Supply Sensitivity	PSSR	V_{DD} = +5 V ± 10%, code = midscale		±0.01	±0.025	%/%
DYNAMIC CHARACTERISTICS[5, 7]						
Bandwidth −3 dB	BW_5K	R_{AB} = 5 kΩ, code = 0x40		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = 5 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, R_S = 0 Ω		6		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] Code = 0x7F.
[4] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.
[5] Guaranteed by design; not subject to production test.
[6] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[7] V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; –40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	Wiper = no connect		45		ppm/°C
R_{WB}	R_{WB}	Code=0x00, V_{DD} = 5 V		75	150	Ω
		Code=0x00, V_{DD} = 2.7 V		150	400	Ω
RESISTOR TERMINALS						
Voltage Range[4]	$V_{B, W}$		GND		V_{DD}	V
Capacitance[5] B	C_B	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance[5] W	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	I_{CM}			1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		3	7	µA
		V_{DD} = 5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		2.5	5.2	µA
		V_{DD} = 3.3 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		0.9	2	µA
Power Dissipation[6]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	µW
Power Supply Sensitivity	PSSR	V_{DD} = +5 V ± 10%, code = midscale		±0.01	±0.02	%/%
DYNAMIC CHARACTERISTICS[5, 7]						
Bandwidth –3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, code = 0x40		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] Code = 0x7F.
[4] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.
[5] Guaranteed by design; not subject to production test.
[6] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[7] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[2, 3, 4]						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time Between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design; not subject to production test.
[3] See timing diagrams (Figure 26, Figure 27, and Figure 28) for locations of measured values.
[4] Specifications apply to all parts.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_W to GND	V_{DD}
Terminal Current, A–B, A–W, B–W	
Pulsed[1]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2] θ_{JA}: SC70-6	340°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

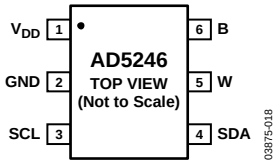

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply.
2	GND	Digital Ground.
3	SCL	Serial Clock Input. Positive edge triggered.
4	SDA	Serial Data Input/Output.
5	W	W Terminal.
6	B	B Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

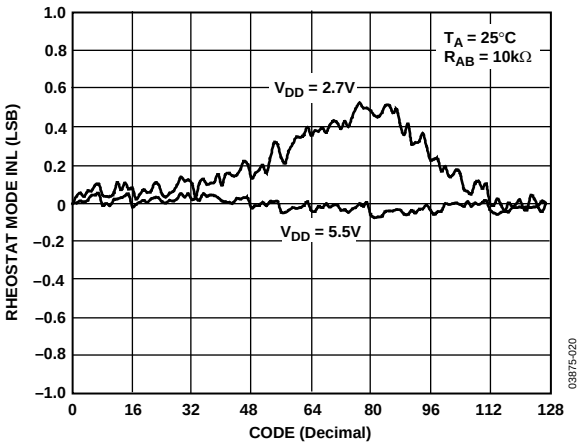

Figure 3. R-INL vs. Code vs. Supply Voltages

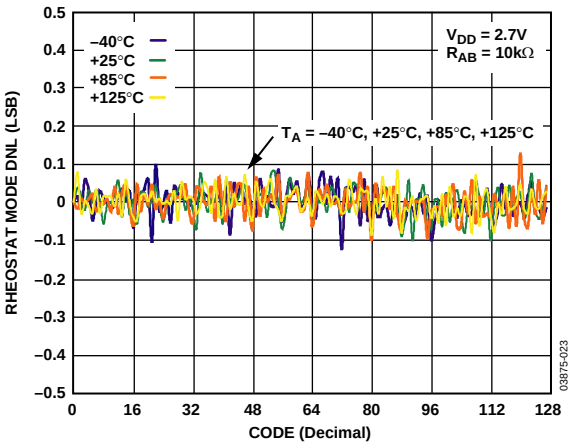

Figure 6. R-DNL vs. Code vs. Temperature

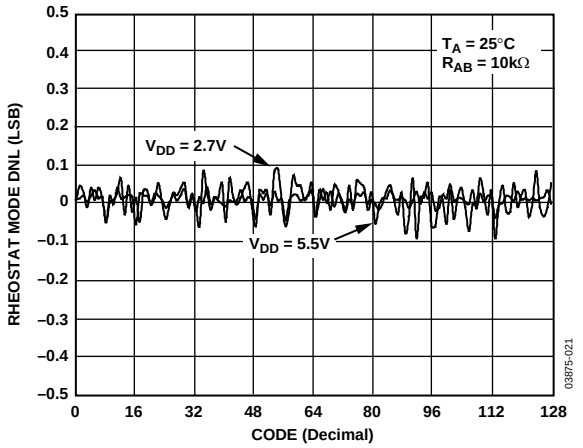

Figure 4. R-DNL vs. Code vs. Supply Voltages

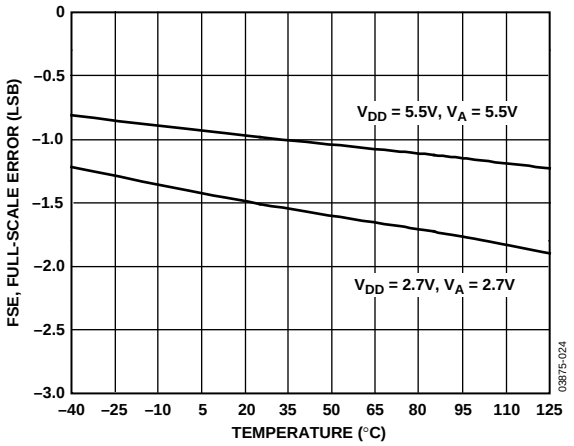

Figure 7. Full-Scale Error vs. Temperature

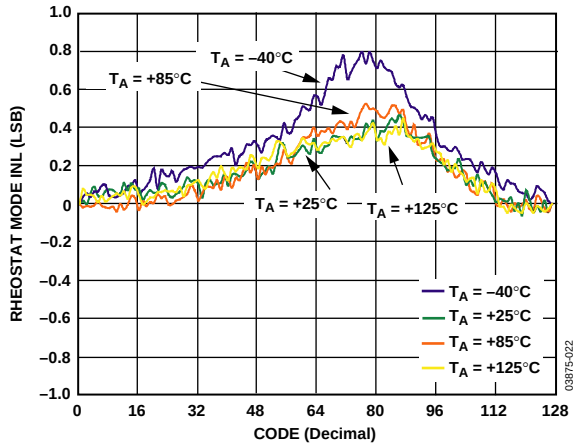

Figure 5. R-INL vs. Code vs. Temperature

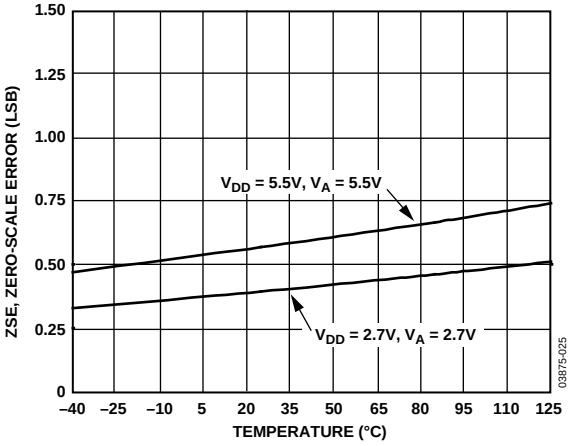

Figure 8. Zero-Scale Error vs. Temperature

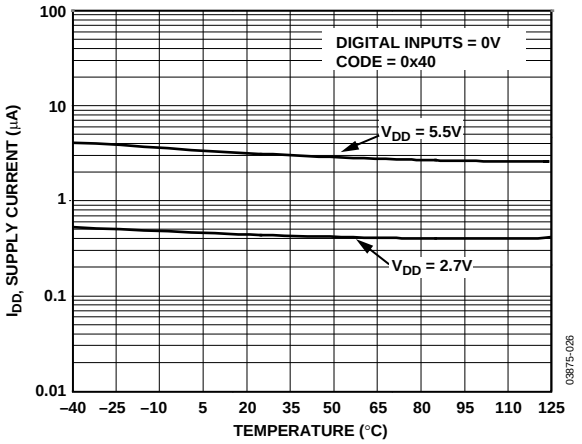

Figure 9. Supply Current vs. Temperature

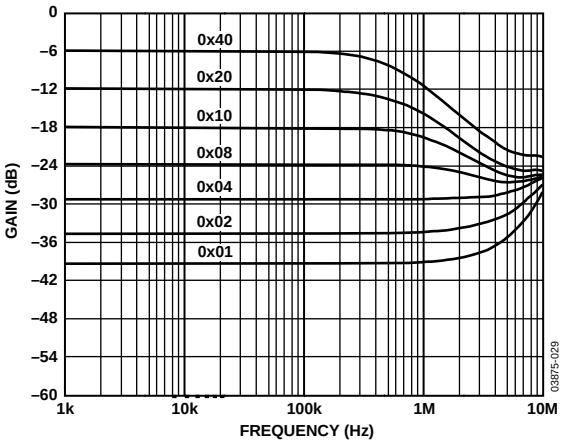

Figure 12. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

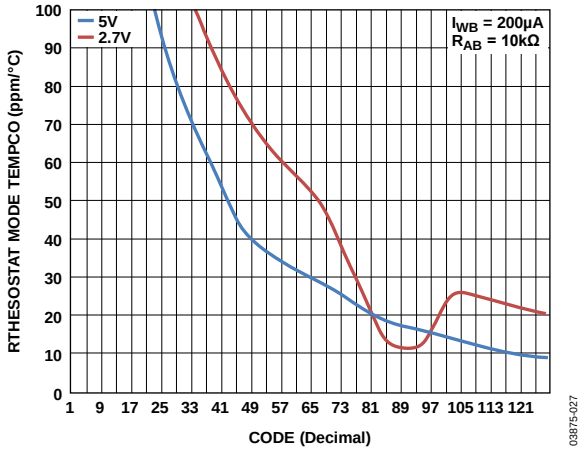

Figure 10. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

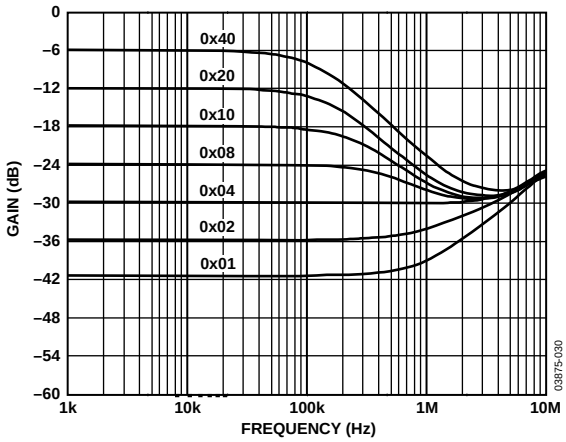

Figure 13. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

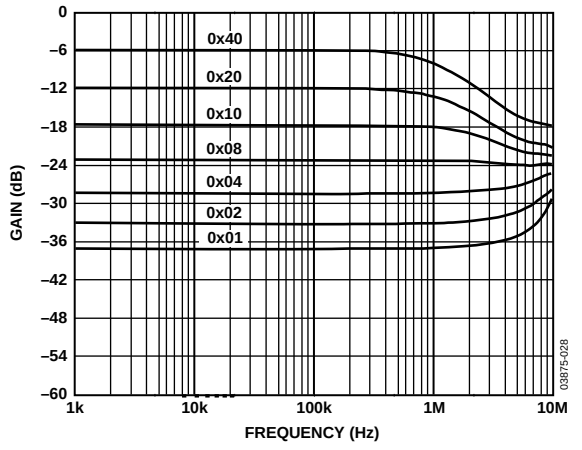

Figure 11. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

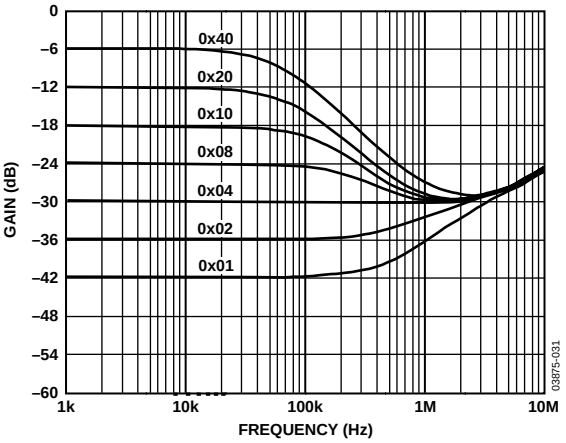

Figure 14. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

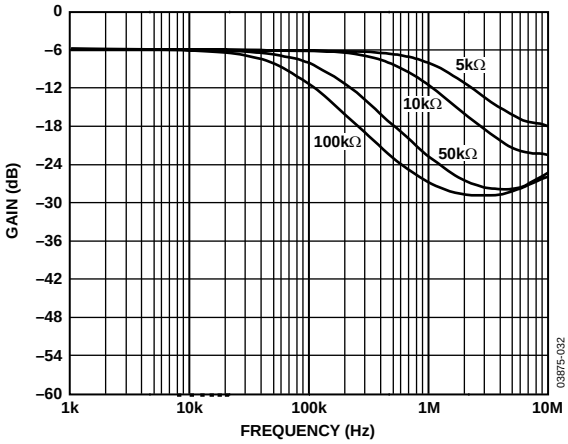

Figure 15. –3 dB Bandwidth @ Code = 0x80

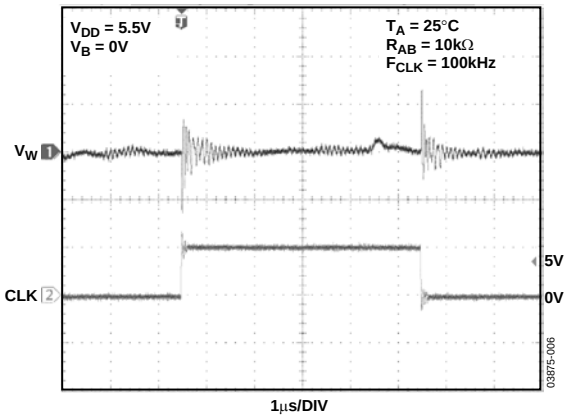

Figure 18. Digital Feedthrough

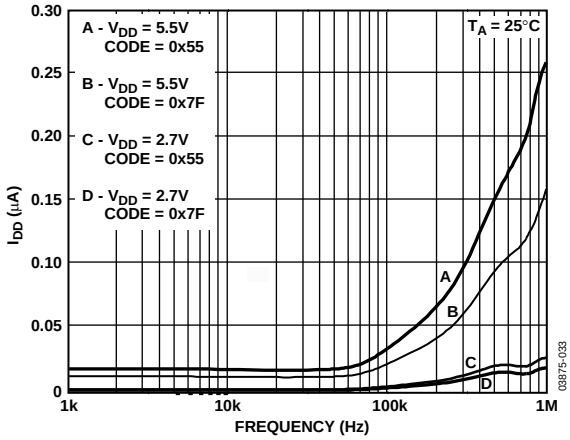

Figure 16. I_{DD} vs. Frequency

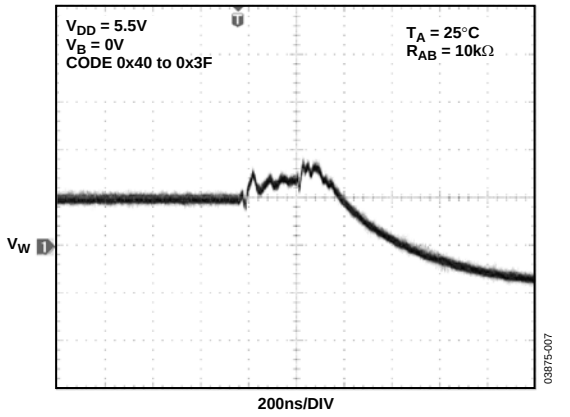

Figure 19. Midscale Glitch, Code 0x40 to 0x3F

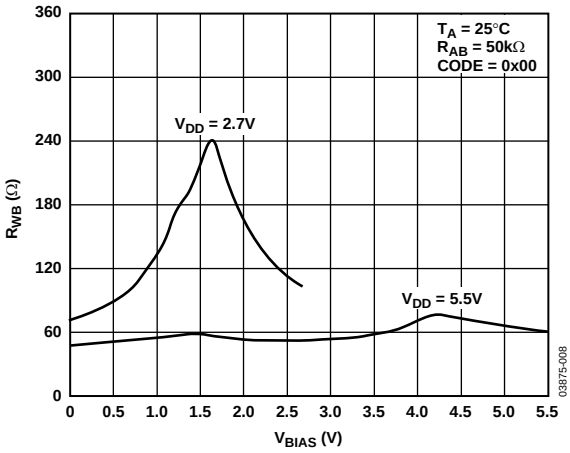

Figure 17. R_{WB} vs. V_{BIAS} vs. V_{DD}

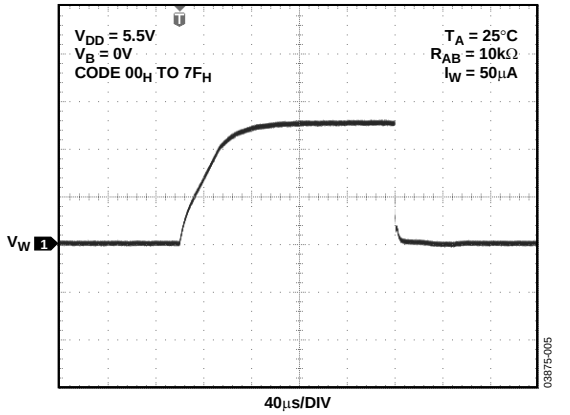

Figure 20. Large Signal Settling Time

TEST CIRCUITS

Figure 21 to Figure 25 define the test conditions used in the product Specification tables.

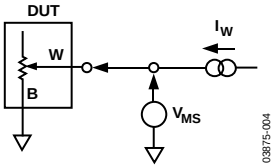

Figure 21. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

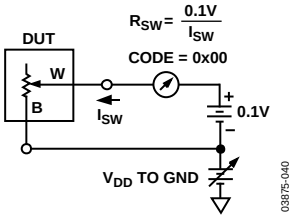

Figure 24. Test Circuit for Incremental On Resistance

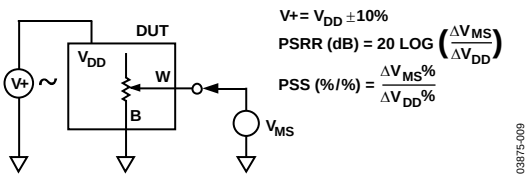

Figure 22. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

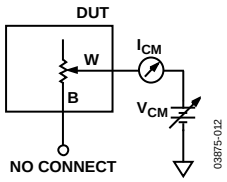

Figure 25. Test Circuit for Common-Mode Leakage Current

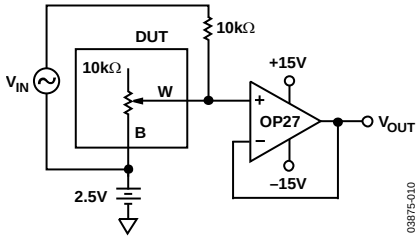

Figure 23. Test Circuit for Gain vs. Frequency

I²C INTERFACE

Table 6. Write Mode

S	0	1	0	1	1	1	0	$\overline{W}$	A	X	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

Table 7. Read Mode

S	0	1	0	1	1	1	0	R	A	0	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

S = Start Condition.

P = Stop Condition.

A = Acknowledge.

X = Don't Care.

$\overline{W}$ = Write.

R = Read.

D6, D5, D4, D3, D2, D1, D0 = Data Bits.

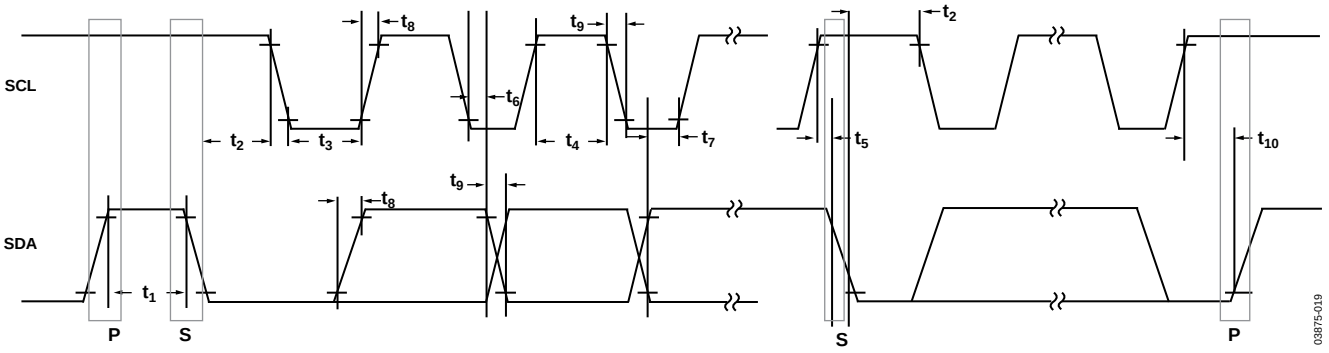

Figure 26. I²C Interface, Detailed Timing Diagram

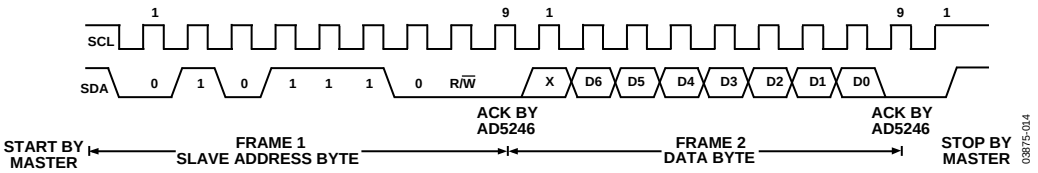

Figure 27. Writing to the RDAC Register

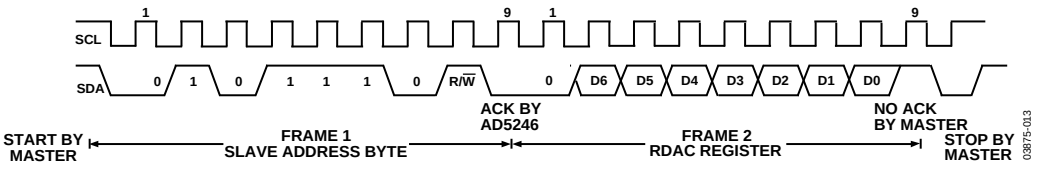

Figure 28. Reading from the RDAC Register

OPERATION

The AD5246 is a 128-position, digitally controlled variable resistor (VR) device.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value, that is, 10 kΩ = 10, 50 kΩ = 50. The nominal resistance (R_{AB}) of the VR has 128 contact points accessed by the wiper terminal. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible settings.

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 7-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of each internal switch.

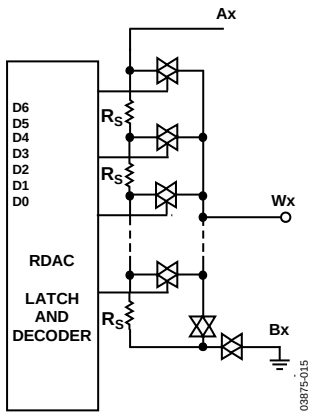

Figure 29. AD5246 Equivalent RDAC Circuit

Note that in the zero-scale condition, there is a relatively small finite wiper resistance. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. Since the resistance element is processed in thin-film technology, the temperature coefficient of R_{AB} is only 45 ppm/°C.

I²C COMPATIBLE 2-WIRE SERIAL BUS

The first byte of the AD5246 is a slave address byte (see Table 6 and Table 7). It has a 7-bit slave address and an R/$\overline{W}$ bit. The seven MSBs of the slave address are 0101110 followed by 0 for a write command or 1 to place the device in read mode.

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 27). The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. Conversely, if the R/$\overline{W}$ bit is low, the master writes to the slave device.

2. In write mode, after acknowledgement of the slave address byte, the next byte is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Table 6).

3. In read mode, after acknowledgment of the slave address byte, data is received over the serial bus in sequences of nine clock pulses (a slight difference from the write mode where eight data bits are followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 28).

4. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 27). In read mode, the master issues a No Acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, which goes high to establish a STOP condition (see Figure 28).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing the part only once. For example, after the RDAC has acknowledged its slave address in write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address and data byte. Similarly, a repeated read function of the RDAC is also allowed.

LEVEL SHIFTING FOR BIDIRECTIONAL INTERFACE

While most legacy systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 1.8 V E²PROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E²PROM. Figure 30 shows one of the implementations. M1 and M2 can be any N channel signal FETs, or if V_{DD} falls below 2.5 V, M1 and M2 can be low threshold FETs such as the FDV301N.

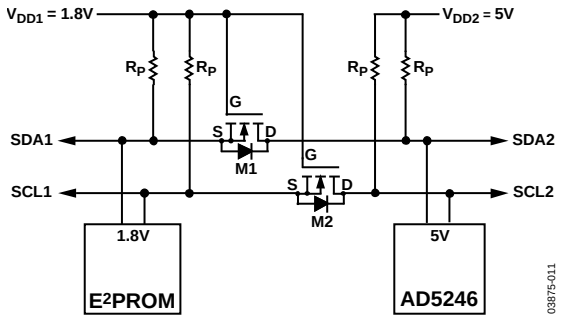

Figure 30. Level Shifting for Operation at Different Potentials

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 31. This applies to the digital input pins SDA and SCL.

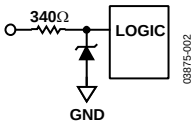

Figure 31. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

The AD5246 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal B and Terminal W that exceed V_{DD} or GND are clamped by the internal forward biased diodes (see Figure 32).

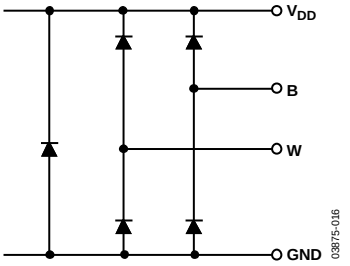

Figure 32. Maximum Terminal Voltages Set by V_{DD} and GND

MAXIMUM OPERATING CURRENT

At low code values, the user should be aware that due to low resistance values, the current through the RDAC may exceed the 5 mA limit. In Figure 33, a 5 V supply is placed on the wiper, and the current through Terminal W and Terminal B is plotted with respect to code. A line is also drawn denoting the 5 mA current limit. Note that at low code values (particularly for the 5 kΩ and 10 kΩ options), the current level increases significantly. Care should be taken to limit the current flow between W and B in this state to a maximum continuous current of 5 mA and a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contacts can occur.

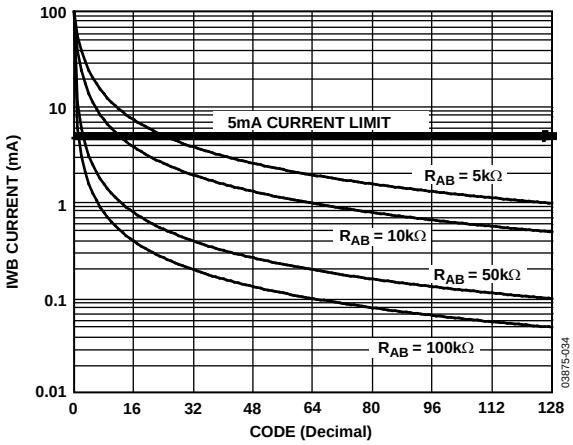

Figure 33. Maximum Operating Current

POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at Terminal B and Terminal W (see Figure 32), it is important to power V_{DD}/GND before applying any voltage to Terminal B and Terminal W; otherwise, the diode is forward biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then V_B/V_W. The relative order of powering V_B and V_W and the digital inputs is not important, providing they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to use a compact, minimum lead-length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 34). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

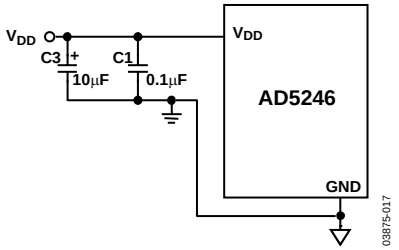

Figure 34. Power Supply Bypassing

CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost for the EEMEM, the AD5246 may be considered as a low cost alternative by maintaining a constant bias to retain the wiper setting. The AD5246 was designed specifically with low power in mind, which allows low power consumption even in battery-operated systems. The graph in Figure 35 demonstrates the power consumption from a 3.4 V 450 mA/hr Li-ion cell phone battery, which is connected to the AD5246.

The measurement over time shows that the device draws approximately 1.3 µA and consumes negligible power. Over a course of 30 days, the battery was depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

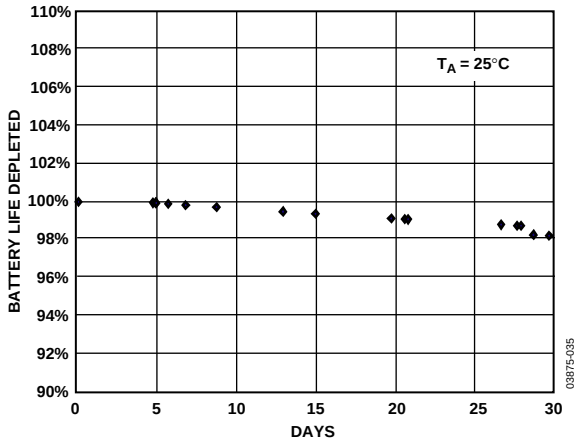

Figure 35. Battery Operating Life Depletion

This demonstrates that constantly biasing the pot is not an impractical approach. Most portable devices do not require the removal of batteries for the purpose of charging. Although the resistance setting of the AD5246 will be lost when the battery needs replacement, such events occur rather infrequently, so that this inconvenience is justified by the lower cost and smaller size offered by the AD5246. If and when total power is lost, the user should be provided with a means to adjust the setting accordingly.

OUTLINE DIMENSIONS

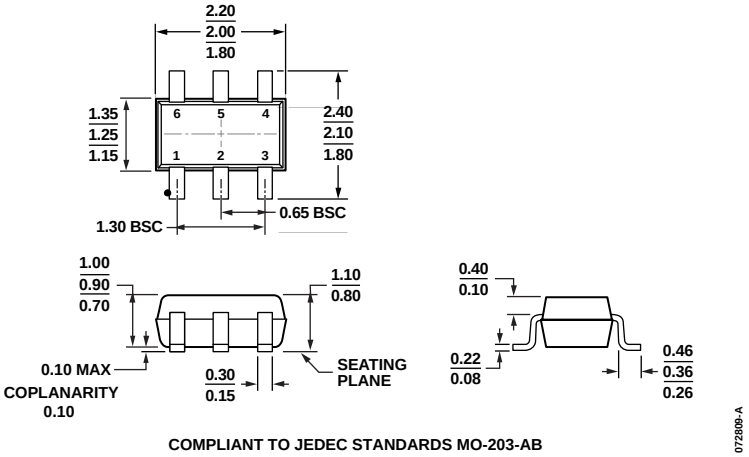

Figure 36. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Branding
AD5246BKSZ5-RL7	5	−40°C to +125°C	6-lead SC70	KS-6	D93
AD5246BKSZ10-R2	10	−40°C to +125°C	6-lead SC70	KS-6	D92
AD5246BKSZ10-RL7	10	−40°C to +125°C	6-lead SC70	KS-6	D92
AD5246BKSZ50-RL7	50	−40°C to +125°C	6-lead SC70	KS-6	D94
AD5246BKSZ100-R2	100	−40°C to +125°C	6-lead SC70	KS-6	D9D
AD5246BKSZ100-RL7	100	−40°C to +125°C	6-lead SC70	KS-6	D9D
EVAL-AD5246DBZ			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.