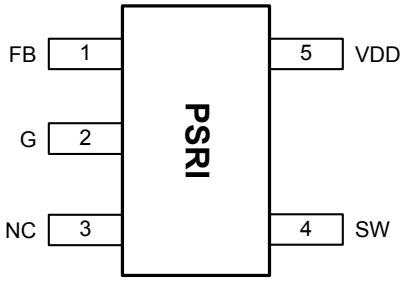
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT355AUC-T	-40°C to 85°C	SOT23-5	5	TAPE & REEL	PSRI

PIN CONFIGURATION



SOT23-5
ACT355AUC-T

PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	FB	Feedback Pin. Connect to a resistor divider network from the auxiliary winding.
2	G	Ground.
3	NC	No Connection.
4	SW	Switch Driver. Connect this pin to the emitter of the power NPN transistor or source of the power MOSFET.
5	VDD	Power Supply.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VDD to G	-0.3 to +23.5	V
Maximum Continuous VDD Current	20	mA
FB to G	-0.3 to +6	V
SW to G	-0.3 to +23.5	V
Continuous SW Current	Internally limited	A
Maximum Power Dissipation (derate 5.3mW/˚C above T_A = 50˚C)	0.53	W
Junction to Ambient Thermal Resistance (θ_{JA})	190	˚C/W
Operating Junction Temperature	-40 to 150	˚C
Storage Temperature	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

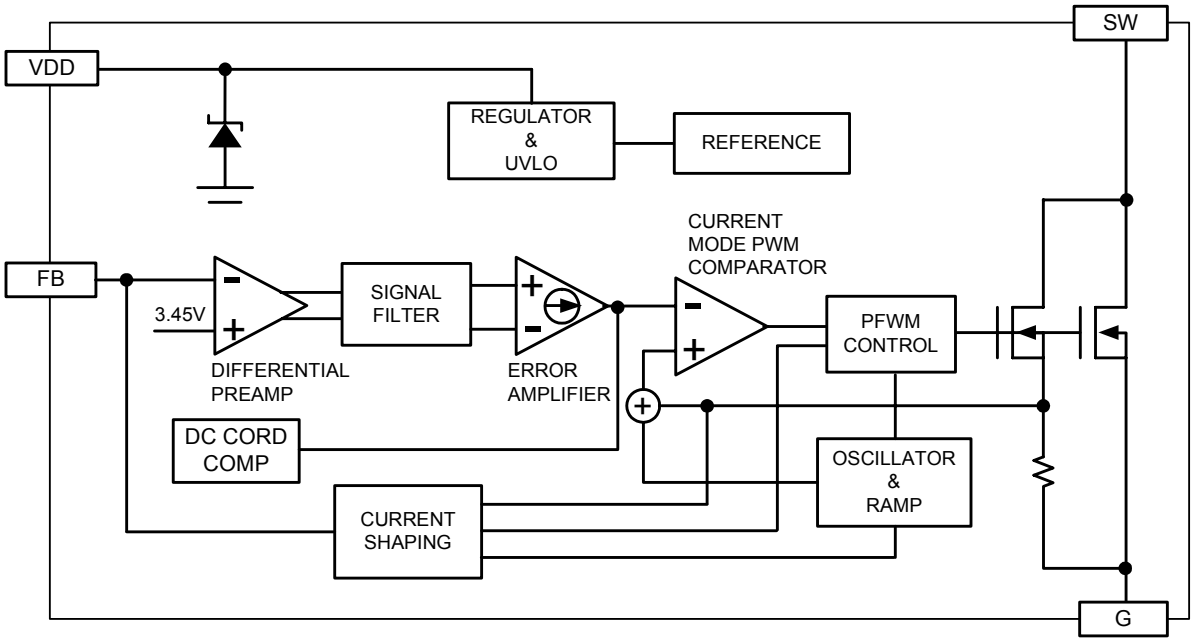
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 15V, V_{OUT} = 5V, L_P = 2mH, N_P = 130, N_S = 10, N_A = 32, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising	16.4	19.4	22.0	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling	7	7.5	8	V
VDD OVP Trigger Voltage	V_{DDOVP}		18.2	20.5	22.5	V
Supply Current	I_{DD}			0.8	1.5	mA
Start Up Supply Current	I_{DDST}	V_{DD} = 15V, before turn-on		30	55	μA
Clamp Switching Frequency			45		58	kHz
Effective FB Feedback Voltage	V_{FB}	FB in Regulation	3.415	3.467	3.520	V
Output Cord Resistance Compensation		Maximum Output Power		+3.7		%
Primary Current Limit	I_{LIM}			320		mA
Maximum Duty Cycle	D_{MAX}	I_{SW} = 10mA	80	86	92	%
Switch On-Resistance	R_{ON}	I_{SW} = 50mA		3.5	5	Ω
SW Rise Time		1nF load, 15Ω pull-up		30		ns
SW Fall Time		1nF load, 15Ω pull-up		20		ns
SW Off Leakage Current		Switch in off-state, V_{SW} = 22V		1	10	μA
Over-Temperature Threshold				160		˚C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As shown in the *Functional Block Diagram,* the ACT355A feedback regulation is done via several circuit blocks to pre-amplify the FB pin error voltage relative to an internal reference, filter out the switching transients, and integrate the resulting useful differential error voltage for current mode PFWM (Pulse Frequency and Width Modulation) control.

SW is a driver output that drives the emitter of an external high voltage NPN transistor or N-channel MOSFET. This emitter-drive method takes advantage of the high V_{CBO} of the transistor, allowing a low cost transistor such as '13003 (V_{CBO} = 700V) or '13002 (V_{CBO} = 600V) to be used for a wide AC input range.

Startup Mode

VDD is the power supply terminal for the IC. During startup, the IC typically draws 30μA supply current. The bleed resistor from the rectified high voltage DC rail supplies current to VDD until it exceeds the V_{DDON} threshold of 19.4V. At this point, the IC enters normal operation when switching begins and the output voltage begins to rise. The VDD bypass capacitor must supply the IC and the NPN base drive until the output voltage builds up enough to provide power from the auxiliary winding to sustain the VDD. The V_{DDOFF} threshold is 7.5V, and therefore, the voltage on the VDD capacitor must not drop more than 10V while the output is charging up.

Constant Voltage (CV) Mode

In constant voltage operation, the IC captures the auxiliary flyback signal at FB pin through a resistor divider network R5 and R6 in the simplified application circuit. The FB pin is pre-amplified against the reference voltage, and the secondary side output voltage error is extracted based on Active-Semi's proprietary filter architecture. This error signal is then integrated by the Error Amplifier .

When the secondary output voltage is above regulation, the Error Amplifier output voltage decreases to reduce the switch current. When the secondary side is below regulation, the Error Amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = 3.45V \times \left(1 + \frac{R5}{R6}\right)\left(\frac{N_S}{N_A}\right) - V_F \qquad (1)$$

where R5 and R6 are top and bottom feedback resistor, N_S and N_A are numbers of transformer secondary and auxiliary turns, and V_F is the rectifier diode forward drop voltage at approximately 0.1A bias. The ACT355A includes internal feedback loop compensation to simplify application circuit design.

Constant Current (CC) Mode

When the secondary output current reaches a level set by the internal current limiting circuit, the IC enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An Internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is $½(L_P \times I_{LIM}^2) \times \eta$, where L_P is the transformer primary inductance, I_{LIM} is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} L_P \times I_{LIM}^2 \left(\frac{\eta \times f_{SW}}{V_{OUTCV}} \right) \quad (2)$$

where f_{SW} is the nominal switching frequency and V_{OUTCV} is the nominal secondary output voltage. The constant current operation typically extends down to lower than 40% of output voltage regulation.

Light Load Mode

When the secondary side output load current decreases to an internally set light load level, the IC's switching frequency is also reduced to save power. This enables the application to meet all current green energy standards. The actual minimum switching frequency is programmable with a small dummy load (while still meeting standby power).

Short Circuit Mode

When the secondary side output is short circuited, the ACT355A enters hiccup mode operation. In this condition, the auxiliary supply voltage collapses and the VDD voltage drops below the V_{DDOFF} threshold. This turns off the IC and causes it to restart. This hiccup behavior continues until the short circuit is removed.

Output Over Voltage Protection

The ACT355A includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage or when no feedback signal is detected for 8 consecutive switching cycles. The IC enters hiccup mode when an output over voltage fault is detected.

Loop Compensation

The ACT355A integrates loop compensation circuitry for simplified application design, optimized transient response, and minimal external components.

Primary Inductance Compensation

The ACT355A includes built-in primary inductance compensation to maintain constant current regulation despite variations in transformer manufacturing.

Peak Inductor Current Limit Compensation

The ACT355A includes peak inductor current limit compensation to achieve constant input power over wide line and wide load range.

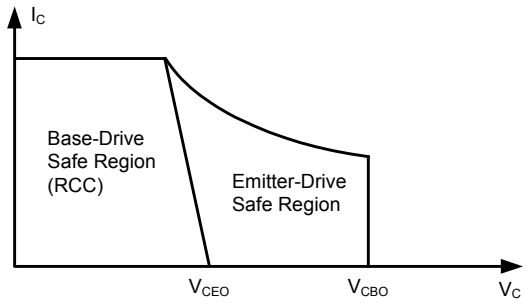
Output Cord Resistance Compensation

The ACT355A provides automatic output cord resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to a typical correction of 3.2% at full power. This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cord resistance.

APPLICATIONS INFORMATION

Figure 2:

NPN Transistor Reverse Bias Safe Operation Area



External Power Transistor

The ACT355A allows a low-cost high voltage power NPN transistor such as '13003 or '13002 to be used safely in flyback configuration. The required collector voltage rating for V_{AC} = 265V with full output load is at least 600V to 700V. As seen from Figure 2, *NPN Reverse Bias Safe Operation Area*, the breakdown voltage of an NPN is significantly improved when it is driven at its emitter. Thus, the ACT355A+'13002 or '13003 combination meets the necessary breakdown safety requirement. Table 1 lists the breakdown voltage of some transistors appropriate for use with the ACT355A.

The power dissipated in the NPN transistor is equal to the collector current times the collector-emitter voltage. As a result, the transistor must always be in saturation when turned on to prevent excessive power dissipation. Select an NPN transistor with sufficiently high current gain (h_{FEMIN} > 8) and a base drive resistor low enough to ensure that the transistor easily saturates.

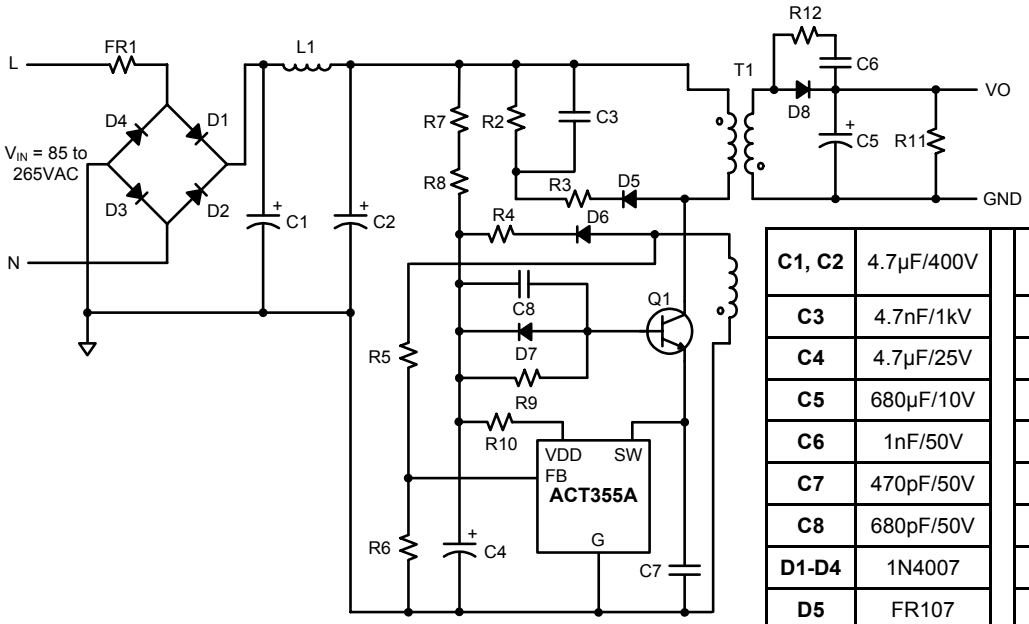
Table 1:

Recommended NPN Transistor

DEVICE	V_{CBO}	V_{CEO}	I_C	h_{FEMIN}	PACKAGE
MJE13002	600V	300V	1.5A	25	TO-126
MJE13003, KSE13003	700V	400V	1.5A	25	TO-126
STX13003	700V	400V	1A	25	TO-92

Figure 3:

Typical Application Circuit



C1, C2	4.7µF/400V	**Q1**	'13002S, TO-92
C3	4.7nF/1kV	**L1**	1.5mH
C4	4.7µF/25V	**FR1**	10Ω
C5	680µF/10V	**R2, R7, R8**	750kΩ
C6	1nF/50V	**R3, R10**	100Ω
C7	470pF/50V	**R4**	33Ω
C8	680pF/50V	**R5**	See Table 2
D1-D4	1N4007	**R6**	See Table 2
D5	FR107	**R9**	390Ω
D6	HER103	**R11**	1kΩ
D7	1N4148	**R12**	10Ω
D8	SB240	**T1**	See Table 2

Design Procedure

Figure 3, *Typical Application Circuit*, shows a complete, optimized constant voltage/constant current charger application. The application design procedure for using the ACT355A is simple. Three components determine the output constant voltage and constant current settings: the transformer T_1 and resistors R5 and R6. Refer to Table 2 for selection values for these three key components for different typical design cases. The *Typical Application Circuit* in Figure 3 lists component values of other devices in the a complete charger application.

Design Notes

1) Feedback resistors R5 and R6 must meet the ±1% maximum tolerance to have good V_0 regulation.
2) The value of the feedback resistor can be chosen slightly different from the table according to the actual system efficiencies in different systems.
3) C8 must be added to guarantee good CC accuracy.

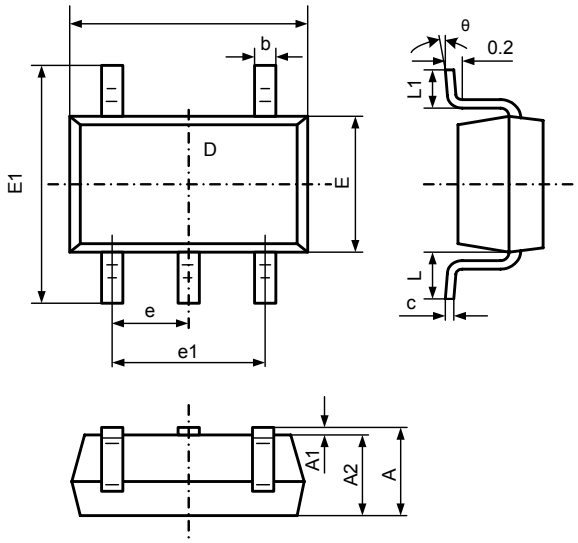
Table 2:

Component Selection Table

DESIGN CASE	OUTPUT		*ActivePSR*™ PART NUMBER	TRANSFORMER				RESISTOR NETWORK	
	V_O (V)	I_O (mA)		N_P	N_A	N_S	L_P±7% (mH)	R5±1% (kΩ)	R6±1% (kΩ)
1	5.0	500	ACT355A	130	32	10	1.6	26.7	6.98
2	5.0	600	ACT355A	130	32	10	1.8	31.6	8.25
3	5.0	650	ACT355A	130	32	10	1.9	34.4	9.09

PACKAGE OUTLINE

SOT23-5 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°