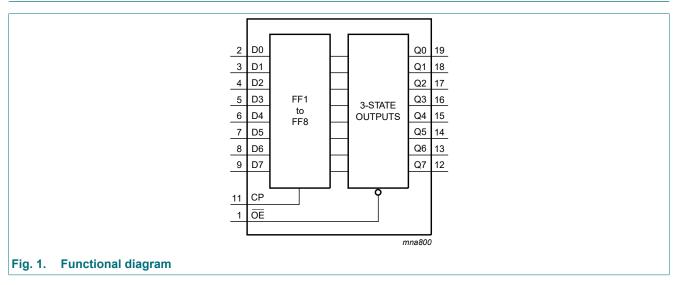
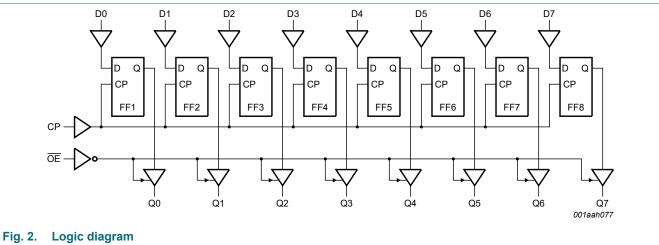
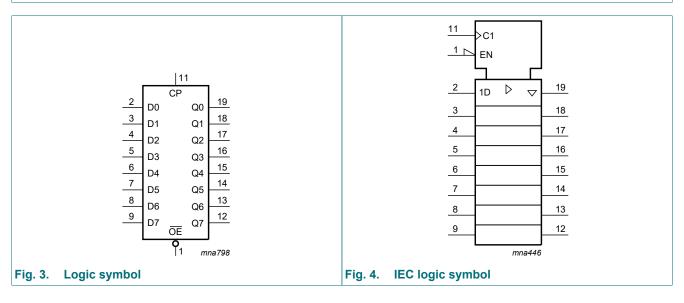
4. Functional diagram

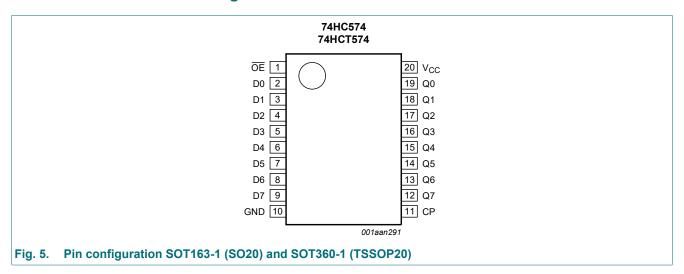






5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
ŌĒ	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data inputs
GND	10	ground (0 V)
СР	11	clock input (LOW-to-HIGH, edge triggered)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop outputs
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;

L = LOW voltage level; I = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;

 $Z = high-impedance OFF-state; \uparrow = LOW-to-HIGH clock transition.$

Operating mode	Input		Internal	Output	
	ŌĒ	СР	Dn	flip-flop	Qn
Load and read register	L	1	I	L	L
	L	1	h	Н	Н
Load register and disable output	Н	↑	I	L	Z
	Н	↑	h	Н	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
Io	output current	$V_O = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±35	mA
I _{CC}	supply current		-	+70	mA
I _{GND}	ground current		-	-70	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

^[1] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C. For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC574			74HCT574			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
74HC574	4									
V_{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_{O} = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 6.0$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10.0	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μA
C _I	input capacitance	•		3.5	-	-	-	-	-	pF
74HCT5	74		'	'	'	'			'	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	8.0	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	Ι _Ο = 20 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μA
ΔI _{CC}	additional supply current	$V_I = V_{CC} - 2.1 \text{ V};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $I_O = 0 \text{ A}$								
		per input pin; Dn inputs	-	50	180	-	225	-	245	μΑ
		per input pin; OE input	-	125	450	-	563	-	613	μΑ
		per input pin; CP input	-	150	540	-	675	-	735	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

Product data sheet

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 9.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC57	4									
t _{pd}	propagation	CP to Qn; see Fig. 6]							
	delay	V _{CC} = 2.0 V	-	47	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	17	30	-	35	-	45	ns
		V _{CC} = 5 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	26	-	33	-	38	ns
t _{en}	enable time	OE to Qn; see Fig. 8	2]							
		V _{CC} = 2.0 V	-	44	140	-	175	-	210	ns
		V _{CC} = 4.5 V	-	16	28	-	35	-	42	ns
		V _{CC} = 6.0 V	-	13	24	-	30	-	36	ns
t _{dis}	disable time	OE to Qn; see Fig. 8	3]							
		V _{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V _{CC} = 6.0 V	-	11	21	-	26	-	32	ns
t _t	transition	Qn; see Fig. 6	1]							
	time	V _{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V _{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V _{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t _W	pulse width	CP HIGH or LOW; see Fig. 7								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t _{su}	set-up time	Dn to CP; see Fig. 7								
		V _{CC} = 2.0 V	60	6	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	2	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	2	-	13	-	15	-	ns
t _h	hold time	Dn to CP; see Fig. 7								
		V _{CC} = 2.0 V	5	0	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	0	-	5	-	5	-	ns
		V _{CC} = 6.0 V	5	0	-	5	-	5	-	ns
f _{max}	maximum	CP; see Fig. 6								
	frequency	V _{CC} = 2.0 V	6.0	37	-	4.8	-	4.0	-	MHz
		V _{CC} = 4.5 V	30	112	-	24	-	20	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	123	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	133	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	$C_L = 50 \text{ pF; } f = 1 \text{ MHz;}$ $V_I = \text{GND to } V_{CC}$	5] -	22	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT5	74							<u> </u>	<u> </u>	
t _{pd}	propagation	CP to Qn; see Fig. 6 [1]								
	delay	V _{CC} = 4.5 V	-	18	33	-	41	-	50	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _{en}	enable time	OE to Qn; see Fig. 8 [2]								
		V _{CC} = 4.5 V	-	19	33	-	41	-	50	ns
t _{dis}	disable time	OE to Qn; see Fig. 8 [3]								
		V _{CC} = 4.5 V	-	16	28	-	35	-	42	ns
t _t	transition	Qn; see <u>Fig. 6</u> [4]								
	time	V _{CC} = 4.5 V	-	5	12	-	15	-	18	ns
t _W	pulse width	CP HIGH or LOW; see Fig. 7								
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
t _{su}	set-up time	Dn to CP; see Fig. 7								
		V _{CC} = 4.5 V	12	3	-	15	-	18	-	ns
t _h	hold time	Dn to CP; see Fig. 7								
		V _{CC} = 4.5 V	5	-1	-	5	-	5	-	ns
f _{max}	maximum	CP; see Fig. 6								
	frequency	V _{CC} = 4.5 V	30	69	-	24	-	20	-	MHz
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	76	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	$C_L = 50 \text{ pF; } f = 1 \text{ MHz;}$ [5] V _I = GND to V _{CC} - 1.5 V	-	25	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] [3] t_{en} is the same as t_{PZH} and t_{PZL} . t_{dis} is the same as t_{PLZ} and t_{PHZ} .

- t_{dis} is the same as t_{THL} and t_{TLH}.
 C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 P_D = C_{PD} x V_{CC}² x f_i x N + Σ(C_L x V_{CC}² x f_o) where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

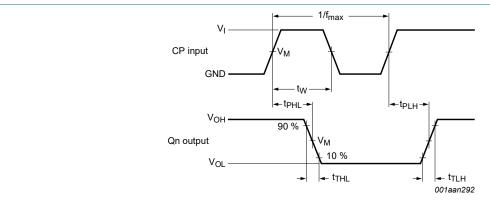
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \ x \ V_{CC} \ ^2 \ x \ f_o) = sum \ of \ outputs.$

Product data sheet

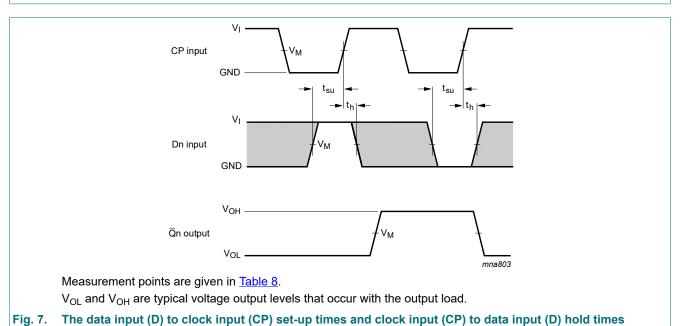
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



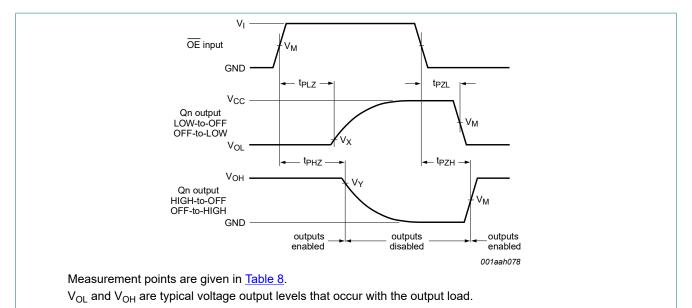
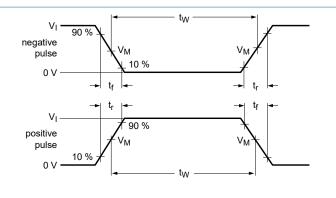
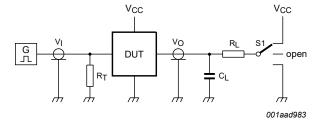


Fig. 8. Enable and disable times

Table 8. Measurement points

Туре	Input	Output					
	V _M	V _M	V _X	V _Y			
74HC574	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}			
74HCT574	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}			





Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

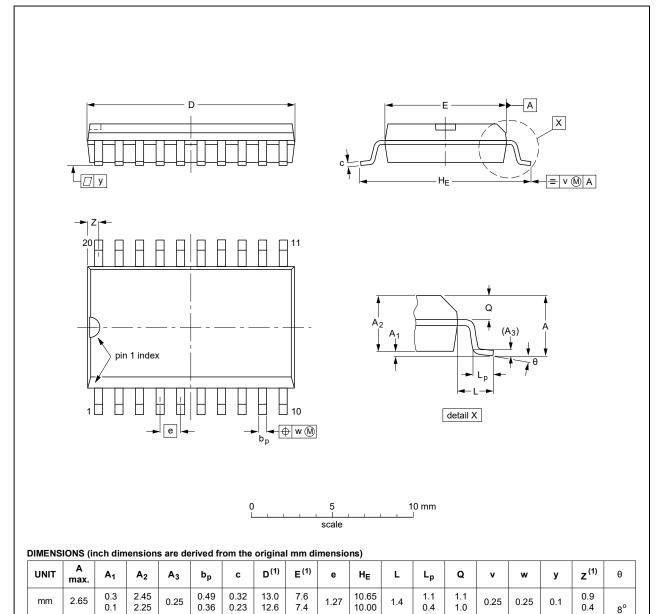
Туре	Input Load		S1 position				
	V _I	t _r , t _f	CL	R_L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t_{PZL}, t_{PLZ}
74HC574	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74HCT574	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

Product data sheet

11. Package outline



SOT163-1



inches

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.019

0.014

0.013

0.009

0.51

0.49

0.30

0.29

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013				99-12-27 03-02-19

0.05

0.419

0.394

0.055

0.043

0.016

0.043

0.039

0.01

0.01

Fig. 10. Package outline SOT163-1 (SO20)

0.012

0.004

0.096

0.089

0.01

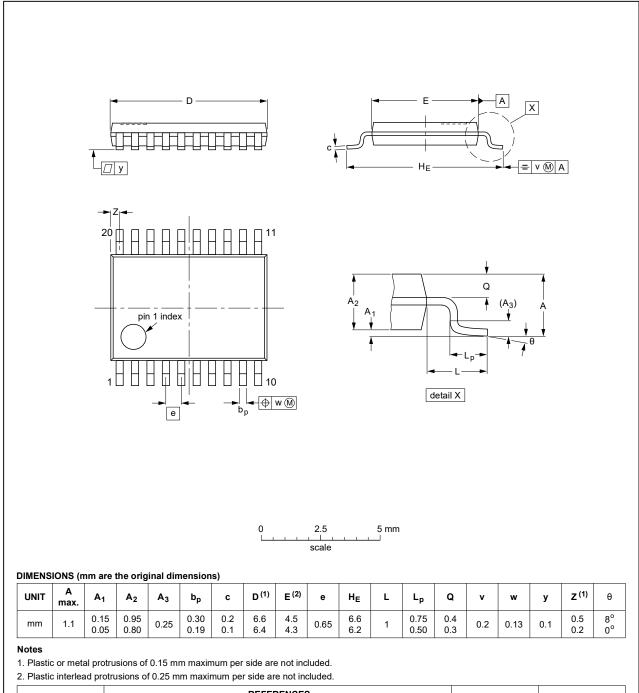
Product data sheet

0.035

0.016

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



OUTLINE		REFER	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT360-1		MO-153			99-12-27 03-02-19

Fig. 11. Package outline SOT360-1 (TSSOP20)

Product data sheet

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT574 v.8	20210730	Product data sheet	-	74HC_HCT574 v.7	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC574DB and 74HCT574DB (SOT339-1/SSOP20) removed. Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. 				
74HC_HCT574 v.7	20160304	Product data sheet	-	74HC_HCT574 v.6	
Modifications:	Type numbers 74HC574N and 74HCT574N (SOT146-1) removed.				
74HC_HCT574 v.6	20150126	Product data sheet	-	74HC_HCT574 v.5	
Modifications:	<u>Section 7</u> : Power dissipation capacitance condition for 74HCT574 is corrected.				
74HC_HCT574 v.5	20120425	Product data sheet	-	74HC_HCT574 v.4	
Modifications:	V _X and V _Y measurement points added to <u>Table 8</u> .				
74HC_HCT574 v.4	20111219	Product data sheet	-	74HC_HCT574 v.3	
Modifications:	Legal pages updated.				
74HC_HCT574 v.3	20101215	Product data sheet	-	74HC_HCT574_CNV v.2	
74HC_HCT574_CNV v.2	19970827	Product specification	-	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Octal D-type flip-flop; positive edge-trigger; 3-state

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