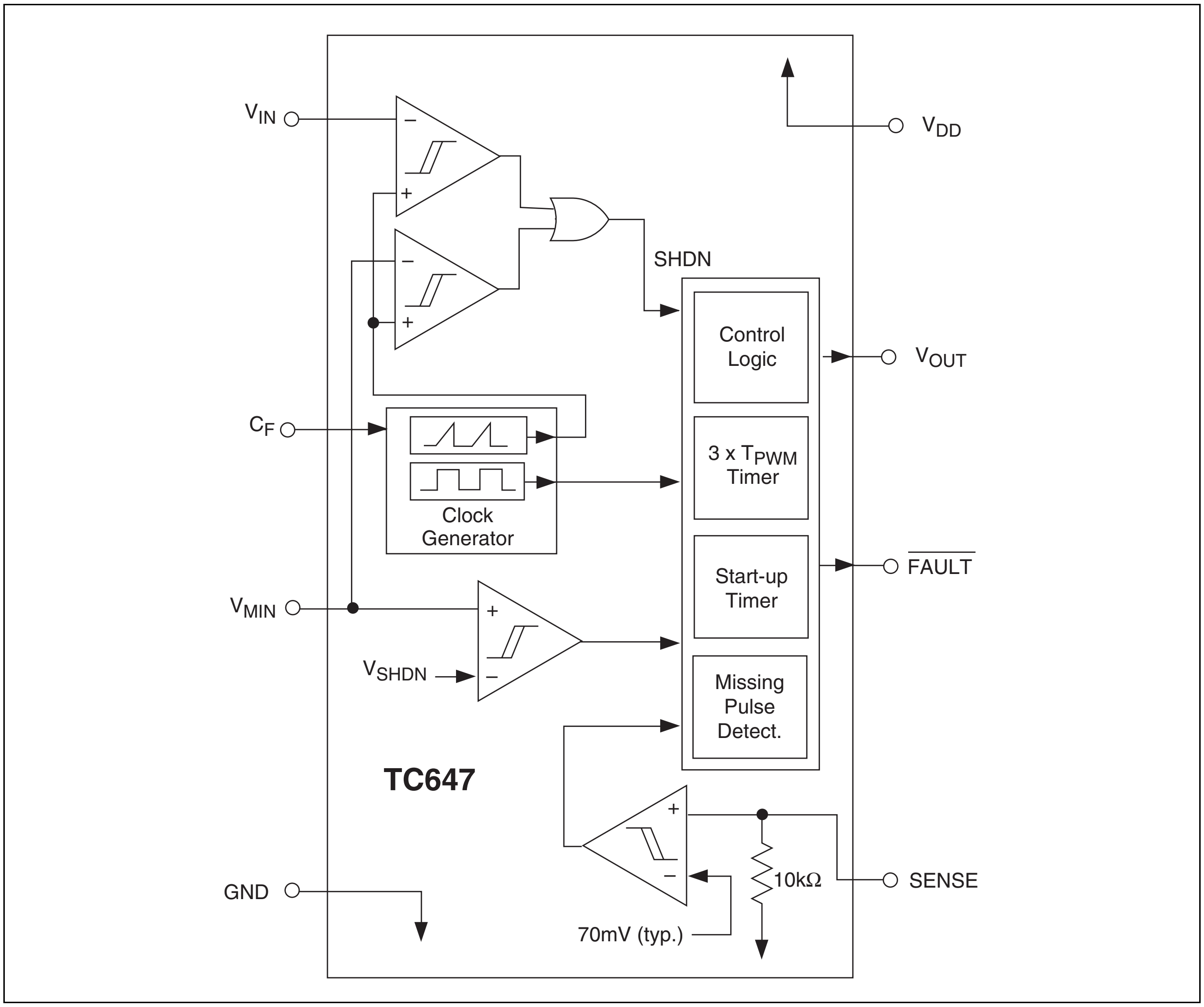
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage 6V

Input Voltage, Any Pin.... (GND – 0.3V) to (V_{DD} +0.3V)

Package Thermal Resistance:

PDIP ($R_{\theta JA}$).. 125°C/W
SOIC ($R_{\theta JA}$) .... 155°C/W
MSOP ($R_{\theta JA}$) .... 200°C/W

Specified Temperature Range .... -40°C to +125°C

Storage Temperature Range.............. -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, $T_{MIN} < T_A < T_{MAX}$, V_{DD} = 3.0V to 5.5V.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{DD}	Supply Voltage	3.0	—	5.5	V	
I_{DD}	Supply Current, Operating	—	0.5	1	mA	Pins 6, 7 Open, C_F = 1 µF, $V_{IN} = V_{C(MAX)}$
$I_{DD(SHDN)}$	Supply Current, Shutdown Mode	—	25	—	µA	Pins 6, 7 Open, C_F = 1 µF, V_{MIN} = 0.35V
I_{IN}	V_{IN}, V_{MIN} Input Leakage	– 1.0	—	+1.0	µA	**Note 1**
V_{OUT} Output						
t_R	V_{OUT} Rise Time	—	—	50	µsec	I_{OH} = 5 mA, **Note 1**
t_F	V_{OUT} Fall Time	—	—	50	µsec	I_{OL} = 1 mA, **Note 1**
t_{SHDN}	Pulse Width (On V_{MIN}) to Clear Fault Mode	30	—	—	µsec	V_{SHDN}, V_{HYST} Specifications, **Note 1**
I_{OL}	Sink Current at V_{OUT} Output	1.0	—	—	mA	V_{OL} = 10% of V_{DD}
I_{OH}	Source Current at V_{OUT} Output	5.0	—	—	mA	V_{OH} = 80% of V_{DD}
V_{IN}, V_{MIN} Inputs						
$V_{C(MAX)}$	Input Voltage at V_{IN} or V_{MIN} for 100% PWM Duty Cycle	2.5	2.65	2.8	V	
$V_{C(SPAN)}$	$V_{C(MAX)} - V_{C(MIN)}$	1.3	1.4	1.5	V	
V_{SHDN}	Voltage Applied to V_{MIN} to Ensure Shutdown Mode	—	—	V_{DD} x 0.13	V	
V_{REL}	Voltage Applied to V_{MIN} to Release Shutdown Mode	V_{DD} x 0.19	—	—	V	V_{DD} = 5V
Pulse Width Modulator						
F_{PWM}	PWM Frequency	26	30	34	Hz	C_F = 1.0 µF
SENSE Input						
$V_{TH(SENSE)}$	SENSE Input Threshold Voltage with Respect to GND	50	70	90	mV	**Note 1**
$\overline{\text{FAULT}}$ Output						
V_{OL}	Output Low Voltage	—	—	0.3	V	I_{OL} = 2.5 mA
t_{MP}	Missing Pulse Detector Timer	—	32/F	—	Sec	
$t_{STARTUP}$	Start-up Timer	—	32/F	—	Sec	
t_{DIAG}	Diagnostic Timer	—	3/F	—	Sec	

Note 1: Ensured by design, not tested.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	V_{IN}	Analog Input
2	C_F	Analog Output
3	V_{MIN}	Analog Input
4	GND	Ground Terminal
5	SENSE	Analog Input
6	$\overline{\text{FAULT}}$	Digital (Open Collector) Output
7	V_{OUT}	Digital Output
8	V_{DD}	Power Supply Input

2.1 Analog Input (V_{IN})

The thermistor network (or other temperature sensor) connects to the V_{IN} input. A voltage range of 1.25V to 2.65V (typical) on this pin drives an active duty cycle of 0% to 100% on the V_{OUT} pin.

2.2 Analog Output (C_F)

C_F is the positive terminal for the PWM ramp generator timing capacitor. The recommended C_F is 1 µF for 30 Hz PWM operation.

2.3 Analog Input (V_{MIN})

An external resistor divider connected to the V_{MIN} input sets the minimum fan speed by fixing the minimum PWM duty cycle (1.25V to 2.65V = 0% to 100%, typical). The TC647 enters shutdown mode when $V_{MIN} \leq V_{SHDN}$. During shutdown, the $\overline{\text{FAULT}}$ output is inactive and supply current falls to 25 µA (typical). The TC647 exits shutdown mode when $V_{MIN} \geq V_{REL}$. See Section 5.0, “Typical Applications”, for more details.

2.4 Ground (GND)

GND denotes the ground terminal.

2.5 Analog Input (SENSE)

Pulses are detected at the SENSE pin as fan rotation chops the current through a sense resistor. The absence of pulses indicates a fault.

2.6 Digital Output ($\overline{\text{FAULT}}$)

The $\overline{\text{FAULT}}$ line goes low to indicate a fault condition. When $\overline{\text{FAULT}}$ goes low due to a fan fault condition, the device is latched in shutdown mode until deliberately cleared or until power is cycled. $\overline{\text{FAULT}}$ may be connected to V_{MIN} if a hard shutdown is desired.

2.7 Digital Output (V_{OUT})

V_{OUT} is an active high complimentary output that drives the base of an external NPN transistor (via an appropriate base resistor) or the gate of an N-channel MOSFET. This output has asymmetrical drive (see Section 1.0, “Electrical Characteristics”).

2.8 Power Supply Input (V_{DD})

V_{DD} may be independent of the fan’s power supply (see Section 1.0, “Electrical Characteristics”).

3.0 DETAILED DESCRIPTION

3.1 PWM

The PWM circuit consists of a ramp generator and threshold detector. The frequency of the PWM is determined by the value of the capacitor connected to the C_F input. A frequency of 30 Hz is recommended (C_F = 1 µF). The PWM is also the time base for the Start-up Timer (see Section 3.3, “Start-Up Timer”). The PWM voltage control range is 1.25V to 2.65V (typical) for 0% to 100% output duty cycle.

3.2 V_{OUT} Output

The V_{OUT} pin is designed to drive a low cost transistor or MOSFET as the low side power switching element in the system. Various examples of driver circuits will be shown throughout this data sheet. This output has an asymmetric complimentary drive and is optimized for driving NPN transistors or N-channel MOSFETs. Since the system relies on PWM rather than linear control, the power dissipation in the power switch is kept to a minimum. Generally, very small devices (TO-92 or SOT packages) will suffice.

3.3 Start-Up Timer

To ensure reliable fan start-up, the Start-up Timer turns the V_{OUT} output on for 32 cycles of the PWM whenever the fan is started from the off state. This occurs at power up and when coming out of shutdown mode. If the PWM frequency is 30 Hz (C_F = 1 µF), the resulting start-up time will be approximately one second. If a fault is detected, the Diagnostic Timer is triggered once, followed by the Start-up Timer. If the fault persists, the device is shut down (see Section 3.6, “FAULT Output”).

3.4 Shutdown Control (Optional)

If V_{MIN} (Pin 3) is pulled below V_{SHDN}, the TC647 will go into shutdown mode. This can be accomplished by driving V_{MIN} with an open-drain logic signal or using an external transistor, as shown in Figure 3-1. All functions are suspended until the voltage on V_{MIN} becomes higher than V_{REL} (0.85V @ V_{DD} = 5.0V). Pulling V_{MIN} below V_{SHDN} will always result in complete device shutdown and reset. The FAULT output is unconditionally inactive in shutdown mode.

A small amount of hysteresis, typically one percent of V_{DD} (50 mV at V_{DD} = 5.0V), is designed into the V_{SHDN}/V_{REL} threshold. The levels specified for V_{SHDN} and V_{REL} in Section 1.0, “Electrical Characteristics”, include this hysteresis plus adequate margin to account for normal variations in the absolute value of the threshold and hysteresis.

CAUTION: Shutdown mode is unconditional. That is, the fan will not be activated regardless of the voltage at V_{IN}. The fan should not be shut down until all heat producing activity in the system is at a negligible level.

3.5 SENSE Input (FanSense™ Technology)

The SENSE input (Pin 5) is connected to a low value current sensing resistor in the ground return leg of the fan circuit. During normal fan operation, commutation occurs as each pole of the fan is energized. This causes brief interruptions in the fan current, seen as pulses across the sense resistor. If the device is not in shutdown mode, and pulses are not appearing at the SENSE input, a fault exists.

The short, rapid change in fan current (high dI/dt) causes a corresponding dV/dt across the sense resistor, R_{SENSE}. The waveform on R_{SENSE} is differentiated and converted to a logic-level, pulse-train by C_{SENSE} and the internal signal processing circuitry. The presence and frequency of this pulse-train is a direct indication of fan operation. See Section 5.0, “Typical Applications”, for more details.

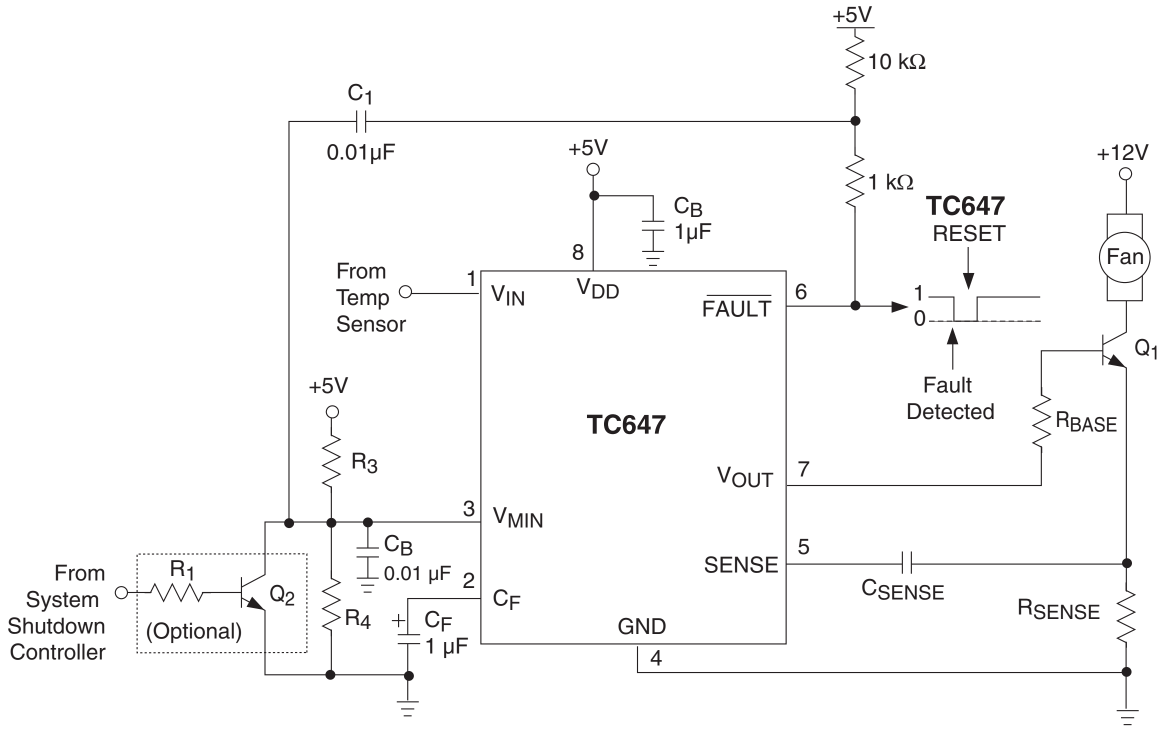
3.6 FAULT Output

Pulses appearing at SENSE due to the PWM turning on are blanked with the remaining pulses being filtered by a missing pulse detector. If consecutive pulses are not detected for 32 PWM cycles (≅1 Sec if C_F = 1 µF), the Diagnostic Timer is activated and V_{OUT} is driven high continuously for three PWM cycles (≅100 msec if C_F = 1 µF). If a pulse is not detected within this window, the Start-up Timer is triggered (see Section 3.3, “Start-Up Timer”). This should clear a transient fault condition. If the missing pulse detector times out again, the PWM is stopped and FAULT goes low. When FAULT is activated due to this condition, the device is latched in shutdown mode and will remain off indefinitely.

Note: At this point, action must be taken to restart the fan by momentarily pulling V_{MIN} below V_{SHDN}, or cycling system power. In either case, the fan cannot remain disabled due to a fault condition as severe system damage could result. If the fan cannot be restarted, the system should be shut down.

The TC647 may be configured to continuously attempt fan restarts, if so desired.

Continuous restart mode is enabled by connecting the $\overline{\text{FAULT}}$ output to V_{MIN} through a 0.1 µF capacitor, as shown in Figure 3-1. When so connected, the TC647 automatically attempts to restart the fan whenever a fault condition occurs. When the $\overline{\text{FAULT}}$ output is driven low, the V_{MIN} input is momentarily pulled below V_{SHDN}, initiating a reset and clearing the fault condition. Normal fan start-up is then attempted as previously described. The $\overline{\text{FAULT}}$ output may be connected to external logic (or the interrupt input of a microcontroller) to shut the TC647 down if multiple fault pulses are detected at approximately one second intervals.



Note: The parallel combination of R_3 and R_4 must be >10 kΩ.

FIGURE 3-1: *Fan Fault Output Circuit.*

4.0 SYSTEM BEHAVIOR

The flowcharts describing the TC647's behavioral algorithm are shown in Figure 4-1. They can be summarized as follows:

4.1 Power-Up

(1) Assuming the device is not being held in shutdown mode ($V_{MIN} > V_{REL}$)…

(2) Turn V_{OUT} output on for 32 cycles of the PWM clock. This ensures that the fan will start from a dead stop.

(3) During this Start-up Timer, if a fan pulse is detected, branch to Normal Operation; if none are received…

(4) Activate the 32-cycle Start-up Timer one more time and look for fan pulse; if a fan pulse is detected, proceed to Normal Operation; if none are received…

(5) Proceed to Fan Fault.

(6) End.

4.2 Normal Operation

Normal Operation is an endless loop which may only be exited by entering shutdown mode or Fan Fault. The loop can be thought of as executing at the frequency of the oscillator and PWM.

(1) Reset the missing pulse detector.

(2) Is TC647 in shutdown? If so…

  a. V_{OUT} duty cycle goes to zero.

  b. $\overline{\text{FAULT}}$ is disabled.

  c. Exit the loop and wait for $V_{MIN} > V_{REL}$ to resume operation (indistinguishable from Power-up).

(3) Drive V_{OUT} to a duty cycle proportional to greater of V_{IN} and V_{MIN} on a cycle by cycle basis.

(4) If a fan pulse is detected, branch back to the start of the loop (1).

(5) If the missing pulse detector times out …

(6) Activate the 3-cycle Diagnostic Timer and look for pulses; if a fan pulse is detected, branch back to the start of the loop (1); if none are received…

(7) Activate the 32-cycle Start-up Timer and look for pulses; if a fan pulse is detected, branch back to the start of the loop (1); if none are received…

(8) Quit Normal Operation and go to Fan Fault.

(9) End.

4.3 Fan Fault

Fan Fault is an infinite loop wherein the TC647 is latched in shutdown mode. This mode can only be released by a reset (i.e., V_{MIN} being brought below V_{SHDN}, then above V_{REL}, or by power cycling).

(1) While in this state, $\overline{\text{FAULT}}$ is latched on (low) and the V_{OUT} output is disabled.

(2) A reset sequence applied to the V_{MIN} pin will exit the loop to Power-up.

(3) End.

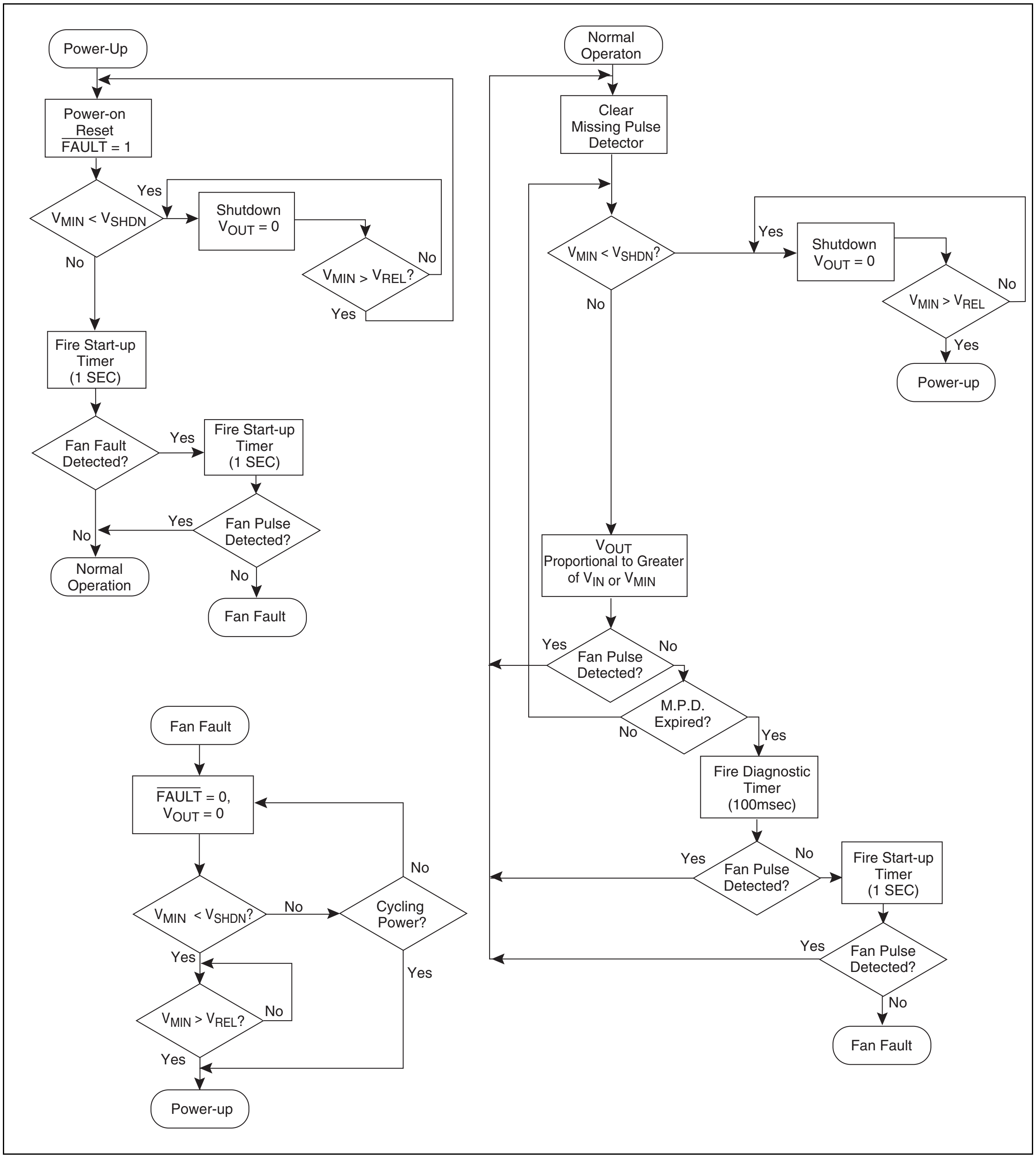


FIGURE 4-1: *TC647 Behavioral Algorithm Flowchart.*

5.0 TYPICAL APPLICATIONS

Designing with the TC647 involves the following:

(1) The temp sensor network must be configured to deliver 1.25V to 2.65V on V_{IN} for 0% to 100% of the temperature range to be regulated.

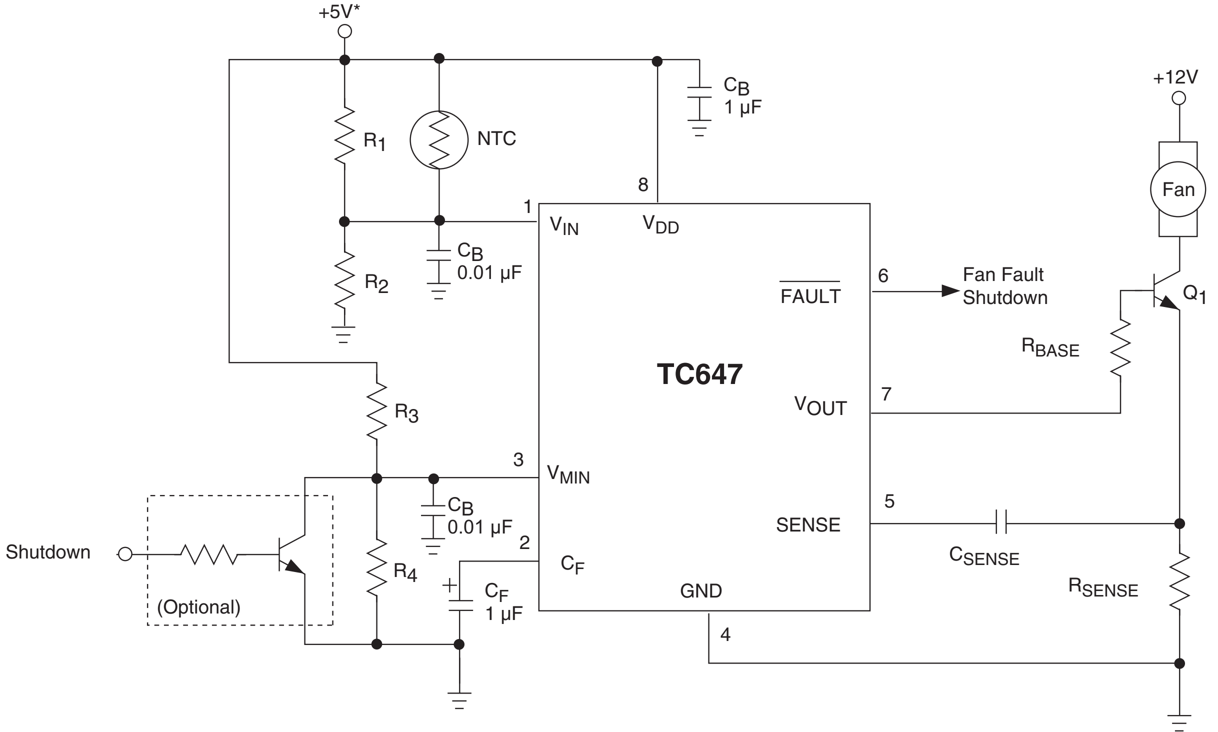
(2) The minimum fan speed (V_{MIN}) must be set.

(3) The output drive transistor and associated circuitry must be selected.

(4) The SENSE network, R_{SENSE} and C_{SENSE}, must be designed for maximum efficiency while delivering adequate signal amplitude.

(5) If shutdown capability is desired, the drive requirements of the external signal or circuit must be considered.

The TC642 demonstration and prototyping board (TC642DEMO) and the TC642 Evaluation Kit (TC642EV) provide working examples of TC647 circuits and prototyping aids. The TC642DEMO is a printed circuit board optimized for small size and ease of inclusion into system prototypes. The TC642EV is a larger board intended for benchtop development and analysis. At the very least, anyone contemplating a design using the TC647 should consult the documentation for both TC642EV and (DS21403) and TC642DEMO (DS21401). Figure 5-1 shows the base schematic for the TC642DEMO.



Note: *See cautions regarding latch-up considerations in Section 5.0, "Typical Applications".

FIGURE 5-1: *Typical Application Circuit.*

5.1 Temperature Sensor Design

The temperature signal connected to V_{IN} must output a voltage in the range of 1.25V to 2.65V (typical) for 0% to 100% of the temperature range of interest. The circuit in Figure 5-2 illustrates a convenient way to provide this signal.

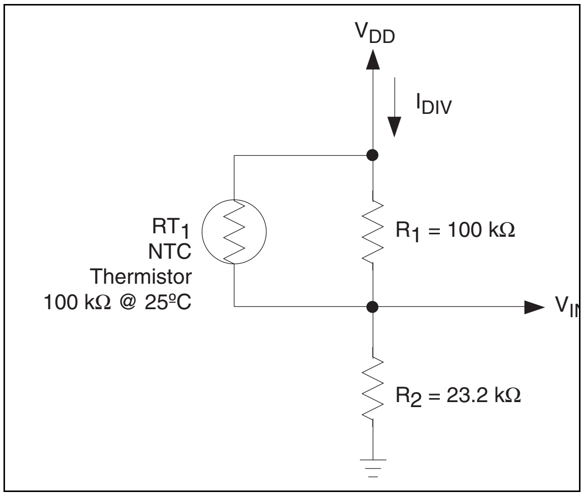


FIGURE 5-2: *Temperature Sensing Circuit.*

Figure 5-2 illustrates a simple temperature dependent voltage divider circuit. RT_1 is a conventional 100 kΩ @ 25°C NTC thermistor, while R_1 and R_2 are standard resistors. The supply voltage, V_{DD}, is divided between R_2 and the parallel combination of RT_1 and R_1 (for convenience, the parallel combination of RT_1 and R_1 will be referred to as R_{TEMP}). The resistance of the thermistor at various temperatures is obtained from the manufacturer's specifications. Thermistors are often referred to in terms of their resistance at 25°C. Generally, the thermistor shown in Figure 5-2 is a non-linear device with a negative temperature coefficient (also called an NTC thermistor). In Figure 5-2, R_1 is used to linearize the thermistor temperature response and R_2 is used to produce a positive temperature coefficient at the V_{IN} node. As an added benefit, this configuration produces an output voltage delta of 1.4V, which is well within the range of the $V_{C(SPAN)}$ specification of the TC647. A 100 kΩ NTC thermistor is selected for this application in order to keep I_{DIV} at a minimum.

For the voltage range at V_{IN} to be equal to 1.25V to 2.65V, the temperature range of this configuration is 0°C to 50°C. If a different temperature range is required from this circuit, R_1 should be chosen to equal the resistance value of the thermistor at the center of this new temperature range. It is suggested that a maximum temperature range of 50°C be used with this circuit due to thermistor linearity limitations. With this change, R_2 is adjusted according to the following equations:

EQUATION

$$\frac{V_{DD}\ x\ R_2}{R_{TEMP}\ (T_1) + R_2} = V(T_1)$$

$$\frac{V_{DD}\ x\ R_2}{R_{TEMP}\ (T_2) + R_2} = V(T_2)$$

Where T_1 and T_2 are the chosen temperatures and R_{TEMP} is the parallel combination of the thermistor and R_1.

These two equations facilitate solving for the two unknown variables, R_1 and R_2. More information about Thermistors may be obtained from AN679, *"Temperature Sensing Technologies"*, and AN685, *"Thermistors in Single Supply Temperature Sensing Circuits"*, which can be downloaded from Microchip's website at www.microchip.com.

5.2 Minimum Fan Speed

A voltage divider on V_{MIN} sets the minimum PWM duty cycle and, thus, the minimum fan speed. As with the V_{IN} input, 1.25V to 2.65V corresponds to 0% to 100% duty cycle. Assuming that fan speed is linearly related to duty cycle, the minimum speed voltage is given by the equation:

EQUATION

$$V_{MIN} = \frac{Minimum\ Speed}{Full\ Speed}\ x\ (1.4V) + 1.25V$$

For example, if 2500 RPM equates to 100% fan speed, and a minimum speed of 1000 RPM is desired, then the V_{MIN} voltage is:

EQUATION

$$V_{MIN} = \frac{1000}{2500}\ x\ (1.4V) + 1.25V = 1.81V$$

The V_{MIN} voltage may be set using a simple resistor divider as shown in Figure 5-3. Per Section 1.0, "Electrical Characteristics", the leakage current at the V_{MIN} pin is no more than 1 µA. It would be very conservative to design for a divider current, I_{DIV}, of 100 µA. If V_{DD} = 5.0V then;

EQUATION

$$I_{DIV} = 1e^{-4}A = \frac{5.0V}{R_1 + R_2},\ therefore$$

$$R_1 + R_2 = \frac{5.0V}{1e^{-4}A} = 50{,}000\ \Omega = 50\ k\Omega$$

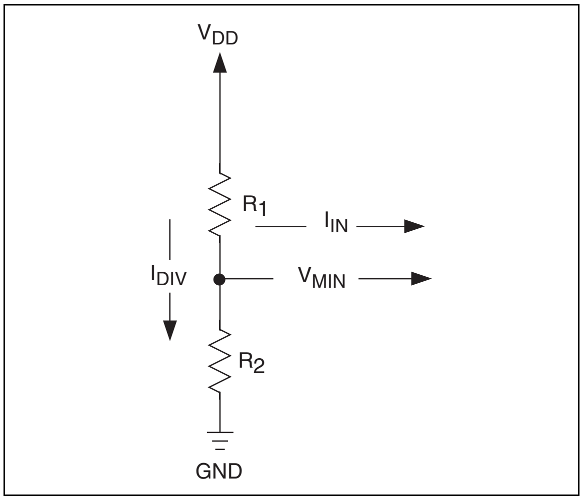


FIGURE 5-3: V_{MIN} Circuit.

We can further specify R_1 and R_2 by the condition that the divider voltage is equal to our desired V_{MIN}. This yields the following equation:

EQUATION

$$V_{MIN} = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

Solving for the relationship between R_1 and R_2 results in the following equation:

EQUATION

$$R_1 = R_2 \times \frac{V_{DD} - V_{MIN}}{V_{MIN}}$$

In this example, $R_1 = (1.762) R_2$. Substituting this relationship back into the previous equation yields the resistor values:

$R_2 = 18.1\ k\Omega$

$R_1 = 31.9\ k\Omega$

In this case, the standard values of 31.6 kΩ and 18.2 kΩ are very close to the calculated values and would be more than adequate.

5.3 Operations at Low Duty Cycle

One boundary condition which may impact the selection of the minimum fan speed is the irregular activation of the Diagnostic Timer due to the TC647 "missing" fan commutation pulses at low speeds. This is a natural consequence of low PWM duty cycles (typically 25% or less). Recall that the SENSE function detects commutation of the fan as disturbances in the current through R_{SENSE}. These can only occur when the fan is energized (i.e., V_{OUT} is "on"). At very low duty cycles, the V_{OUT} output is "off" most of the time. The fan may be rotating normally, but the commutation events are occurring during the PWM's off-time.

The phase relationship between the fan's commutation and the PWM edges tends to "walk around" as the system operates. At certain points, the TC647 may fail to capture a pulse within the 32-cycle missing pulse detector window. When this happens, the 3-cycle Diagnostic Timer will be activated, the V_{OUT} output will be active continuously for three cycles and, if the fan is operating normally, a pulse will be detected. If all is well, the system will return to normal operation. There is no harm in this behavior, but it may be audible to the user as the fan will accelerate briefly when the Diagnostic Timer fires. For this reason, it is recommended that V_{MIN} be set no lower than 1.8V.

5.4 FanSense™ Network (R_{SENSE} and C_{SENSE})

The FanSense network, comprised of R_{SENSE} and C_{SENSE}, allows the TC647 to detect commutation of the fan motor (FanSense™ technology). This network can be thought of as a differentiator and threshold detector. The function of R_{SENSE} is to convert the fan current into a voltage. C_{SENSE} serves to AC-couple this voltage signal and provide a ground referenced input to the SENSE pin. Designing a proper SENSE network is simply a matter of scaling R_{SENSE} to provide the necessary amount of gain (i.e., the current-to-voltage conversion ratio). A 0.1 µF ceramic capacitor is recommended for C_{SENSE}. Smaller values require larger sense resistors, and higher value capacitors are bulkier and more expensive. Using a 0.1 µF results in reasonable values for R_{SENSE}. Figure 5-4 illustrates a typical SENSE network. Figure 5-5 shows the waveforms observed using a typical SENSE network.

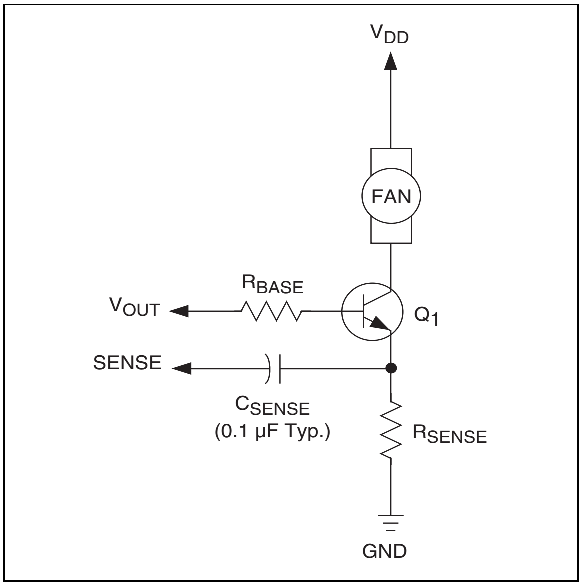


FIGURE 5-4: SENSE Network.

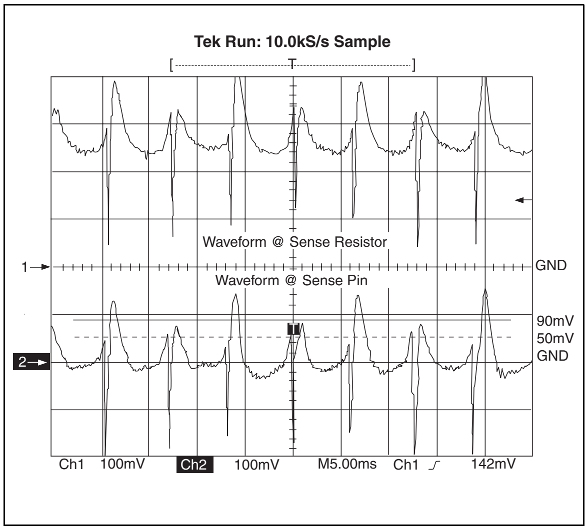


FIGURE 5-5: *SENSE Waveforms.*

Table 5-1 lists the recommended values of R_{SENSE} based on the nominal operating current of the fan. Note that the current draw specified by the fan manufacturer may be a worst-case rating for near-stall conditions and not the fan's nominal operating current. The values in Table 5-1 refer to actual average operating current. If the fan current falls between two of the values listed, use the higher resistor value. The end result of employing Table 5-1 is that the signal developed across the sense resistor is approximately 450 mV in amplitude.

TABLE 5-1: R_{SENSE} VS. FAN CURRENT

Nominal Fan Current (mA)	R_{SENSE} (Ω)
50	9.1
100	4.7
150	3.0
200	2.4
250	2.0
300	1.8
350	1.5
400	1.3
450	1.2
500	1.0

5.5 Output Drive Transistor Selection

The TC647 is designed to drive an external transistor or MOSFET for modulating power to the fan. This is shown as Q_1 in Figures 3-1, 5-1, 5-4, 5-6, 5-7, 5-8 and 5-9. The V_{OUT} pin has a minimum source current of 5 mA and a minimum sink current of 1 mA. Bipolar transistors or MOSFETs may be used as the power switching element, as shown in Figure 5-7. When high current gain is needed to drive larger fans, two transistors may be used in a Darlington configuration. These circuit topologies are shown in Figure 5-7: (a) shows a single NPN transistor used as the switching element; (b) illustrates the Darlington pair; and (c) shows an N-channel MOSFET.

One major advantage of the TC647's PWM control scheme versus linear speed control is that the power dissipation in the pass element is kept very low. Generally, low cost devices in very small packages, such as TO-92 or SOT, can be used effectively. For fans with nominal operating currents of no more than 200 mA, a single transistor usually suffices. Above 200 mA, the Darlington or MOSFET solution is recommended. For the fan sensing function to work correctly, it is imperative that the pass transistor be fully saturated when "on".

Table 5-2 gives examples of some commonly available transistors and MOSFETs. This table should be used as a guide only since there are many transistors and MOSFETs which will work just as well as those listed. The critical issues when choosing a device to use as Q_1 are: (1) the breakdown voltage ($V_{(BR)CEO}$ or V_{DS}(MOSFET)) must be large enough to withstand the highest voltage applied to the fan (**Note:** This will occur when the fan is off); (2) 5 mA of base drive current must be enough to saturate the transistor when conducting the full fan current (transistor must have sufficient gain); (3) the V_{OUT} voltage must be high enough to sufficiently drive the gate of the MOSFET to minimize the $R_{DS(on)}$ of the device; (4) rated fan current draw must be within the transistor's/MOSFET's current handling capability; and (5) power dissipation must be kept within the limits of the chosen device.

A base-current limiting resistor is required with bipolar transistors. This is shown in Figure 5-6.

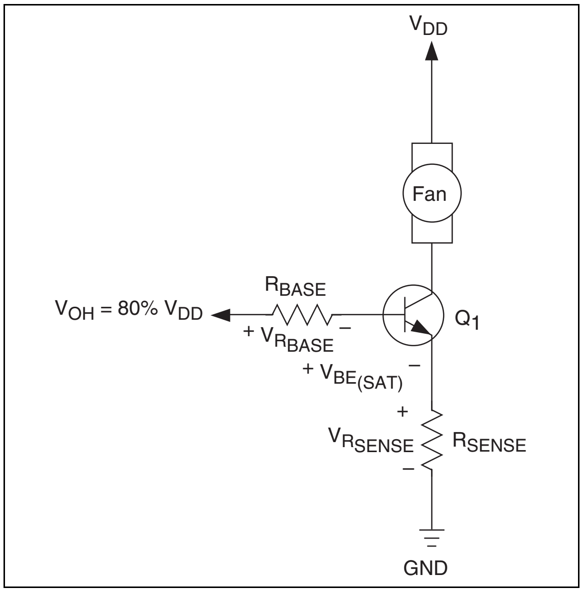


FIGURE 5-6: *Circuit For Determining R_{BASE}.*

The correct value for this resistor can be determined as follows:

$V_{OH} = V_{RSENSE} + V_{BE(SAT)} + V_{RBASE}$

$V_{RSENSE} = I_{FAN} \times R_{SENSE}$

$V_{RBASE} = R_{BASE} \times I_{BASE}$

$I_{BASE} = I_{FAN} / h_{FE}$

V_{OH} is specified as 80% of V_{DD} in Section 1.0, “Electrical Characteristics”; $V_{BE(SAT)}$ is given in the chosen transistor data sheet. It is now possible to solve for R_{BASE}.

EQUATION

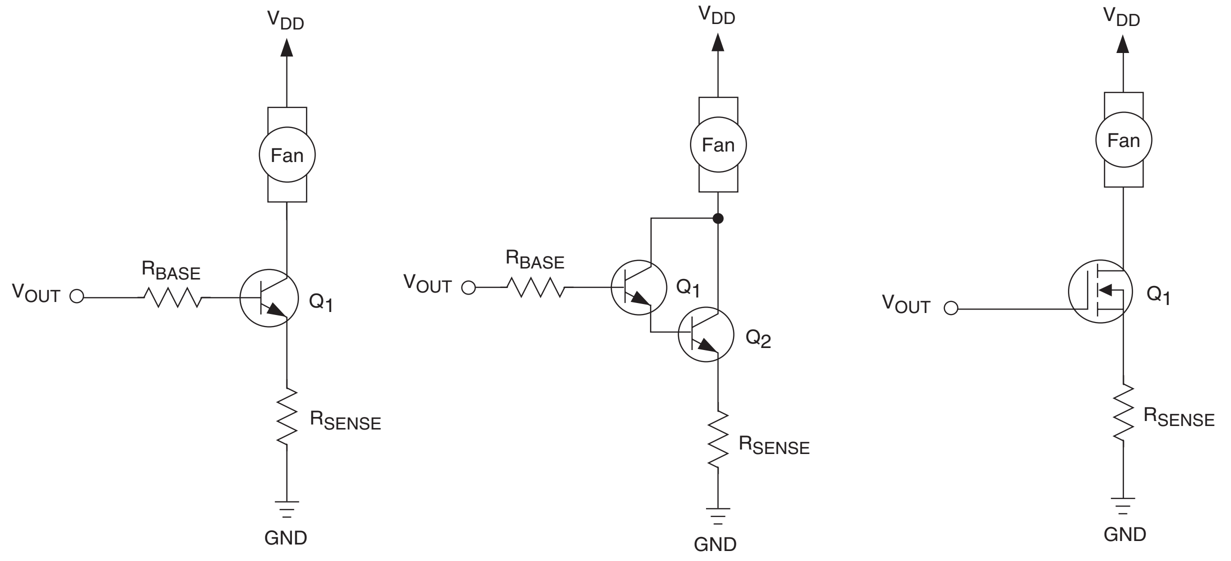
$$R_{BASE} = \frac{V_{OH} - V_{BE(SAT)} - V_{RSENSE}}{I_{BASE}}$$

Some applications require the fan to be powered from the negative 12V supply to keep motor noise out of the positive voltage power supplies. As shown in Figure 5-8, zener diode D_1 offsets the -12V power supply voltage, holding transistor Q_1 off when V_{OUT} is low. When V_{OUT} is high, the voltage at the anode of D_1 increases by V_{OUT} causing Q_1 to turn on. Operation is otherwise the same as the case of fan operation from +12V.

TABLE 5-2: TRANSISTORS AND MOSFETS FOR Q_1 (V_{DD} = 5V)

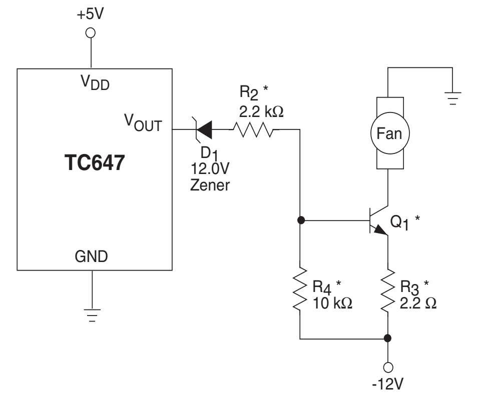
Device	Package	Max. $V_{BE(sat)}/V_{GS}$ (V)	Min. H_{FE}	V_{CEO}/V_{DS} (V)	Fan Current (mA)	Suggested R_{BASE} (Ω)
MMBT2222A	SOT-23	1.2	50	40	150	800
MPS2222A	TO-92	1.2	50	40	150	800
MPS6602	TO-92	1.2	50	40	500	301
SI2302	SOT-23	2.5	NA	20	500	**Note 1**
MGSF1N02E	SOT-23	2.5	NA	20	500	**Note 1**
SI4410	SO-8	4.5	NA	30	1000	**Note 1**
SI2308	SOT-23	4.5	NA	60	500	**Note 1**

Note 1: A series gate resistor may be used in order to control the MOSFET turn-on and turn-off times.



a) Single Bipolar Transistor **b) Darlington Transistor Pair** **C) N-Channel MOSFET**

FIGURE 5-7: *Output Drive Transistor Circuit Topologies.*



*Note: Value depends on the specific application and is shown for example only.

FIGURE 5-8: *Powering the Fan from a -12V Supply.*

5.6 Latch-Up Considerations

As with any CMOS IC, the potential exists for latch-up if signals are applied to the device which are outside the power supply range. This is of particular concern during power-up if the external circuitry (such as the sensor network, V_{MIN} divider or shutdown circuit) is powered by a supply different from that of the TC647. Care should be taken to ensure that the TC647's V_{DD} supply powers up first. If possible, the networks attached to V_{IN} and V_{MIN} should connect to the V_{DD} supply at the same physical location as the IC itself. Even if the IC and any external networks are powered by the same supply, physical separation of the connecting points can result in enough parasitic capacitance and/or inductance in the power supply connections to delay one power supply “routing” versus another.

5.7 Power Supply Routing and Bypassing

Noise present on the V_{IN} and V_{MIN} inputs may cause erroneous operation of the $\overline{\text{FAULT}}$ output. As a result, these inputs should be bypassed with a 0.01 µF capacitor mounted as close to the package as possible. This is particularly true of V_{IN}, which is usually driven from a high impedance source (such as a thermistor). In addition, the V_{DD} input should be bypassed with a 1 µF capacitor. Ground should be kept as short as possible. To keep fan noise off the TC647 ground pin, individual ground returns for the TC647 and the low side of the fan current sense resistor should be used.

Design Example

Step 1. Calculate R_1 and R_2 based on using an NTC having a resistance of 10 kΩ at T_{MIN} (25°C) and 4.65 kΩ at T_{MAX} (45°C) (see Figure 5-9).

R_1 = 20.5 kΩ
R_2 = 3.83 kΩ

Step 2. Set minimum fan speed V_{MIN} = 1.8V. Limit the divider current to 100 µA from which R_5 = 33 kΩ and R_6 = 18 kΩ

Step 3. Design the output circuit.

Maximum fan motor current = 250 mA.
Q_1 beta is chosen at 50 from which
R_7 = 800Ω.

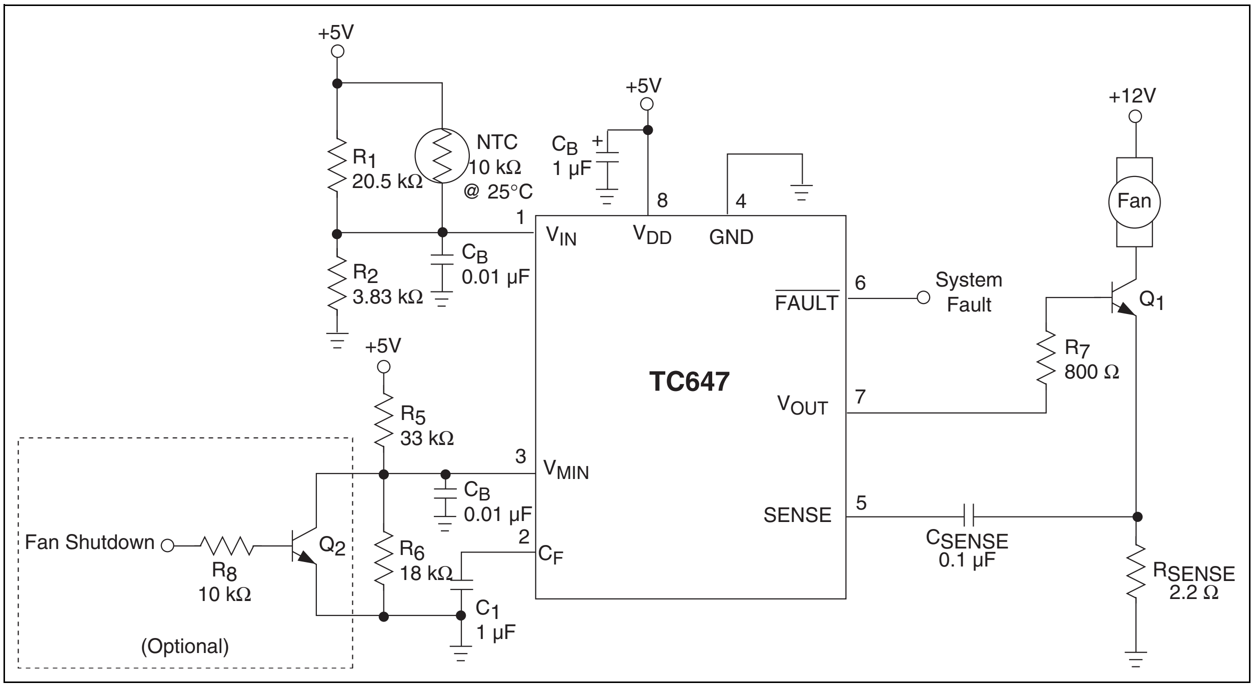


FIGURE 5-9: *Design Example.*

5.8 TC647 as a Microcontroller Peripheral

In a system containing a microcontroller or other host intelligence, the TC647 can be effectively managed as a CPU peripheral. Routine fan control functions can be performed by the TC647 without controller intervention. The microcontroller receives temperature data from one or more points throughout the system. It calculates a fan operating speed based on an algorithm specifically designed for the application at hand. The processor controls fan speed using complimentary port bits I/O1 through I/O3. Resistors R_1 through R_6 (5% tolerance) form a crude 3-bit DAC that translates the 3-bit code from the controller or processor's outputs into a 1.6V DC control signal. A monolithic DAC or digital pot may be used instead of the circuit shown in Figure 5-10.

With V_{MIN} set to 1.8V, the TC647 has a minimum operating speed of approximately 40% of full rated speed when the processor's output code is 000[B]. Output codes 001[B] to 111[B] operate the fan from roughly 40% to 100% of full speed. An open-drain output from the processor I/O can be used to reset the $\overline{\text{TC647}}$ following detection of a fault condition. The $\overline{\text{FAULT}}$ output can be connected to the processor's interrupt input, or to an I/O pin, for polled operation (see Figure 5-10).

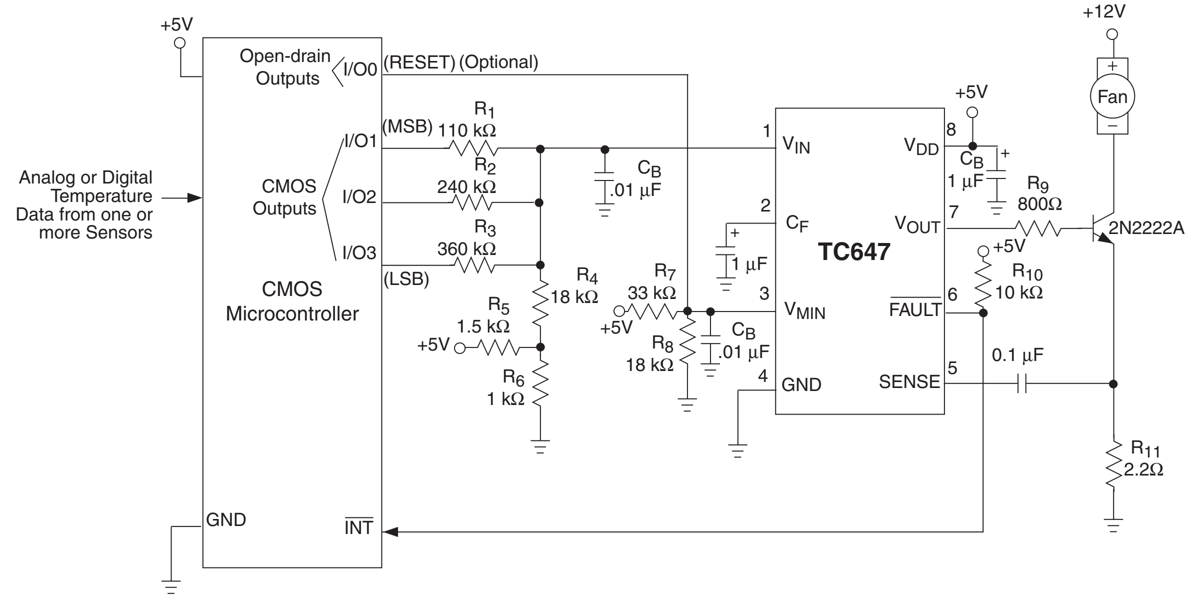
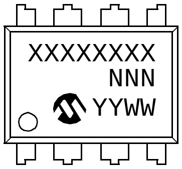


FIGURE 5-10: *TC647 as a Microcontroller Peripheral.*

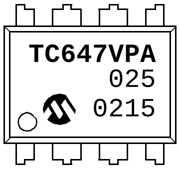
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

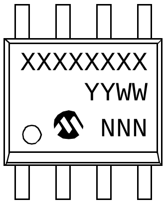
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (150 mil)



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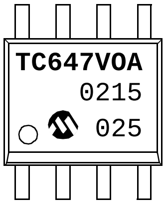
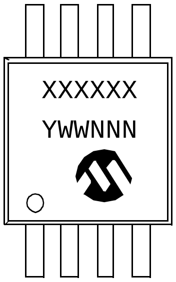


8-Lead MSOP



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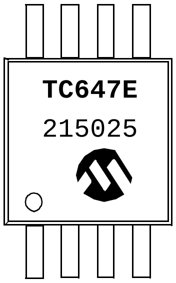
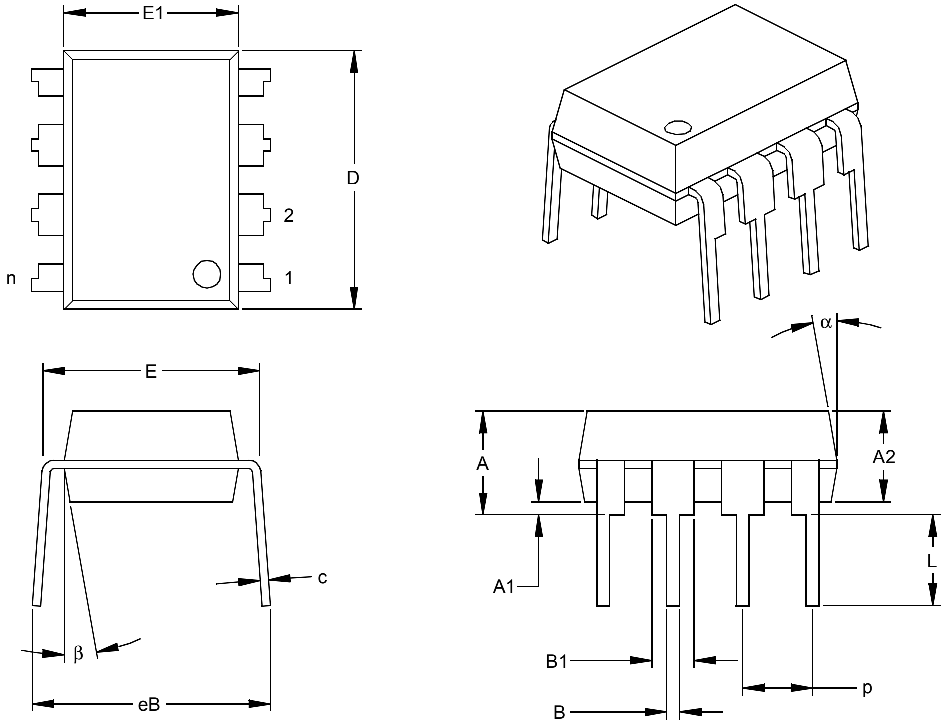


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

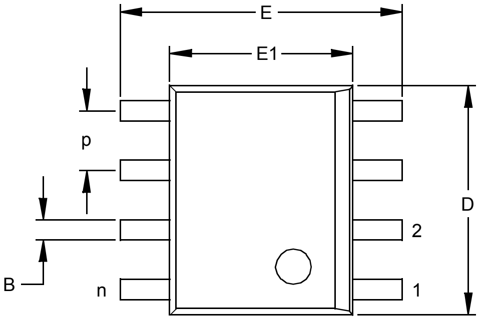


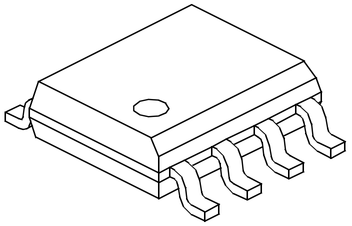
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

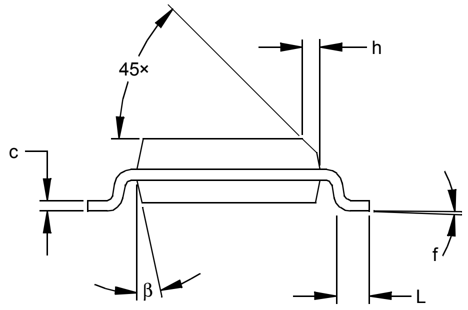
* Controlling Parameter
§ Significant Characteristic

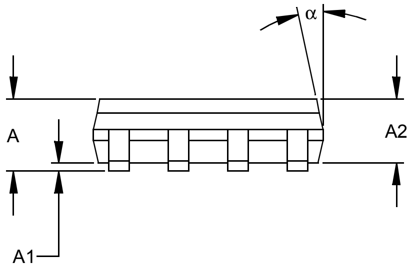
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)







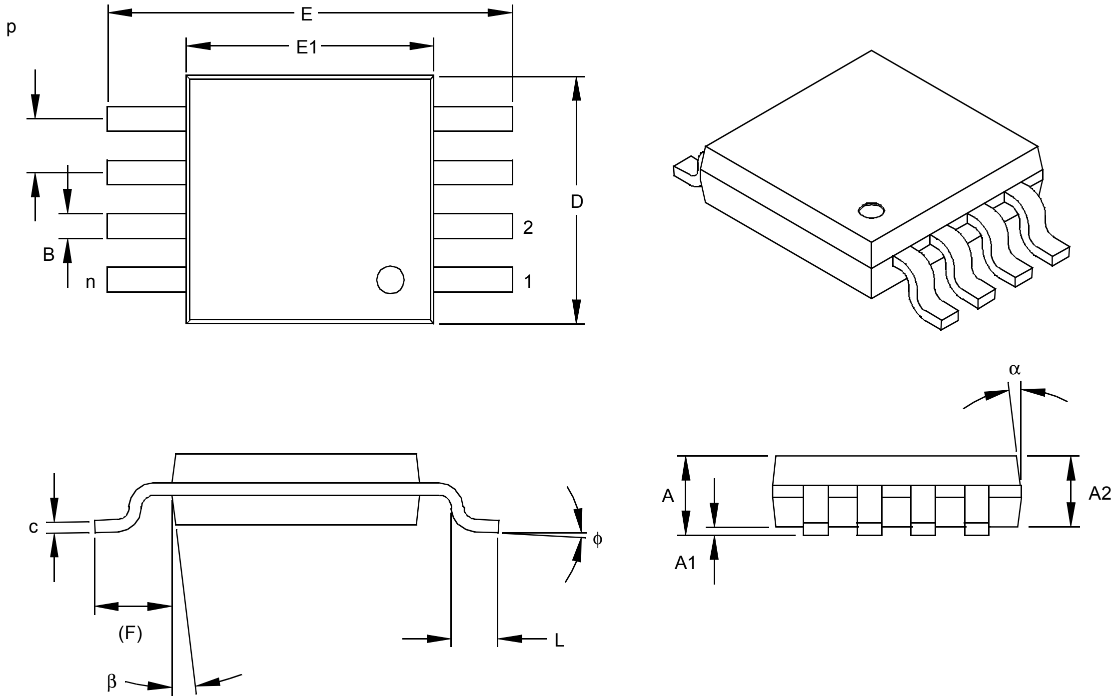


	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

6.2 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

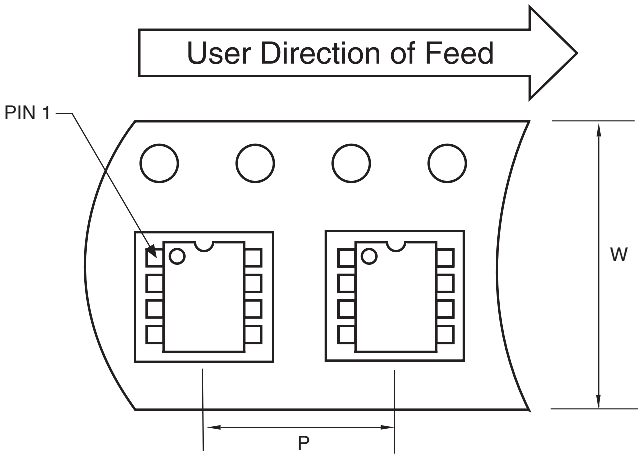
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed. 010" (0.254mm) per side.

Drawing No. C04-111

6.3 Taping Form

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices

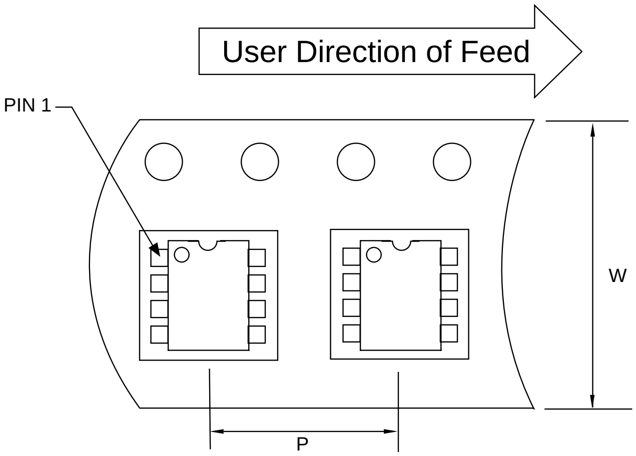


Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin MSOP Devices



Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

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Device: TC647: PWM Fan Speed Controller w/Fault Detection

Temperature Range:
V = 0°C to +85°C
E = -40°C to +85°C

Package:
PA = Plastic DIP (300 mil Body), 8-lead *
OA = Plastic SOIC, (150 mil Body), 8-lead
UA = Plastic Micro Small Outline (MSOP), 8-lead

* PDIP package is only offered in the V temp range

Examples:

a) TC647VOA: PWM Fan Speed Controller w/ Fault Detection, SOIC package.
b) TC647VUA: PWM Fan Speed Controller w/ Fault Detection, MSOP package.
c) TC647VPA: PWM Fan Speed Controller w/ Fault Detection, PDIP package.
d) TC647EOATR: PWM Fan Speed Controller w/Fault Detection, SOIC package, Tape and Reel.

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