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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Supply Voltage Powerup Rise Time	$V_{DD\text{-}RISE}$		10	—	—	µs
Ambient Temperature	T_A		–40	25	85	°C

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–45 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4312 device is a high-performance RF integrated circuit with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of this device should only be done at ESD-protected workstations.
3. For input pins 315/$\overline{434}$, RATIO, BT[1:0], TH[1:0].
4. At RF input pin RX_IN.

Table 3. DC Characteristics

(T_A = 25 °C, V_{DD} = 3.3 V, R_s = 50 Ω, F_{RF} = 433.92 MHz unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{VDD}		—	20	TBD	mA
Reset Supply Current	I_{RST}	Reset asserted	—	2	TBD	µA
High Level Input Voltage[1]	V_{IH}		0.7 x V_{DD}	—	V_{DD} + 0.3	V
Low Level Input Voltage[1]	V_{IL}		–0.3	—	0.3 x V_{DD}	V
High Level Input Current[1]	I_{IH}	V_{IN} = V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[1]	I_{IL}	V_{IN} = 0 V, V_{DD} = 3.6 V	–10	—	10	µA
High Level Output Voltage[2]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{DD}	—	—	V
Low Level Output Voltage[2]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{DD}	V

Notes:
1. For input pins OOK, 315/$\overline{434}$, RATIO, BT[1:0], TH[1:0].
2. For output pin DOUT.

Table 4. Reset Timing Characteristics

(V_{DD} = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width	t_{SRST}	100	—	—	µs

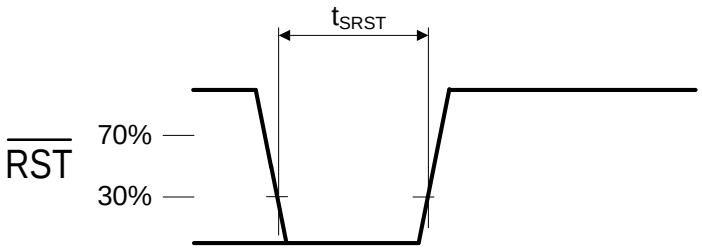


Figure 1. Reset Timing

Table 5. Si4312 Receiver Characteristics

(T_A = 25 °C, V_{DD} = 3.3 V, R_s = 50 Ω, F_{RF} = 433.92 MHz unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity @ BER = 10^{-3} (Note 1)		1.0 kbps, 315 MHz (Note2)	—	–110	—	dBm
		10 kbps, 315 MHz (Note2)	—	–103	—	dBm
		1.0 kbps, 433.92 MHz (Note2)	—	–106	—	dBm
		10 kbps, 433.92 MHz	TBD	–101	—	dBm
Data Rate[3]		NRZ	—	—	10	kbps
Adjacent Channel Rejection ±200 kHz (Note 1)		Desired signal is 3 dB above sensitivity (BER = 10^{-3}), unmodulated interferer is at ±200 kHz, rejection measured as difference between desired signal and interferer level in dB when BER = 10^{-3}	TBD	35	—	dB
Alternate Channel Rejection ±400 kHz[1,2]		Desired signal is 3 dB above sensitivity (BER = 10^{-3}), unmodulated interferer is at ±400 kHz, rejection measured as difference between desired signal and interferer level in dB when BER = 10^{-3}	—	55	—	dB
Image Rejection, IF = 128 kHz[1,2]			—	23	—	dB
Blocking[1,2]		±2 MHz, 1.0 kbps, desired signal is 3 dB above sensitivity, CW interferer level is increased until BER = 10^{-3}	—	65	—	dB
		±10 MHz, 1.0 kbps, desired signal is 3 dB above sensitivity, CW interferer level is increased until BER = 10^{-3}	—	70	—	dB
Maximum RF Input Power [1,2]			—	8	—	dBm
Input IP3[3]		$\lvert f_2 - f_1 \rvert$ = 5 MHz, high gain mode, desired signal is 3 dB above sensitivity, CW interference levels are increased until BER = 10^{-3}	—	–10	—	dBm
LNA Input Capacitance[3]			—	7	—	pF
Receiver Channel Bandwidth[4]			—	160	—	kHz
RX Boot Time[3]		From reset	—	500	—	ms

Notes:
1. 1.0 kbps, Manchester encoded, RATIO = 0, TH[1:0] = 00, xtal = ±20 ppm.
2. Guaranteed by characterization.
3. Guaranteed by design.
4. The frequency scanning (see section “3.6. Frequency Scanning”) extends this to 420 kHz.

Table 6. Crystal Characteristics

(V_{DD} = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillator Frequency			—	16	—	MHz
Crystal ESR			—	—	100	Ω
XTL1, XTL2 Input Capacitance			—	11	—	pF

2. Typical Application Schematic

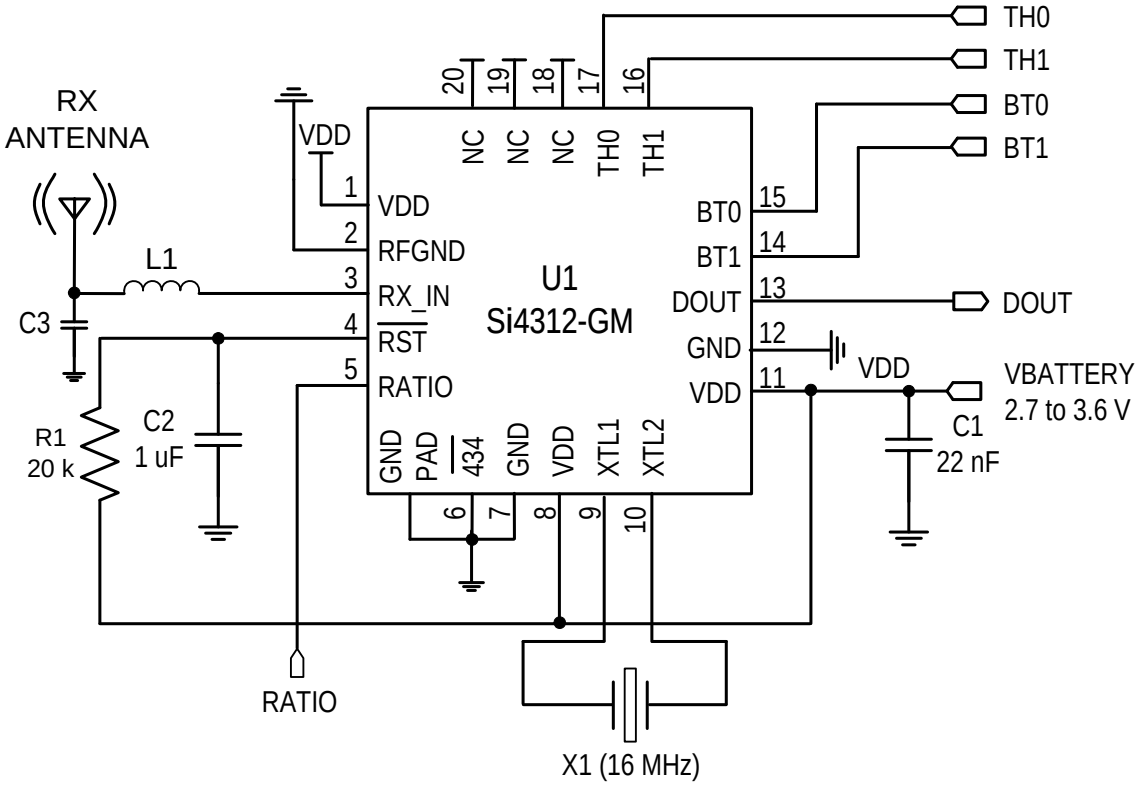


Figure 2. Si4312 OOK 433.92 MHz Application Schematic

2.1. Typical Application Bill of Materials

Table 7. Si4312 Typical Application Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2	Time constant capacitor, 1 µF	Murata
C3	Antenna matching capacitor, 15 pF	Murata
L1	Antenna matching inductor, 33 nH for 433.92 MHz and 62 nH for 315 MHz	Murata
R1	Time constant resistor, 20 kΩ	Murata
X1	16 MHz crystal	Hosonic
U1	Si4312 315/433.92 MHz OOK receiver	Silicon Laboratories

3. Functional Description

3.1. Overview

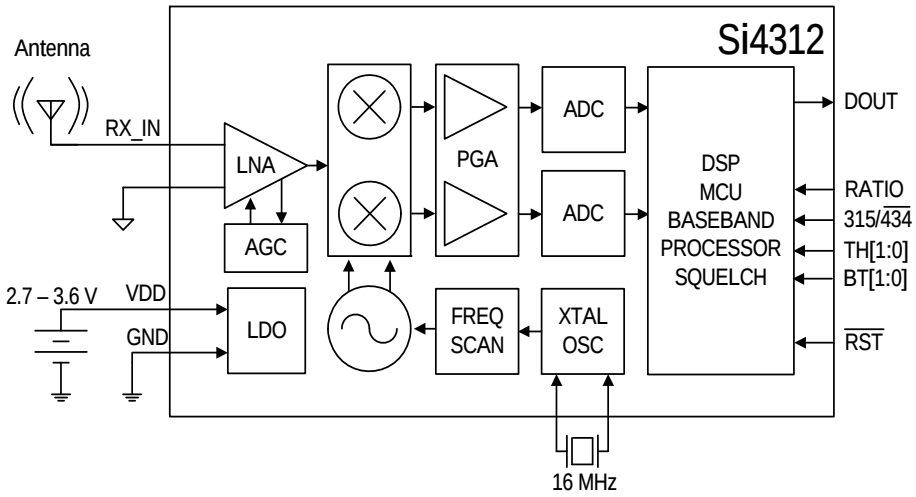


Figure 3. Functional Block Diagram

The Si4312 is a fully-integrated OOK CMOS RF receiver that operates in the unlicensed 315 and 433.92 MHz ultra high frequency (UHF) bands. It is designed for high-volume, cost-sensitive RF receiver applications. The chip operates at a carrier frequency of 315 or 433.92 MHz and supports OOK digital modulation with data rates of up to 10 kbps NRZ or 5 kbps Manchester coded. The Si4312 has selectable data filters to optimize the sensitivity of the receiver for a given data rate. The Si4312 employs a frequency scanning algorithm to improve the sensitivity of the receiver with a small IF bandwidth while still maintaining the ability to accommodate large transmit frequency offsets. The integrated on-chip squelch circuit prevents false output data when the RF input signal is absent or below sensitivity.

The device leverages Silicon Labs' patented and proven digital low-IF architecture and offers superior sensitivity and interference rejection. The Si4312 can achieve superior sensitivity in the presence of large interference due to its high dynamic range ADCs and digital filters. The digital low-IF architecture also enables superior blocking ability and low intermodulation distortion for robust reception in the presence of wide-band interference.

Digital integration reduces the number of required external components compared to traditional offerings, resulting in a solution that only requires a 16 MHz crystal and passive components allowing a small and compact printed circuit board (PCB) implementation area. The high integration of the Si4312 improves the system manufacturing reliability, improves quality, eases design-in, and minimizes costs.

3.2. Receiver Description

The RF input signal is amplified by a low-noise amplifier (LNA) and down-converts to a low intermediate frequency with a quadrature image-reject mixer. The mixer output is amplified by a programmable gain amplifier (PGA), filtered, and digitized with a high-resolution analog-to-digital converter (ADC). All RF functions are integrated into the device eliminating any production alignment issues associated with external components, such as SAW and ceramic IF filters.

Silicon Labs' advanced digital low-IF architecture achieves superior performance by using the DSP to perform channel filtering, demodulation, automatic gain control (AGC), automatic frequency control (AFC), and other baseband processing. DSP implementation of the channel filters provides better repeatability and control of the bandwidth and frequency response of the filter compared to analog implementations. No off-chip ceramic filters are needed with the Si4312 as all IF channel filtering is performed in the digital domain.

3.3. Carrier Frequency Selection

The Si4312 can be tuned to either 315 or 433.92 MHz by driving Pin 6 (315/$\overline{434}$) to VDD or GND. The 315 MHz operation is chosen by driving Pin 6 (315/$\overline{434}$) to VDD, and 433.92 MHz operation is chosen by driving Pin 6 (315/$\overline{434}$) to GND.

Table 8. Carrier Frequency Selection

Pin 6 (315/$\overline{434}$)	Frequency [MHz]
0	433.92
1	315

3.4. Bit Time BT[1:0] Selection

The Si4312 can operate with data rates of up to 10 kbps non-return to zero (NRZ) data or 5 kbps Manchester encoded data. However, OOK modulation uses other encoding schemes such as pulse width modulation (PWM) and pulse position modulation (PPM) where a bit can be encoded into a pulse with a certain duty cycle or pulse width as shown in Figure 4.

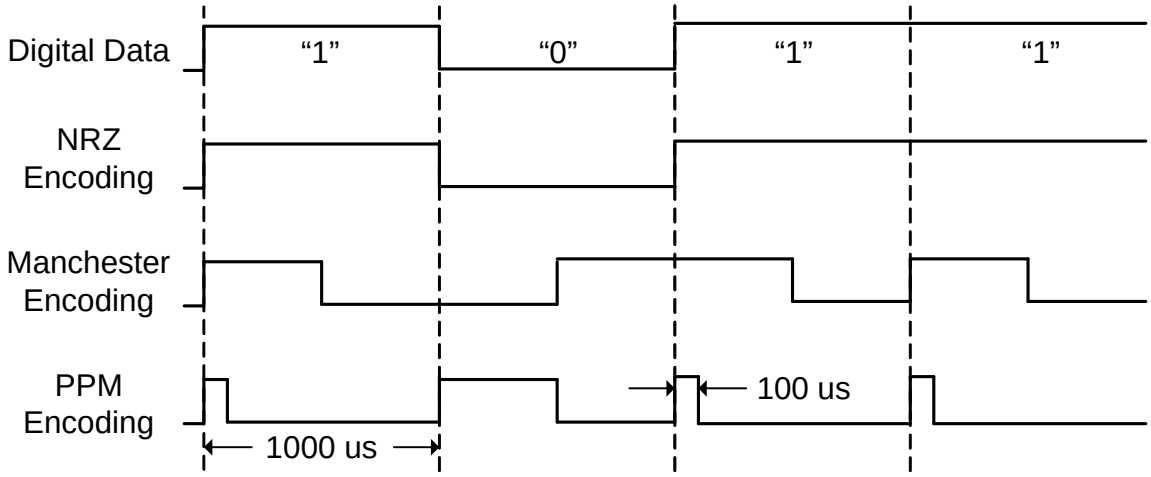


Figure 4. Example Data Waveforms

In order to set the data filter bandwidth correctly, the shortest pulse width of the transmitted encoded data should be chosen as the bit time. In the PPM example shown in Figure 4, the shortest pulse width is 100 µs; so, the bit time is chosen as BT = 100 µs even though the actual data rate is 1 kbps (1000 µs). After finding BT, Table 9 can be used to find the bit settings for pins 14 and 15, BT[1:0]. In this PPM example, BT[1:0] is set as logic BT1 = 1 and BT0 = 1 or BT[1:0] = (1,1) since BT = 100 µs.

Table 9. How to Choose BT[1:0] Based on the Bit Time

Bit Time [µs]	Filter Bandwidth [kHz]	BT1 (pin 14)	BT0 (pin 15)
BT ≥ 1000	1.5	0	0
1000 < BT ≤ 500	3.0	0	1
500 < BT ≤ 200	7.5	1	0
200 < BT ≤ 100	15	1	1

3.5. RATIO Selection Used for the Slicer Threshold Calculation Window

In OOK modulation, many different encoding schemes exist, which can result in variable ON and OFF times as seen in the example data waveforms shown in Figure 4. In order to determine the proper slicer threshold used for demodulating the OOK signal into digital data, the Si4312 must sample an "ON" and "OFF" event in a time window called the threshold calculation window. The samples during the "ON" time will determine the ON voltage, and the samples during the "OFF" time will determine the OFF voltage. These voltages are used to determine the slicer threshold voltage as follows:

$$\text{SlicerThreshold} = \frac{(\text{Max\_ON\_Voltage} + \text{Min\_OFF\_Voltage})}{2}$$

Defining the BT variable from the last section as the ON time and

$$\text{RATIO} = \frac{\text{OFF}}{\text{ON}}$$

then, the threshold calculation window is calculated as follows:

$$\begin{aligned}\text{Threshold Calculation Window} &= 1.25 \times (\text{ON} + \text{OFF}) \\ &= 1.25 \times (\text{BT} + \text{BT} \times \text{RATIO}) \\ &= 1.25 \times \text{BT}(\text{RATIO} + 1)\end{aligned}$$

The threshold calculation window is 1.25 times longer than the ON plus OFF times for margin to allow sampling of both ON and OFF times. Figure 5 shows a graph of the threshold calculation window.

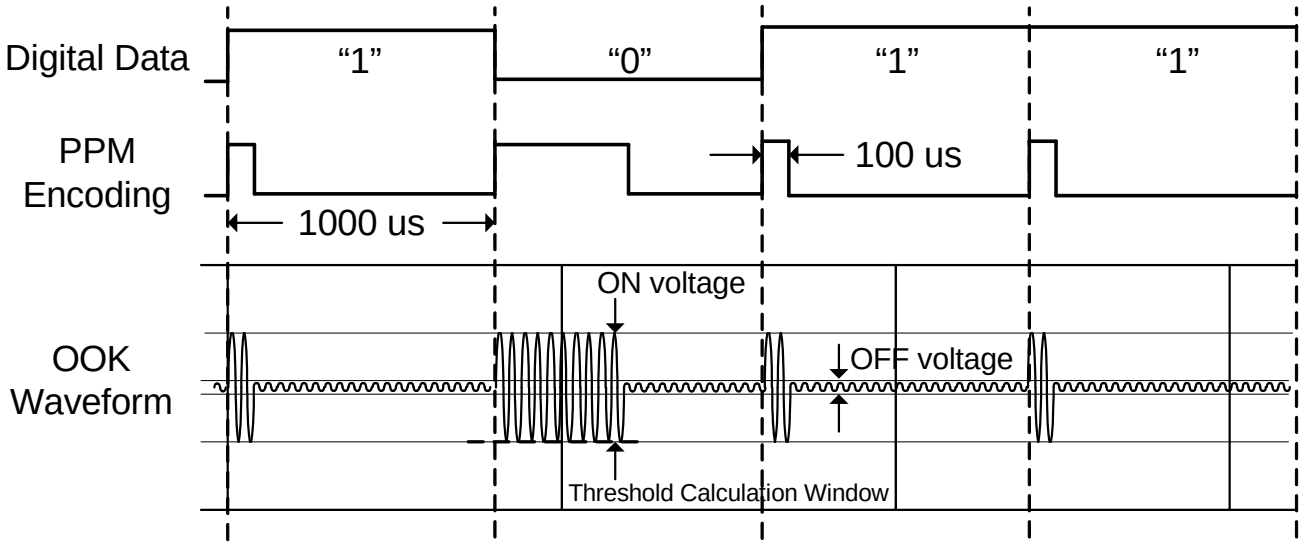


Figure 5. Example of the Threshold Calculation

Ratio is a unit-less multiplier that relates the OFF time to the ON time. The Si4312 defines two constants for RATIO as shown in Table 10 based on the logic level of pin 5.

Table 10. RATIO Constants Based on Logic Level of Pin 5

Pin 5	RATIO
0	5
1	10

Since the OFF time = RATIO x BT and the values for RATIO are either 5 or 10, RATIO should be chosen such that either the value of 5 or 10 x the BT[1:0] setting is just larger than the OFF time. For the PPM example shown in Figure 4, BT[1:0] = (1,1) since BT = 100 µs. The actual OFF time is 900 µs; so, we would set pin 5 = 1 to get a RATIO of 10 such that the calculated OFF time is BT[1:0] x RATIO = 100 µs x 10 = 1000 µs, which is greater than the actual OFF time of 900 µs.
An alternative approach to choosing the RATIO bit (pin 5) is to choose the RATIO parameter such that the threshold calculation window is greater than the actual ON plus OFF times using Table 11 and the values chosen for BT[1:0].

Table 11. Threshold Calculation Window Times Based on RATIO and BT[1:0] Settings

RATIO	BT1	BT0	Threshold Calculation Window (ms)
0	0	0	7.500
0	0	1	3.750
0	1	0	1.500
0	1	1	0.750
1	0	0	13.750
1	0	1	6.875
1	1	0	2.750
1	1	1	1.375

3.6. Frequency Scanning

The channel bandwidth directly affects the sensitivity of any wireless receiver. Typical analog OOK receivers use an external ceramic filter with a large bandwidth to accommodate the data rate, crystal tolerances, and transmit carrier frequency offsets, which leads to unnecessary amounts of noise and lower sensitivity levels. The Si4312 uses a narrow channel bandwidth of 160 kHz and frequency scanning to obtain excellent sensitivity levels (–110 dBm at data rate of 1 kbps at 315 MHz) while still accommodating up to ±210 kHz of scan bandwidth from its operating frequency.

The frequency scan algorithm works by breaking the scan bandwidth (420 kHz) into three frequency bins approximately 140 kHz wide and checking for transmit signal energy in each bin. Because the received signal power can vary by large orders of magnitude depending on how close the transmitter is to the receiver, the frequency algorithm may have to re-scan the frequency bins if the received power level saturates the receiver. Three gain settings are used in the frequency scan algorithm denoted as high-, medium-, and low-gain.

The chip begins scanning the frequency in the highest receiver gain setting to find signals that have a receive signal strength indicator (RSSI) level from sensitivity to about –70 dBm. If energy is detected in only one of these frequency bands, it is double-checked again and deemed as the correct operating frequency band. Therefore, the frequency scan algorithm takes at least two searches to find the correct frequency band. The scan time per frequency bin search is equal to the threshold calculation window time as chosen by the RATIO and BT[1:0] settings given in Table 11. Therefore, the best case frequency scan time is equal to two times the threshold calculation window time.

In case the input signal is large while the gain is also large, the receiver could be overloaded; therefore, the frequency scan algorithm follows a series of frequency and gain level settings based on measured RSSI as shown in Figure 6. In the worst case, there are a total of nine frequency bin searches (three frequency bins times three gain settings) plus one additional frequency re-scan because we don't know when the signal starts or for double checking. Thus, the worst-case scan time is equal to 10 times the threshold calculation window time. Figure 6 shows the frequency scan algorithm broken into three frequency bins of 140 kHz and three gain settings.

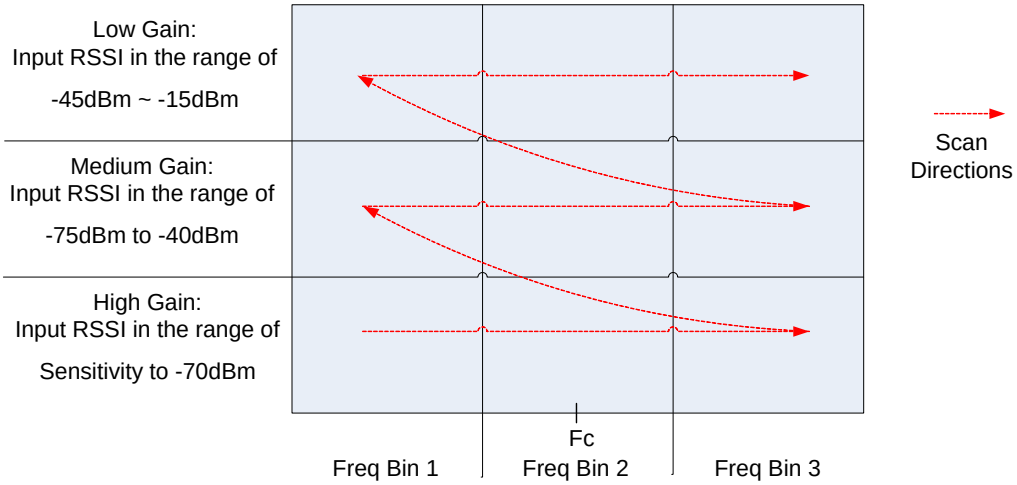


Figure 6. Frequency Scan Algorithm Depicting 3 Frequency Bins of 140 kHz and 3 Gain Settings

Frequency scanning is always enabled to find the transmitted signal. The scanning process stops after the correct frequency band is found for the transmitted signal and is held throughout the duration of the packet plus a time of no RF signal activity. This dead time is called “threshold hold time” and is described in section 3.7. Theshold hold time allows a frequency found in the first packet of transmission to be held for any subsequent retransmissions of packets if the retransmissions occur before the threshold hold time. This held frequency ensures all bits of the second and subsequent packets are recovered completely. Frequency scanning resumes after the time of no RF signal activity exceeds the threshold hold time.

3.7. Threshold Hold Time Selection

The threshold hold time is defined as the length of time the Si4312 keeps its slicer threshold voltage level when no signals are present. If a signal does not appear after this time interval, the Si4312 will re-start the frequency scan process and look for the signal in one of its three frequency bins. The threshold hold times are determined by the bit settings chosen on pins 16 and 17 as shown in Table 12.

Table 12. Threshold Time Settings Based on TH[1:0] Logic Levels

TH1 (Pin 16)	TH0 (Pin 17)	Threshold Hold Time (ms)
0	0	70
0	1	100
1	0	300
1	1	500

3.8. Low Noise Amplifier Input Circuit

Figure 2 shows the typical application circuit with 50 Ω matching. Components C3 and L1 are used to transform the input impedance of the LNA. C3 is equal to 15 pF and L1 is equal to 33 nH at 433.92 MHz and 62 nH at 315 MHz for 50 Ω matching.

3.9. Crystal Oscillator

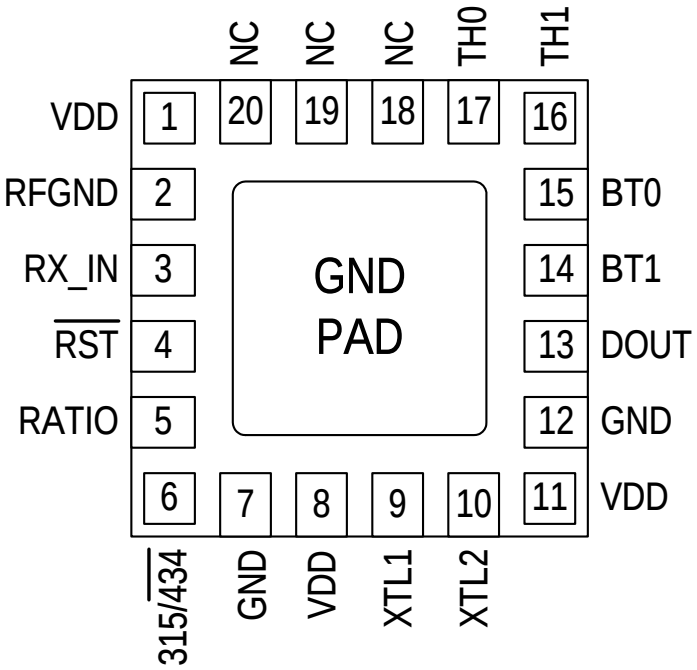
An on-board crystal oscillator is used to generate a 16 MHz reference clock for the Si4312. This reference frequency is required for proper operation of the Si4312 and is used for calibration of the on-chip VCO and other timing references. No external load capacitors are required to set the 16 MHz reference frequency if the recommended crystal load capacitor is around 14 pF, assuming the effective board capacitance between pins XTL1 and XTL2 is 3 pF and the chip input capacitance on pins XTL1 or XTL2 is 11 pF. Refer to Table 6, “Crystal Characteristics,” on page 6 for board capacitance and frequency tolerance information. The frequency tolerance of the crystal should be chosen such that the received signal is within the IF bandwidth of the Si4312 receiver.

Additionally, the Si4312 can be driven by an external 16 MHz reference clock. The clock signal can be applied to either the XTL1 or XTL2 inputs. When the 16 MHz reference clock is applied to one of the inputs, the other crystal input pin must be floating.

3.10. Reset Pin

Driving the $\overline{\text{RST}}$ pin (pin 4) low will disable the Si4312 and place the device into reset mode. All active blocks in the device are powered off in this mode, bringing the current consumption to less than 10 uA. The Si4312 is enabled by driving the $\overline{\text{RST}}$ pin (pin 4) to VDD. Refer to Table 4 "Reset Timing Characteristics" for the reset timing requirements. The chip requires about 500 ms to go from reset to active mode. The Si4312 can output invalid data during the 500 ms turn-on time.

4. Pin Descriptions: Si4312-B10-GM



Pin Number(s)	Name	Description
1, 8, 11	VDD	Supply voltage, may connect to external battery.
2	RFGND	RF ground. Connect to ground plane on PCB.
3	RX_IN	RF receiver input.
4	$\overline{\text{RST}}$	Device reset, active low input.
5	RATIO	Constant used to determine threshold calculation window, input pin.
6	315/$\overline{434}$	Selectable logic input for 315 or 433.92 MHz operation.
7, 12, GND PAD	GND	Ground. Connect to ground plane on PCB.
9	XTL1	Crystal input.
10	XTL2	Crystal input.
13	DOUT	Data output.
14, 15	BT[1:0]	Bit time selection input pins.
16, 17	TH[1:0]	Threshold hold time selection input pins.
18,19,20	NC	No connect. Leave floating.

5. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4312-B10-GM	315/433.92 MHz OOK Receiver	QFN Pb-free	–40 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option.			

6. Package Markings (Top Marks)

6.1. Si4312 Top Mark

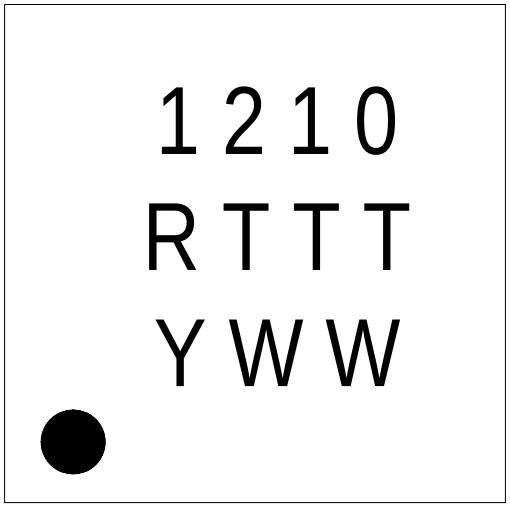


Figure 7. Si4312 Top Mark Example

6.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	12 = Si4312
	Firmware Revision	10 = Firmware Revision 1.0
Line 2 Marking:	Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	YWW = Date Code	Assigned by the Assembly House. Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date.

7. Package Outline: Si4312-B10-GM

Figure 8 illustrates the package details for the Si4312-B10-GM. Table 13 lists the values for the dimensions shown in the illustration.

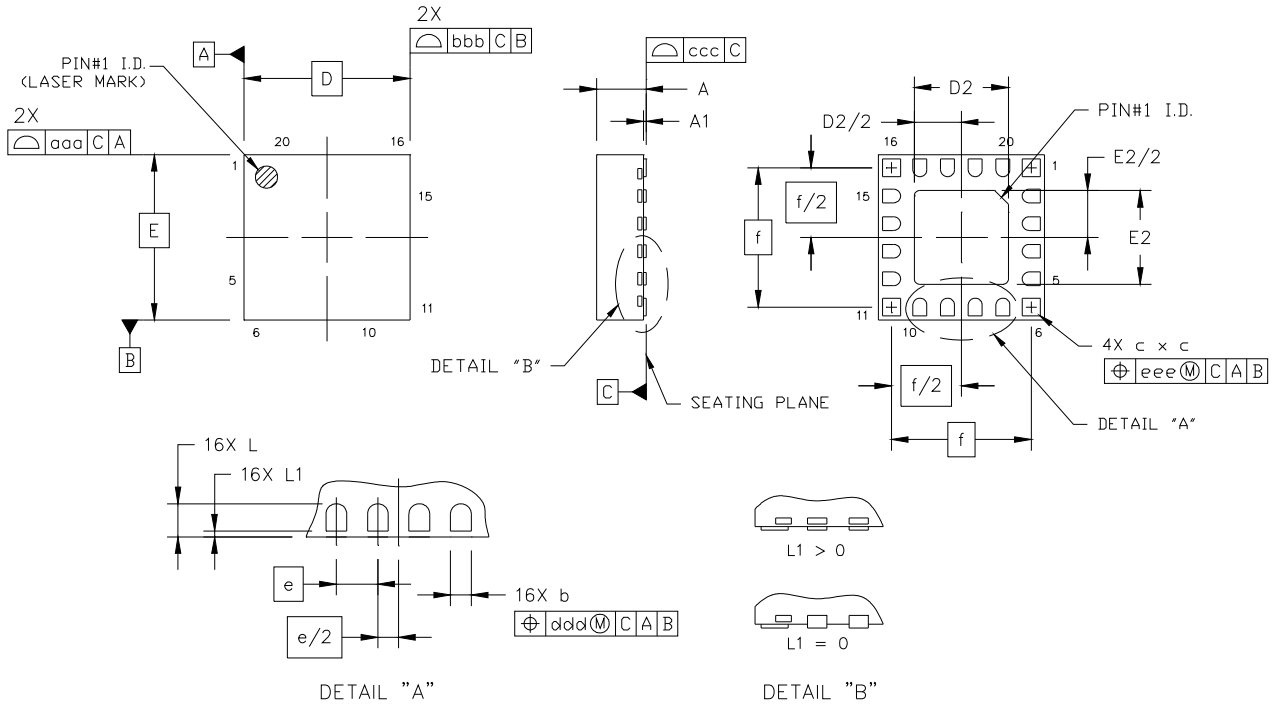


Figure 8. 20-Pin Quad Flat No-Lead (QFN)

Table 13. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.30	0.35	0.40
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

8. PCB Land Pattern: Si4312-B10-GM

Figure 9 illustrates the PCB land pattern details for the Si4312-B10-GM. Table 14 lists the values for the dimensions shown in the illustration.

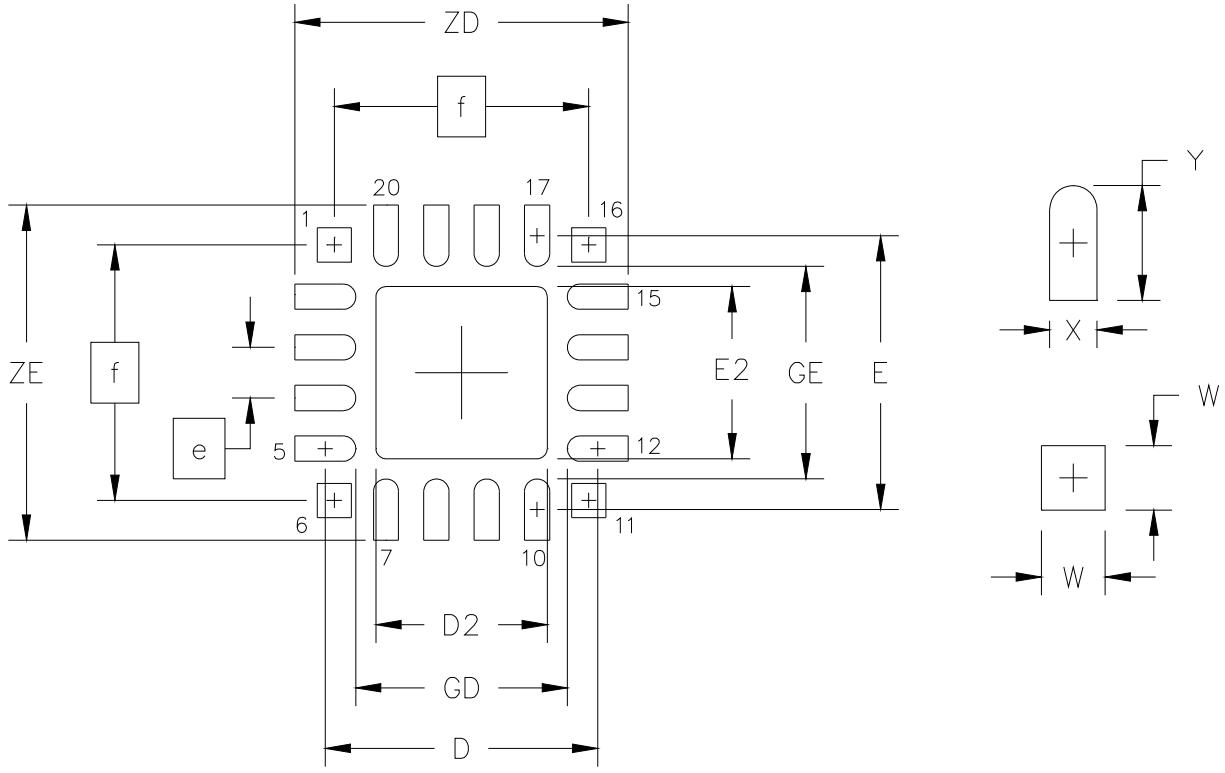


Figure 9. PCB Land Pattern

Table 14. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

NOTES:

DOCUMENT CHANGE LIST

Revision 0.1 to 0.2

- Updated sensitivity and supply current.

Revision 0.2 to 0.5

- Removed I_{VDD} current spec when input = –30 dBm from Table 3 "DC Characteristics"
- Updated sensitivity specs and test conditions in Table 5 "Si4312 Receiver Characteristics"
- Updated frequency scanning description in section “3.6. Frequency Scanning”
- Added reference clock drive capability to section “3.9. Crystal Oscillator”

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: wireless@silabs.com
Internet: www.silabs.com