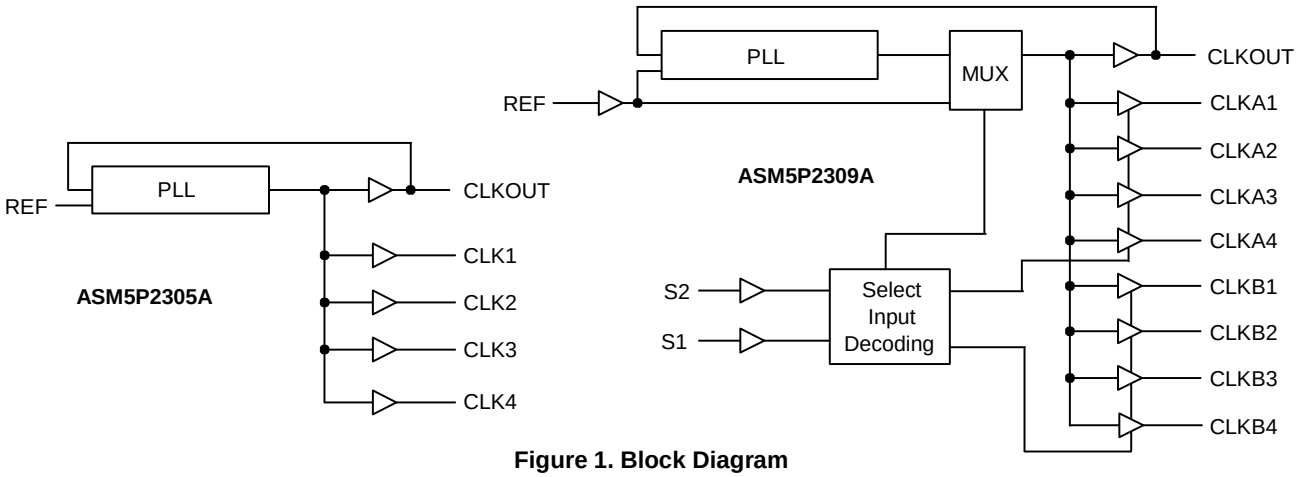


Figure 1. Block Diagram

Table 1. SELECT INPUT DECODING FOR ASM5P2309A

S2	S1	Clock A1 − A4	Clock B1 − B4	CLKOUT (Note 1)	Output Source	PLL Shut−Down
0	0	Three−state	Three−state	Driven	PLL	N
0	1	Driven	Three−state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the output.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input−output delay.

For applications requiring zero input−output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero input−output delay.

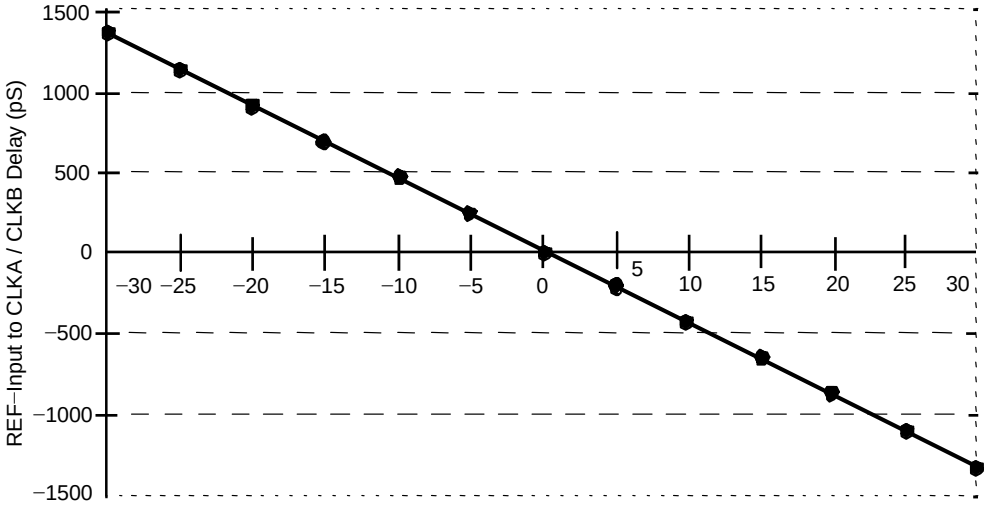


Figure 2. Output Load Difference: CLKOUT Load − CLKA/CLKB Load (pF)

Table 2. PIN DESCRIPTION FOR ASM5P2305A

Pin #	Pin Name	Description
1	REF (Note 2)	Input reference clock frequency, 5 V−tolerant input
2	CLK2 (Note 3)	Buffered clock output
3	CLK1 (Note 3)	Buffered clock output
4	GND	Ground
5	CLK3 (Note 3)	Buffered clock output
6	V_{DD}	3.3 V supply
7	CLK4 (Note 3)	Buffered clock output
8	CLKOUT (Note 3)	Buffered clock output, internal feedback on this pin

Table 3. PIN DESCRIPTION FOR ASM5P2309A

Pin #	Pin Name	Description
1	REF (Note 2)	Input reference clock frequency, 5 V tolerant input
2	CLKA1 (Note 3)	Buffered clock output, bank A
3	CLKA2 (Note 3)	Buffered clock output, bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1 (Note 3)	Buffered clock output, bank B
7	CLKB2 (Note 3)	Buffered clock output, bank B
8	S2 (Note 4)	Select input, bit 2
9	S1 (Note 4)	Select input, bit 1
10	CLKB3 (Note 3)	Buffered clock output, bank B
11	CLKB4 (Note 3)	Buffered clock output, bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3 (Note 3)	Buffered clock output, bank A
15	CLKA4 (Note 3)	Buffered clock output, bank A
16	CLKOUT (Note 3)	Buffered output, internal feedback on this pin

2. Weak pull−down.
3. Weak pull−down on all outputs.
4. Weak pull−up on these inputs.

Table 4. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.5	+4.6	V
DC Input Voltage (Except REF)	−0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	−0.5	7	V
Storage Temperature	−65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22− A114−B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. OPERATING CONDITIONS (for ASM5P2305A (−1, −1H) and ASM5P2309A (−1, −1H))

Parameter	Description		Min	Max	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	Commercial temperature	0	70	°C
		Industrial temperature	−40	85	
C_L	Load Capacitance, below 100 MHz			30	pF
	Load Capacitance, from 100 MHz to 133 MHz			10	pF
C_{IN}	Input Capacitance			7	pF

Table 6. ELECTRICAL CHARACTERISTICS (for ASM5P2305A (−1, −1H) and ASM5P2309A (−1, −1H))

Parameter	Description		Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage (Note 5)					0.8	V
V_{IH}	Input HIGH Voltage (Note 5)			2.2			V
I_{IL}	Input LOW Current		V_{IN} = 0 V			50	μA
I_{IH}	Input HIGH Current		V_{IN} = V_{DD}			100	μA
V_{OL}	Output LOW Voltage (Note 6)		I_{OL} = 8 mA (−1) I_{OL} = 12 mA (−1H)			0.4	V
V_{OH}	Output HIGH Voltage (Note 6)		I_{OH} = −8 mA (−1) I_{OH} = −12 mA (−1H)	2.4			V
I_{DD}	Supply Current	Commercial temp.	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}			30	mA
		Industrial temp.				32	

5. REF input has a threshold voltage of V_{DD} /2.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. SWITCHING CHARACTERISTICS (for ASM5P2305A (−1, −1H) and ASM5P2309A (−1, −1H) (Notes 7, 8)

Parameter	Test Conditions		Min	Typ	Max	Unit
Output Frequency	30 pF load 10 pF load		10 10		100 133	MHz
Duty Cycle (Note 9)	Measured at 1.4 V, F_{OUT} > 50 MHz		40	50	60	%
	Measured at V_{DD} /2, F_{OUT} ≤ 50 MHz		45	50	55	
Output Rise Time (Note 9)	Measured between 0.8 V and 2.0 V	(−1)			2.25	nS
		(−1H)		1.5	2	
Output Fall Time (Note 9)	Measured between 2.0 V and 0.8 V	(−1)			2.25	nS
		(−1H)		1.5	2	
Output−to−output skew (Note 9)	All outputs equally loaded				200	pS
Delay, REF Rising Edge to CLKOUT Rising Edge (Note 9)	Measured at V_{DD} /2			0	±350	pS
Device−to−Device Skew (Note 9)	Measured at V_{DD}/2 on the CLKOUT pins of the device			0	700	pS
Cycle−to−cycle Jitter (Note 9)	Measured at 66.67 MHz, loaded outputs				200	pS
PLL Lock Time (Note 9)	Stable power supply, valid clock presented on REF pin				1.0	mS

7. For all measurements use Test Circuit #1.
8. All parameters are specified with loaded outputs.
9. Parameter is guaranteed by design and characterization. Not 100% tested in production.

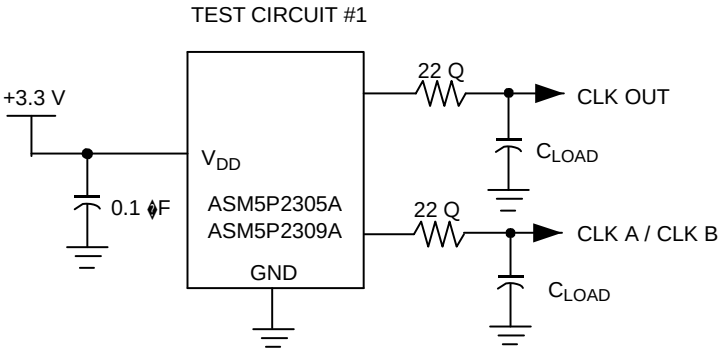


Figure 3. Test Circuit

Switching Waveforms

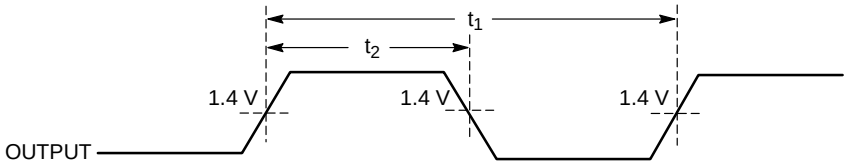


Figure 4. Duty Cycle Timing

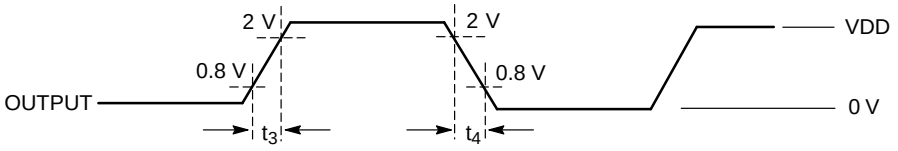


Figure 5. All Outputs Rise/Fall Time

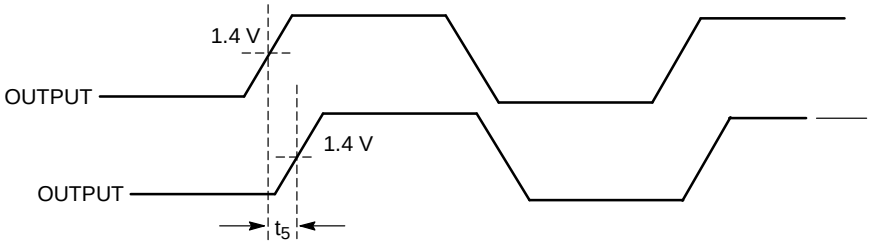


Figure 6. Output−Output Skew

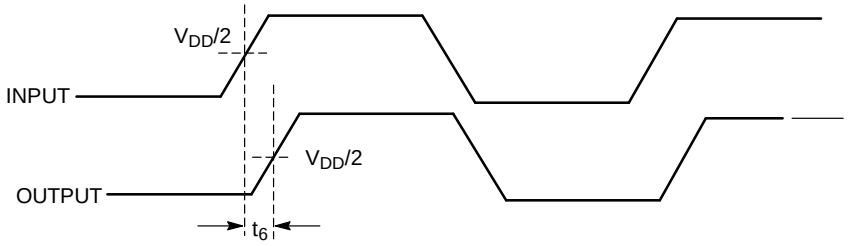


Figure 7. Input−Output Propagation Delay

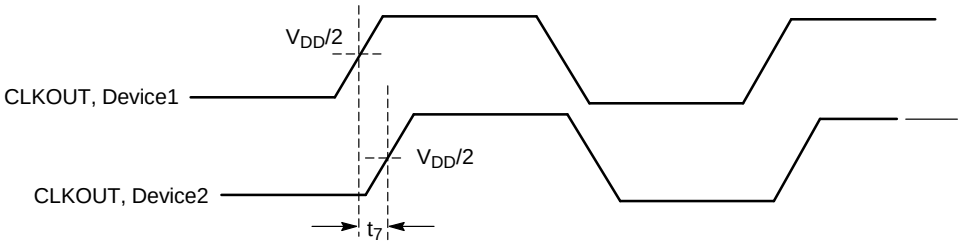
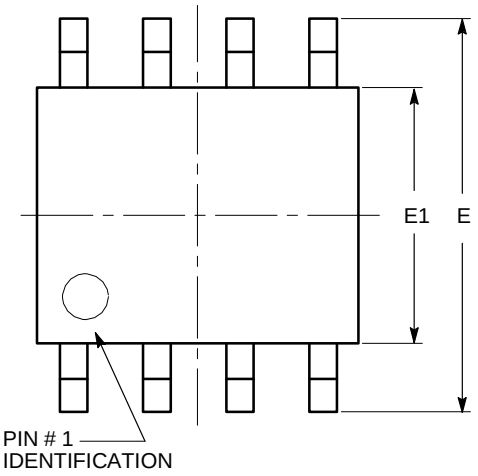


Figure 8. Device−Device Skew

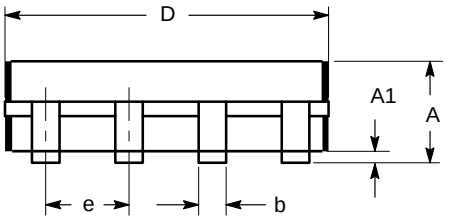
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

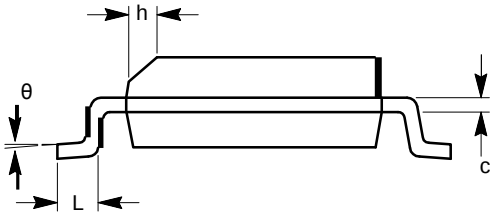


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

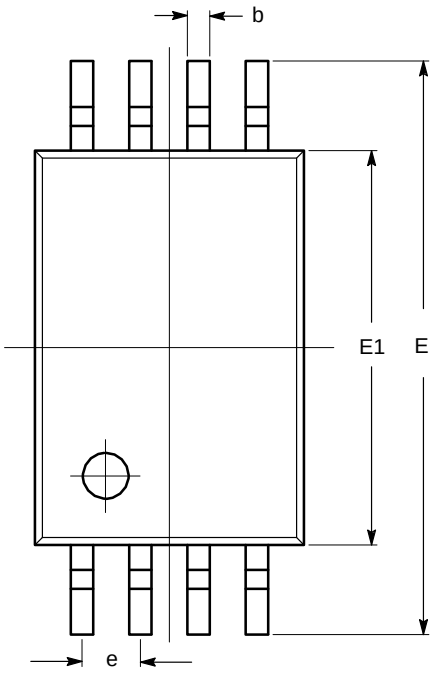


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

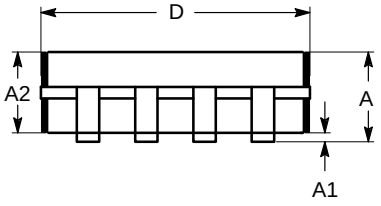
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

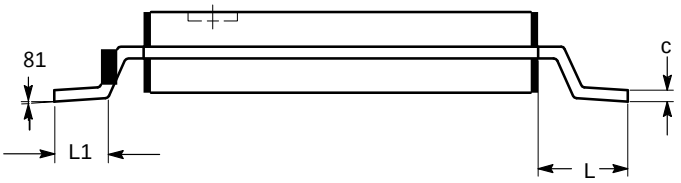


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW

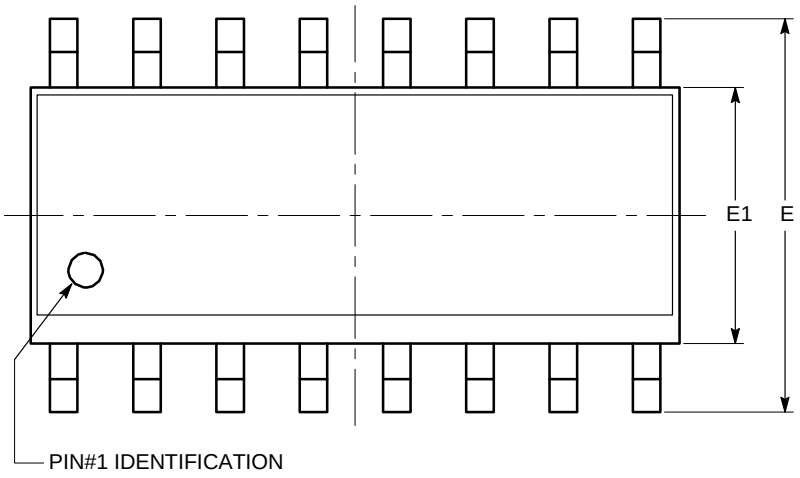


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

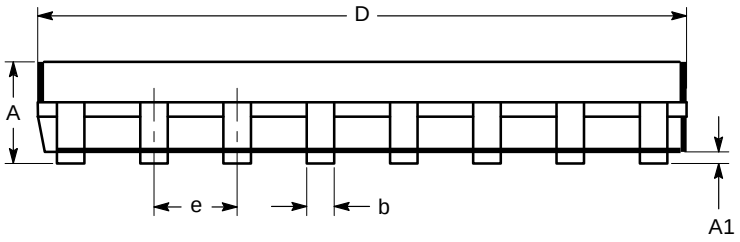
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

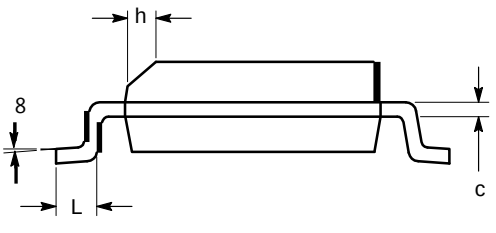


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

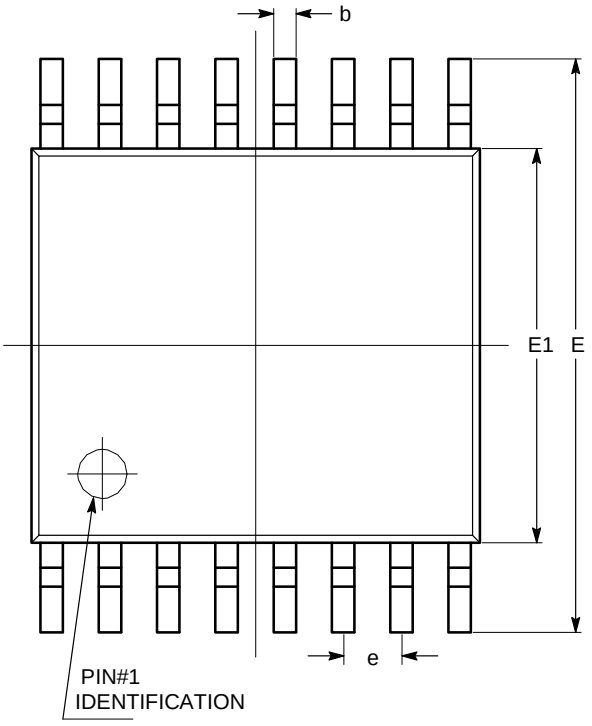


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

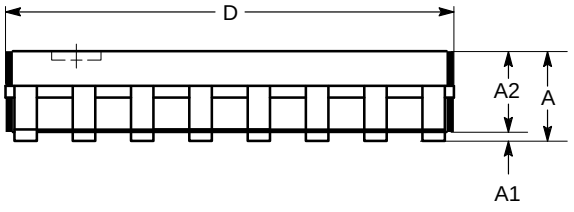
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

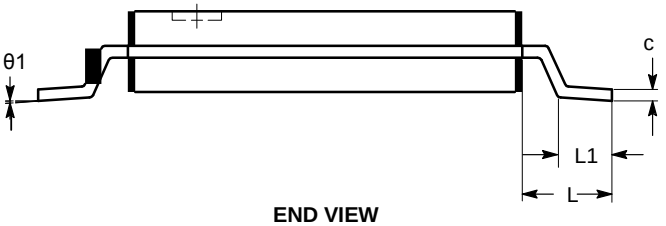


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0º		8º



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
P5P2309AF−1−16ST	5P2309AF−1	16−pin 150−mil SOIC−TUBE,Pb Free	Commercial
P5I2309AF−1−16ST	5I2309AF−1	16−pin 150−mil SOIC− TUBE,Pb Free	Industrial
P5P2309AF−116SR	5P2309AF−1	16−pin 150−mil SOIC−TAPE & REEL,Pb Free	Commercial
P5I2309AF−116SR	5I2309AF−1	16−pin 150−mil SOIC−TAPE & REEL,Pb Free	Industrial
P5P2309AF−1−16TT	5P2309AF−1	16−pin 4.4−mm TSSOP − TUBE,Pb Free	Commercial
ASM5I2309AF−1−16−TT	5I2309AF−1	16−pin 4.4−mm TSSOP − TUBE,Pb Free	Industrial
P5P2309AF−1−16TR	5P2309AF−1	16−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Commercial
ASM5I2309AF−1−16−TR	5I2309AF−1	16− pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Industrial
P5P2309AF−1H16ST	5P2309AF−1H	16−pin 150−mil SOIC−TUBE,Pb Free	Commercial
ASM5I2309AF−1H−16−ST	5I2309AF−1H	16−pin 150−mil SOIC− TUBE,Pb Free	Industrial
P5P2309AF−1H16SR	5P2309AF−1H	16−pin 150−mil SOIC−TAPE & REEL,Pb Free	Commercial
ASM5I2309AF−1H−16−SR	5I2309AF−1H	16−pin 150−mil SOIC−TAPE & REEL,Pb Free	Industrial
ASM5P2309AF−1H−16−TT	5P2309AF−1H	16−pin 4.4−mm TSSOP − TUBE,Pb Free	Commercial
ASM5I2309AF−1H−16−TT	5I2309AF−1H	16−pin 4.4−mm TSSOP − TUBE,Pb Free	Industrial
P5P2309AF−1H16TR	5P2309AF−1H	16−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Commercial
ASM5I2309AF−1H−16−TR	5I2309AF−1H	16−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Industrial
P5P2305AF−1−08ST	5P2305AF−1	8−pin 150−mil SOIC−TUBE,Pb Free	Commercial
P5I2305AF−108ST	5I2305AF−1	8−pin 150−mil SOIC− TUBE,Pb Free	Industrial
P5P2305AF−1−08SR	5P2305AF−1	8−pin 150−mil SOIC−TAPE & REEL,Pb Free	Commercial
ASM5I2305AF−1−08−SR	5I2305AF−1	8−pin 150−mil SOIC−TAPE & REEL,Pb Free	Industrial
ASM5P2305AF−1−08−TT	5P2305AF−1	8−pin 4.4−mm TSSOP − TUBE,Pb Free	Commercial
ASM5I2305AF−1−08−TT	5I2305AF−1	8−pin 4.4−mm TSSOP − TUBE,Pb Free	Industrial
ASM5P2305AF−1−08−TR	5P2305AF−1	8−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Commercial
ASM5I2305AF−1−08−TR	5I2305AF−1	8−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Industrial
ASM5P2305AF−1H−08−ST	5P2305AF−1H	8−pin 150−mil SOIC−TUBE,Pb Free	Commercial
P5I2305AF−1H08ST	5I2305AF−1H	8−pin 150−mil SOIC− TUBE,Pb Free	Industrial
P5P2305AF−1H08SR	5P2305AF−1H	8−pin 150−mil SOIC−TAPE & REEL,Pb Free	Commercial
P5I2305AF−1H08SR	5I2305AF−1H	8−pin 150−mil SOIC−TAPE & REEL,Pb Free	Industrial
ASM5P2305AF−1H−08−TT	5P2305AF−1H	8−pin 4.4−mm TSSOP − TUBE,Pb Free	Commercial
ASM5I2305AF−1H−08−TT	5I2305AF−1H	8−pin 4.4−mm TSSOP − TUBE,Pb Free	Industrial
P5P2305AF−1H08TR	5P2305AF−1H	8−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Commercial
P5I2305AF−1H08TR	5I2305AF−1H	8−pin 4.4−mm TSSOP − TAPE & REEL,Pb Free	Industrial

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