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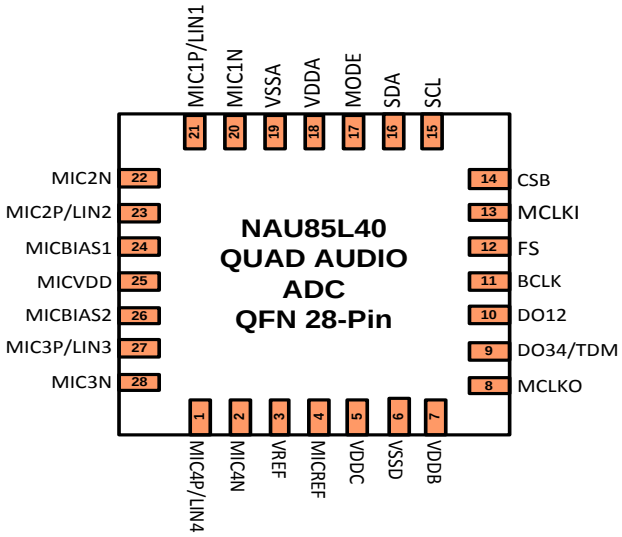
Pin Diagram



Pin Description

Pin #	Name	Type	Functionality
1	MIC4P/LIN4	Analog Input	MICP Input 4 / Line In Input 4
2	MIC4N	Analog Input	MICN Input 4
3	VREF	Reference	Decoupling for Mid-rail Reference Voltage
4	MICREF	Analog Output	Decoupling for MIC Reference Voltage
5	VDDC	Supply	Digital Core Supply
6	VSSD	Supply	Digital Ground
7	VDDB	Supply	Digital Buffer (Input/Output) Supply
8	MCLKO	Digital Output	Output from PLL
9	DO34	Digital Output	Digital Audio ADC Data Output for ADC 3 and 4 or TDM
10	DO12	Digital Output	Digital Audio ADC Data Output for ADC 1 and 2
11	BCLK	Digital I/O	Digital Audio Bit Clock
12	FS	Digital I/O	Digital Audio Frame Sync
13	MCLKI	Digital Input	Master Clock Input
14	CSB	Digital Input	SPI 3-Wire MPU Chip Select/I2C address LSB
15	SCL	Digital Input	SPI 3-Wire MPU Clock Input/I2C Clock (SCL).
16	SDA	Digital I/O	SPI 3-Wire MPU Data Input/I2C Data I/O (SDA).
17	MODE	Digital Input	Control Interface Mode Selection Pin (I2C=1, SPI=0)
18	VDDA	Supply	Analog Power Supply
19	VSSA	Supply	Analog Ground
20	MIC1N	Analog Input	MICN Input 1

21	MIC1P/LIN1	Analog Input	MICP Input 1 / Line In Input 1
22	MIC2N	Analog Input	MICN Input 2
23	MIC2P/LIN2	Analog Input	MICP Input 2 / Line In Input 2
24	MICBIAS1	Analog Output	Microphone Bias for Microphone ADC 1 and 2
25	MICVDD	Supply	Microphone Supply
26	MICBIAS2	Analog Output	Microphone Bias for Microphone ADC 3 and 4
27	MIC3P/LIN3	Analog Input	MICP Input 3 / Line In Input 3
28	MIC3N	Analog Input	MICN Input 3

Electrical Characteristics

Conditions: VDDA = VDDC=1.8V, VDDB = 3.3V, MICVDD=3.3V, MCLK = 12.88MHz, T_A = +25°C, 1 kHz signal, Fs = 48 kHz, 24-bit audio data, with differential inputs unless otherwise stated.

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ADC					
THD+N ADC Total Harmonic Distortion + Noise		MIC Input, MIC_GAIN = 6dB, VIN = 0.8Vrms, f=1KHz, Fs = 16KHz, OSR=128X	90		dB
		Reference= @ 0dB gain, 0.8Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x	91		dB
SNR Signal to Noise Ratio		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 8KHz, Mono Differential Input	100		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8KHz, Mono Differential Input	98		dB
		Reference = VOUT(0dBFS), A-Weighted, Quad Input, Gain = 12dB,fs = 16KHz	96		dB
		Reference= MIC Gain= 0dB gain, (A-weighted) VDDA=1.8V, Fs = 48 kHz, OSR=128x	101		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVP_P applied to AVDD, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	65		dB
Xtalk	ADC channel cross talk	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1KHz, Fs = 48KHz , Channel 1(3) to Channel 2 (4)	-124		dB
FS_{ADC}	ADC Full Scale Input Level	AV_{DD} = 1.8V	1		V_{RMS}
MICBIAS					
V_{BIAS}	Output Voltage	Programmable 2.1V to 2.8V in 0.1V Steps	2.5		V
I_{OUT}	Output Current			4	mA

e_{OS}	Output Noise	A-weighted 20Hz-20kHz	-115		dBV

Notes

1. Full Scale input level is relative to the magnitude of VDDA and can be calculated as FS = $1V_{rms}$*VDDA/1.8.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Unused analog input pins should be left as no-connection.
4. Unused digital input pins should be tied to ground.

Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	VDDB = 1.8V			0.33 * VDDB	V
		VDDB = 3.3V			0.37 * VDDB	
Input HIGH level	V_{IH}	VDDB = 1.8V		0.57 * VDDB		V
		VDDB = 3.3V		0.63 * VDDB		
Output HIGH level	V_{OH}	I_{Load} = 1mA	VDDB = 1.8V	0.9 * VDDB		V
			VDDB = 3.3V	0.95 * VDDB		
Output LOW level	V_{OL}	I_{Load} = 1mA	VDDB = 1.8V		0.1 * VDDB	V
			VDDB = 3.3V		0.05 * VDDB	

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital Supply Range with sample rate > 48 kHz or FLL enabled	VDDC	1.62	1.8	1.98	V
Digital Supply Range with sample rate <= 48kHz and FLL disabled	VDDC	1.2	1.8	1.98	V
Digital I/O Supply Range	VDDB	1.62	1.8	3.6	V
Analog Supply Range	VDDA	1.62	1.8	1.98	V
Microphone Bias Supply Voltage	VDDMIC	2.5	4.2	5.5	V
Temperature Range	T_A	-40		+85	°C

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Range (VDDC)	-0.3	2.2	V
Digital I/O Supply Range (VDDB)	-0.3	6.0	V
Analog Supply Range (VDDA)	-0.3	2.2	V
Microphone Bias Supply Voltage (MICVDD)	-0.3	6.0	V
Voltage Input Digital Range	VSSD - 0.3	VDDB + 0.3	V
Voltage Input Analog Range	VSSA - 0.3	VDDA + 0.3	V

Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

1 General Description

The NAU85L40 is a low power, high quality, 4-channel ADC for microphone array applications. There are eight analog inputs with individual input PGA gain stages that are passed to the ADC path for signal processing. A low noise microphone bias circuit supplies a programmable voltage reference for one or more electret microphones on two buffered MICBIAS outputs, these are available to separately supply microphones associated with channels 1 & 2 and channels 3 & 4. The digital audio data from the ADC's can be processed by a Volume Control, High Pass filter, and ALC before it is passed on to the serial I2S or TDM PCM interface. This digital serial output data can be available in two separate dual channel formats on ADCOUT12 for channel 1 & 2 and ADCOUT34 for channel 3 & 4. The 4-channel serial digital audio can also be combined into one serial bit stream on ADCOUT34 in TDM mode. The device clock can be locked to an external clock reference or generated internally by the on-chip FLL. The registers that control the NAU85L40 can be programmed through standard I2C or SPI interface.

2 Analog Inputs

NAU85L40 has four low noise, high common mode rejection ratio analog microphone differential inputs – MIC1/MIC1P together are MIC.1, MIC2N/MIC2P together are MIC.2, MIC3N/MIC3P together are MIC.3, MIC4N/MIC4P together are MIC.4. Each of these microphone inputs are followed by a -1dB to 36dB PGA gain stage with a fixed 12kOhm input impedance.

All inputs are maintained at a DC bias at approximately 1/2 of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs are also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

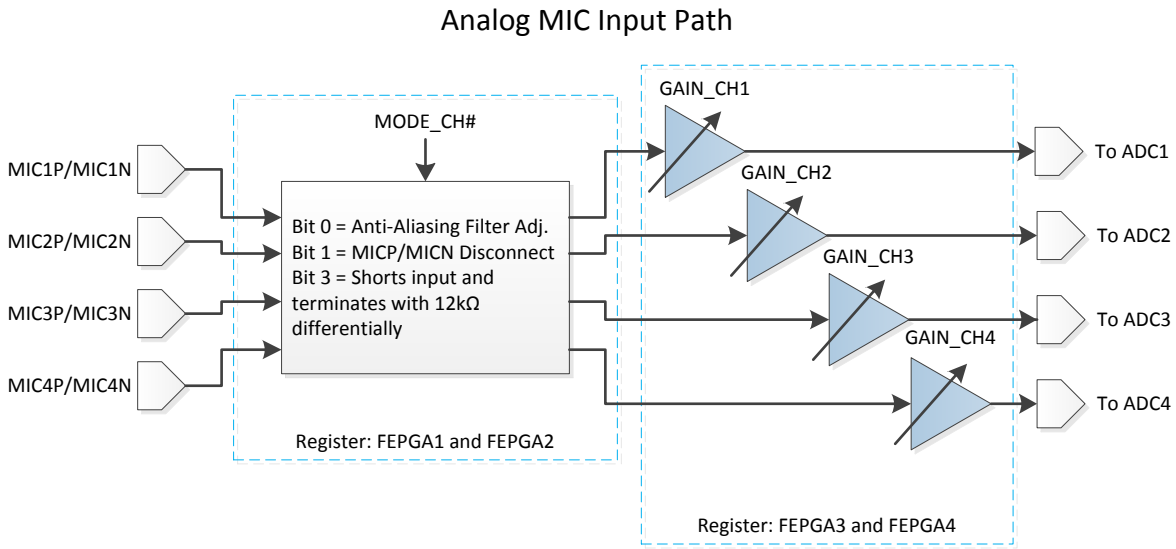


Figure 1: Analog Input Structure

2.1 ADC and Digital Signal Processing

The NAU85L40 has four independent high quality ADCs. These are high performance 24-bit sigma-delta converters that are suitable for a very wide range of applications. All digital processing is with 24-bit precision minimizing processing artifacts and maximizing the audio dynamic range supported by the NAU84L04.

The ADCs are supported by a wide range mixed-mode Automatic Level Control (ALC), a high pass filter, and a notch filter. All of which are optional and programmable. The high pass filter function is intended for DC-blocking or low frequency noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed to greatly reduce a specific frequency band or frequency, such as a 50Hz, 60Hz, or 217Hz unwanted noise. The 4-channel ADC TDM interface also provides for flexible routing options.

2.2 ADC Digital Block

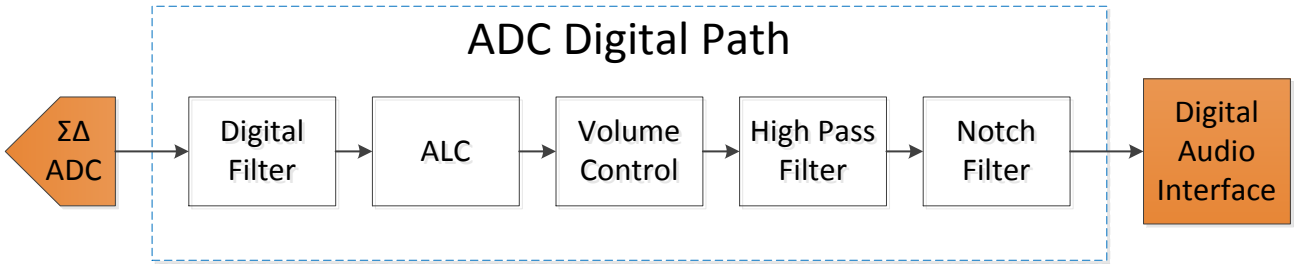


Figure 2: ADC Digital Path

The ADC digital block performs 24-bit analog-to-digital conversion and signal processing, making available a high quality audio sample stream for the audio path digital interface. This block consists of a sigma-delta modulator, digital decimator/ filter, ALC, volume control, high pass filter, and a notch filter.

The polarity of either ADC output signal can be changed independently on either ADC logic output which can be sometimes useful in management of the audio phase. This feature can help minimize any audio

processing that may be otherwise required as the data are passed to other stages in the system. The ADC coding scheme is in two's complement format and the full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0VRMS.

2.2.1 Input Limiter / Automatic Level Control (ALC)

The ADC digital path of the NAU85L40 is supported by the digital Automatic Level Control (ALC) function. This can be used to automatically manage the gain to optimize the signal level at the output of the ADC by automatically amplifying input signals that are too small or decreasing the amplitude of the signals that are too loud.

The ALC monitors the output of the ADC, measured after the digital decimator. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. The peak value is then used by a logic algorithm to determine whether the gain should be increased, decreased, or remain the same.

In normal mode, when sudden peaks occur above the desired gain settings, the ALC reduces volume at a register determined rate and step size. This continues until the output level of the ADC is again at the desired target level. If the input signal suddenly becomes quiet, the ALC increases volume at a register determined rate and step size until the output level from the ADC reaches the target level. If the input gain stays within the target level, the ALC will remain in a steady state.

In addition to the normal operation mode, the ALC may be operated in a special limiter mode that functions similarly to the normal mode but with faster attack times. This mode is primarily used to quickly ramp down signals that are too loud.

2.2.1.1 ALC Peak Limiter Function

Both normal and limiter mode include a peak limiter function. This implements an emergency gain reduction when the ADC output level exceeds a set gain value. When the ADC output exceeds 87.5% of full scale, the ALC block ramps down the gain at the maximum ALC Attack Time rate. This is regardless of the mode and attack rate settings. This continues until the ADC output level has been reduced to below the emergency limit threshold. This action limits ADC clipping if there is a sudden increase in the input signal level.

2.2.1.2 ALC Parameter Definitions

ALC Maximum Gain (ALCMAX): This sets the maximum allowed gain during normal mode ALC operation. In the Limiter mode of ALC operation, the ALCMXGAIN value is not used, instead, the maximum gain allowed is set equal to the pre-existing gain value that was in effect at the moment in time that the Limiter mode is enabled.

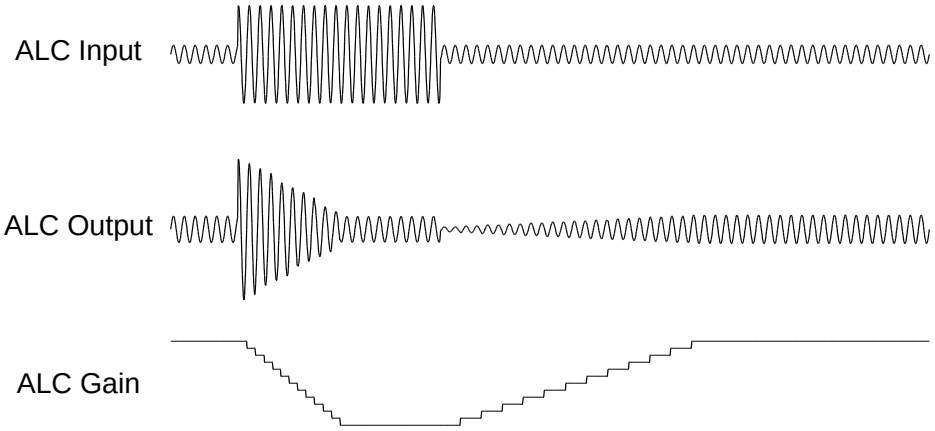


Figure 3: ALC Operation

2.2.1.3 ALC Normal Mode Example Using ALC Hold Time Feature

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimum performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings. Having a shorter hold time may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes.

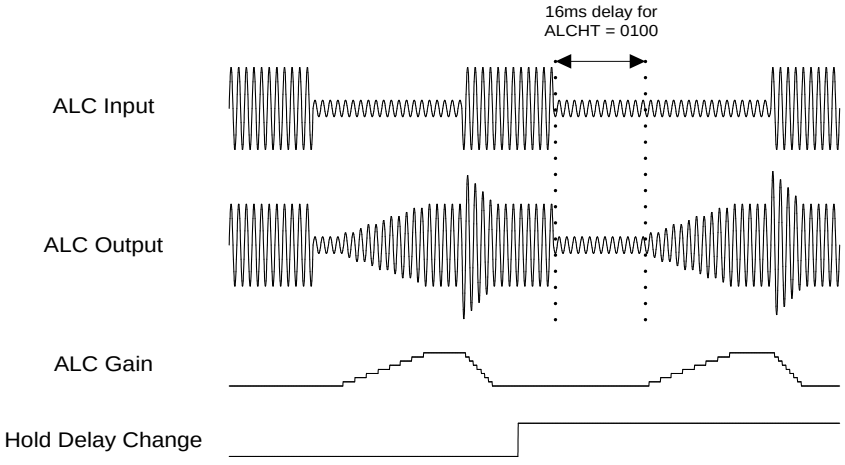


Figure 4: ALC using Hold time

2.2.1.4 Noise Gate (Normal Mode Only)

A noise gate threshold prevents ALC amplification of noise when there is no input signal or no signal above an expected background noise level. The NAU85L40 accomplishes this by comparing the input signal level against the noise gate threshold. The noise gate only operates in conjunction with the ALC and only in Normal mode.

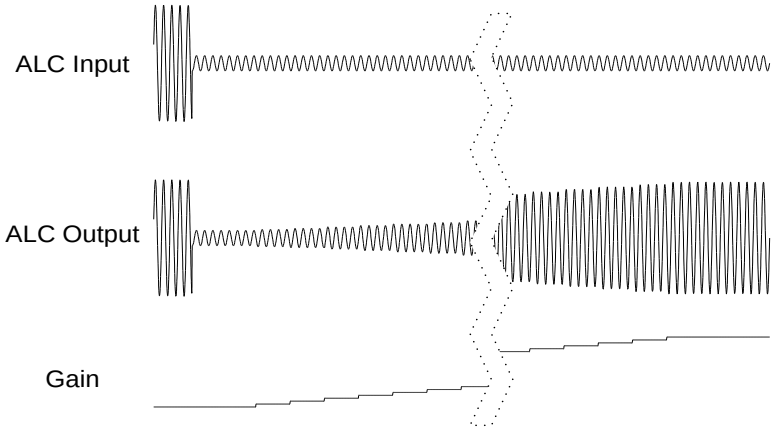


Figure 5: ALC without Noise gate

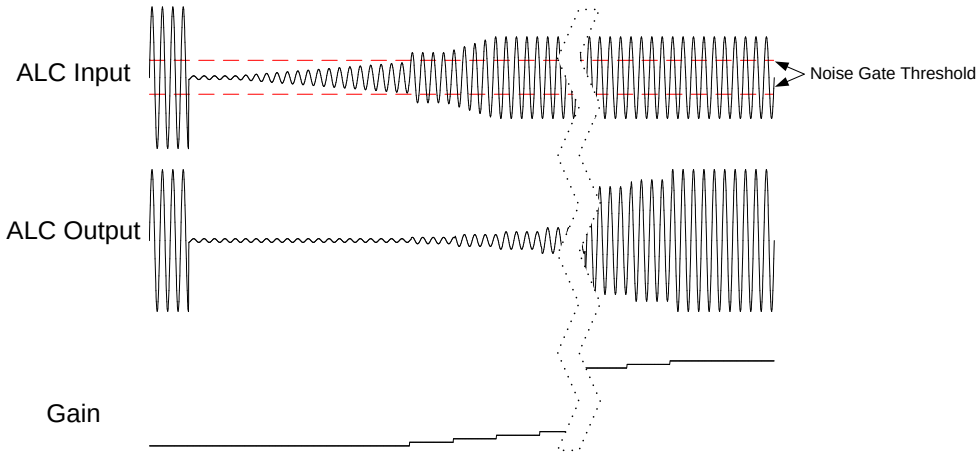


Figure 6: ALC with noise gate

2.2.2 ADC Digital Volume Control

The effective output audio volume of each ADC can be changed from +36dB through -128dB in 0.125dB steps using the digital volume control feature. Included in the volume control is a “digital mute” value that will completely mute the signal output of the ADC.

2.2.3 Programmable Notch Filter

A notch filter in the digital output path optionally supports each ADC. The notch filter is used to stop a very narrow band of frequencies around a center frequency. Audio Data Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. The NAU85L40 supports the two main telecommunications Companding standards: A-law and µ-law. The A-law algorithm is primarily used in European communication systems and the µ-law algorithm is primarily used by North America, Japan, and Australia.

2.3 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire serial control interface. This simple, but highly flexible, interface is compatible with many commonly used command and control serial data protocols and host drivers. See Control Interfaces section for more detail.

Digital audio input/output data streams are transferred to and from the device separately for command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats. See Digital Audio Interface section for more detail.

3 Power Supply

The NAU85L40 has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. Because of this, there are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harming the device. However, pops and clicks may result from some sequences.

3.1 Power on and off reset

The NAU85L40 includes a power on and off reset circuit on chip. The circuit resets the internal logic control at VDDC and VDDA supply power up and this reset function is automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 0.55Vdc and 1.0Vdc for VDDA. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held on while the power levels for both VDDC and VDDA are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6µs.

An additional internal RC filter based circuit is added which helps the circuit respond for fast ramp rates (~10µs) and generate the desired reset period width (~10µs at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50ns.

For reliable operation, it is recommended to write to register Reg0x00 upon power up. This will reset all registers to the known default state.

Note that when VDDA and/or VDDC are below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

3.2 Reference Voltage Generation

The NAU85L40 includes a mid-supply reference circuit that is decoupled to VSS through the VREF pin by means of a bypass capacitor. The VREF voltage is used as the reference for the majority of the circuits inside NAU85L40. Therefore, the bypass capacitor needs to be large in order to achieve good power supply rejection at low frequencies. Typically, a 4.7uF capacitor can be used. However, a larger value can be chosen but it will increase the rise time of VREF and therefore it will delay the valid line output signal. However, a pre-charge circuit can pre-charge the capacitor close to VDDA/2 at power up in order to reduce the rise time for fast line out availability. This bypass capacitor should also be low leakage due to the high impedance nature of the VREF pin

The NAU85L40 provides two microphone bias pins which can be used in various stereo applications. The microphone bias can be used to power electret microphones. In order to ensure safe operation of the device, it is recommended that the microphones do not draw more than 4mA of current from each MICBIAS pin.

4 Clocking and Sample Rates

The internal clocks for the NAU85L40 are derived from a common internal clock source, MCLK. This clock is the reference for the ADCs and DSP core functions, digital audio interface and other internal functions.

MCLK can be derived directly from MCLKI pin or may be generated from a Frequency Locked Loop (FLL) using MCLKI, BCLK or FS as a reference. The FLL provides additional flexibility for a wide range of MCLK frequencies and can be used to generate a free-running clock in the absence of an external reference source. Frequency Locked Loop (FLL)

The integrated FLL can be used to generate a master system clock, MCLK, from MCLKI, BCLK or FS as a reference. Because of the FLL's tolerance of jitter, it may be used to generate a stable MCLK from less stable input clock sources or it can be used to generate a free-running clock in the absence of an external reference clock source.

5 Control Interfaces

5.1 Selection of Control Mode

The NAU85L40 features include a serial control bus that provides access to all of the device control registers. This bus may be configured either as a 2-wire interface that is interoperable with industry standard implementations of the I2C serial bus, or as a 3-wire bus compatible with commonly used industry implementations of the SPI (Serial Peripheral Interface) bus.

The timing in all three bus configurations is fully static resulting in good compatibility with standard bus interfaces and software simulated buses. A software simulated bus can be very simple and low cost, such as by utilizing general purpose I/O pins on the host controller and software "bit banging" techniques to create the required timing.

5.2 2-Wire-Serial Control Mode (I^2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU85L40 can function only as a slave device when in the 2-wire interface configuration.

5.3 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

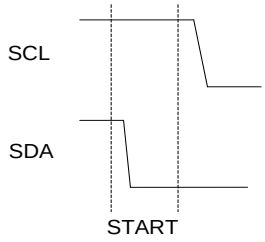


Figure 7: Valid START Condition

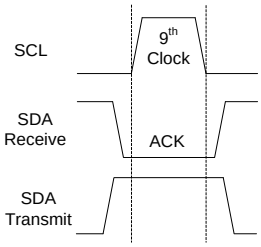


Figure 8: Valid Acknowledge

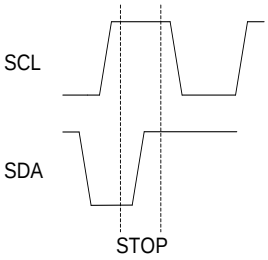


Figure 9: Valid STOP Condition

0	0	1	1	1	0	csb	R/W	Device Address Byte
A15	A14	A13	A12	A11	A10	A9	A8	Control Address Bytes
A7	A6	A5	A4	A3	A2	A1	A0	
D15	D14	D13	D12	D11	D10	D9	D8	Data Bytes
D7	D6	D5	D4	D3	D2	D1	D0	

Figure 10: Slave Address Byte, Control Address Bytes, and Data Byte Order

5.4 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The Device Address of the NAU85L40 is either 0x1C (CSB=0) or 0x1D (CSB=1). In I2C mode the CSB pin will set the LSB of the Slave Address. If the Device Address matches this value, the NAU85L40 will respond with the expected ACK signaling as it accepts the data being transmitted to it.

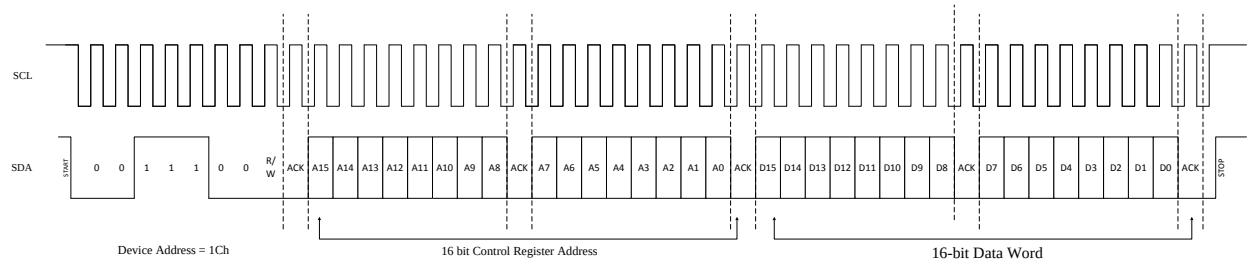


Figure 11: Byte Write Sequence

5.5 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

If the device address matches this value, the NAU85L40 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU85L40 transmits an ACK, followed by a two byte value containing the 16 bits of data from the selected control register inside the NAU85L40.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU85L40. If there is no STOP signal from the master, the NAU85L40 will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU85L40 reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

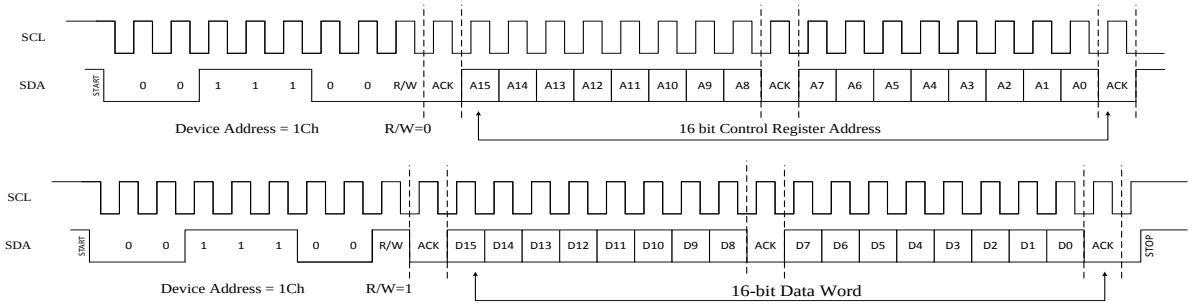


Figure 12: Read Sequence

5.6 SPI Serial Control (3-wire interface)

The Serial Peripheral Interface (SPI) is one of the widely accepted communication interfaces implemented in Nuvoton Audio CODEC portfolio. SPI is a software protocol allowing operation on a simple 3-wire bus where the data is transferred MSB first, where the NAU85L40 architectures a 32-bit write. The SPI interface consists of a clock (SCL), chip select (CSB), serial data input (SDA). SCL is static, allowing the user to stop the clock and then start it again to resume operations where it left off.

5.6.1 16-bit Write Operation (SPI 3-Wire Write)

Whenever the MODE pin on the NAU85L40 is in the logic LOW condition, the device control interface will operate in the 3-Wire SPI mode. This is a write-only mode that does not require the fourth wire normally used to read data from a device on an SPI bus implementation. This mode is a 32-bit transaction consisting of a 16-bit Control Register Address, and 16-bits of control register data. In this mode, SDA data bits are clocked continuously into a temporary holding register on each rising edge of SCL, until the CSB pin undergoes a LOW-to-HIGH logic transition. At the time of the transition, the most recent 32-bits of data are latched into the NAU85L40, with the 16-bit data value being written into the NAU85L40 control register addressed by the Control Register Address portion of the 16-bit value.

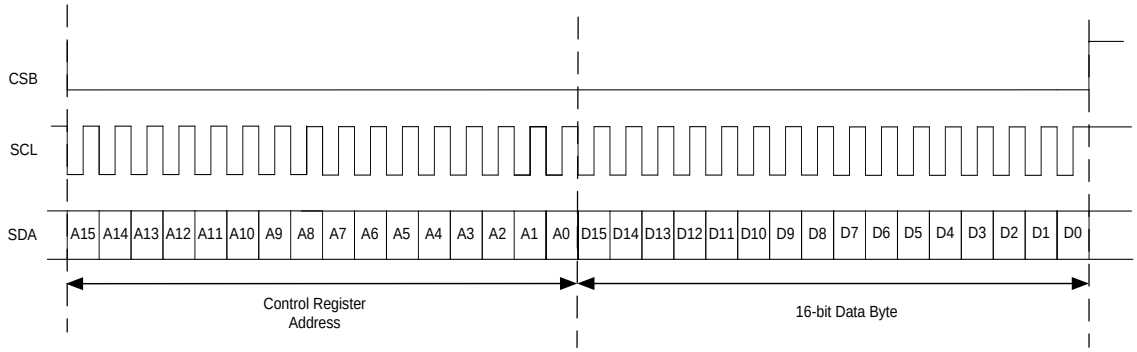


Figure 13: Register write operation using a 32-bit SPI Interface

6 Digital Audio Interface

6.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below where N is the word length.

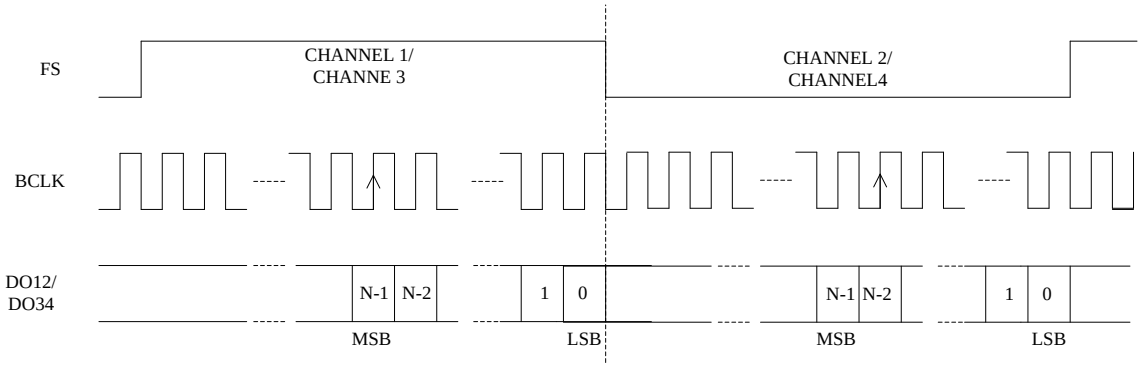


Figure 14: Right Justified Audio Format

6.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

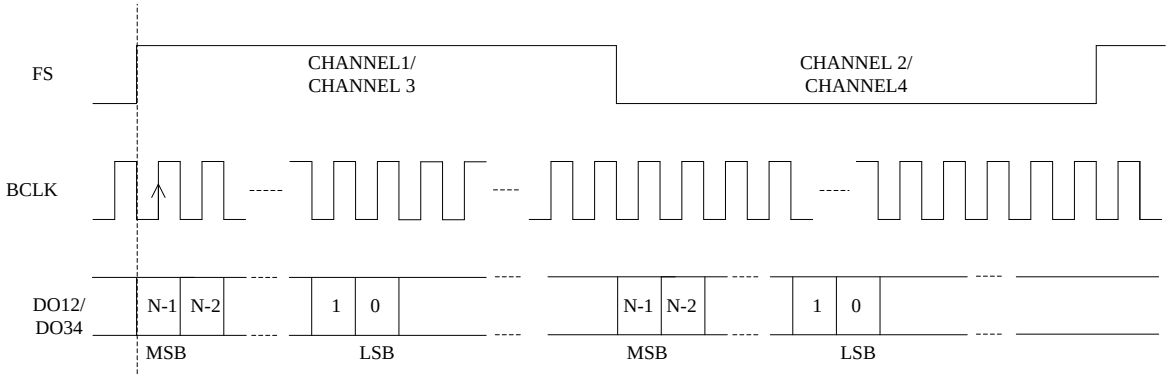


Figure 15: Left Justified Audio Format

6.3 I2S Audio Data Mode

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This is shown in the figure below.

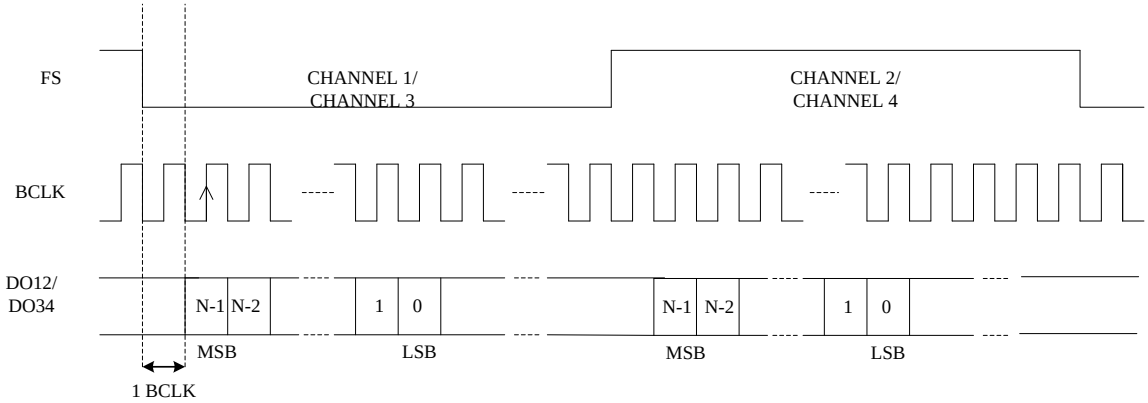


Figure 16: I2S Audio Format

6.4 PCM A Audio Data

In the PCM A mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

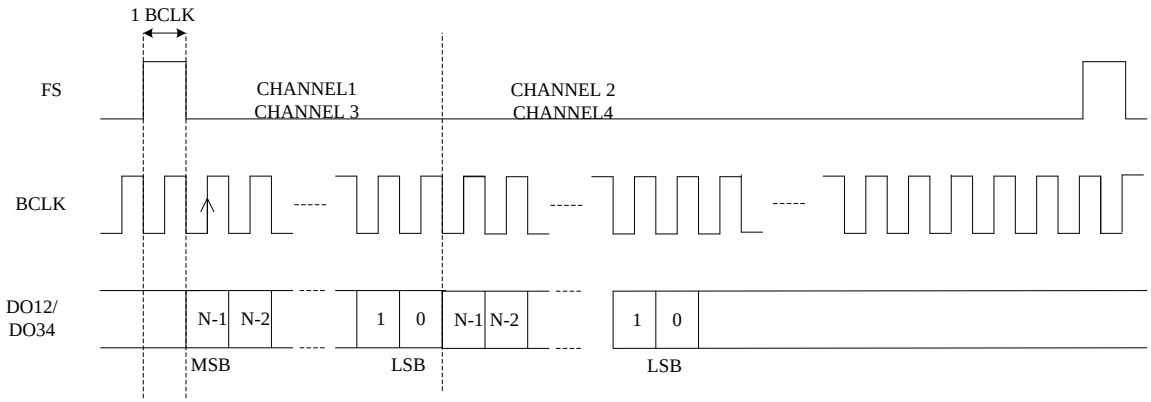


Figure 17: PCM A Audio Format

6.5 PCM B Audio Data

In the PCM B mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

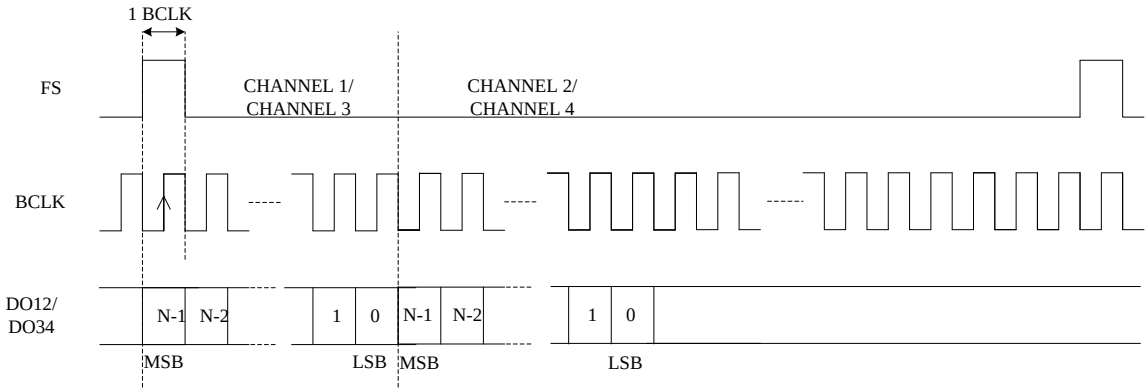


Figure 18: PCM B Audio Format

6.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at ADC data are clocked. This increases the flexibility of the NAU85L40 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU85L40 or other devices to share the audio data bus, thus enabling more than two channels of audio. This feature may also be used to swap left and right channel data, or to cause both the left and right channels to use the same data.

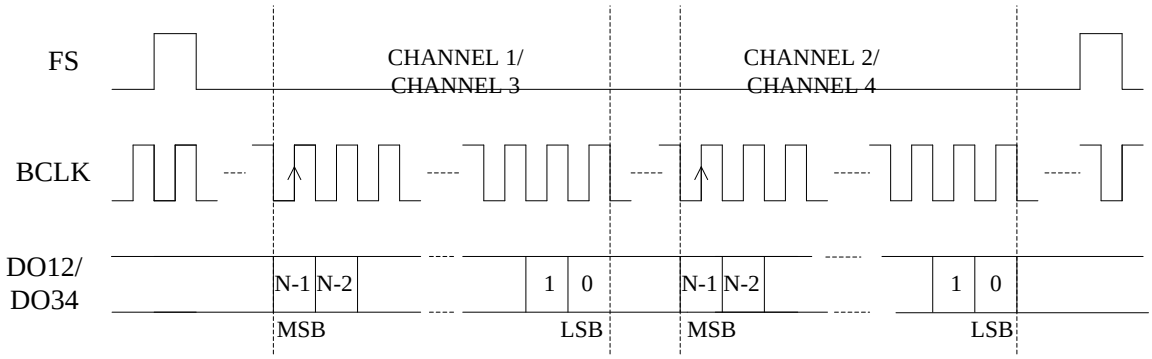


Figure 19: PCM Time Slot Audio Format

6.7 TDM Right Justified Audio Data

In right justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel 1 then channel 3 data is transmitted and when FS is LOW, channel 2 then channel 4 data is transmitted. This is shown in the figure below.

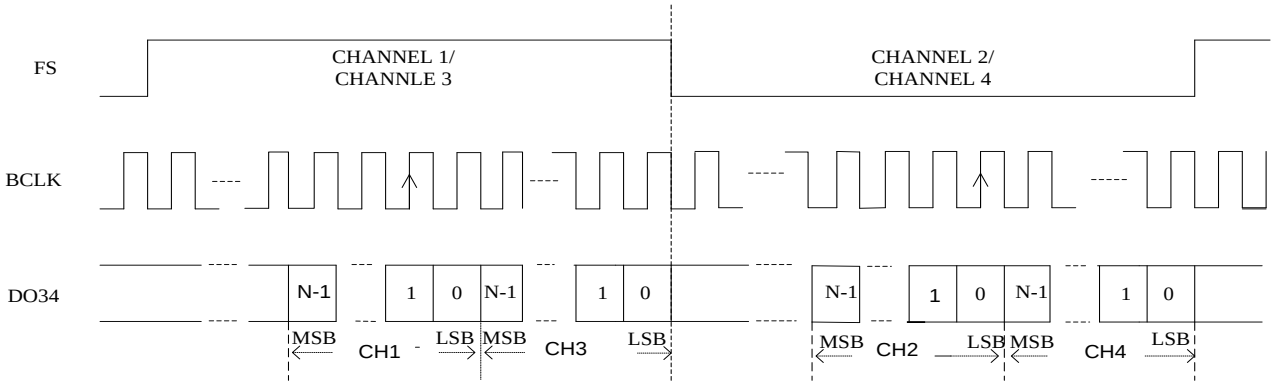


Figure 20: TDM Right Justified Audio Format

6.8 TDM Left Justified Audio Data

In left justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel 1 then channel 3 data is transmitted and when FS is LOW, channel 2 then channel 4 channel data is transmitted. This is shown in the figure below.

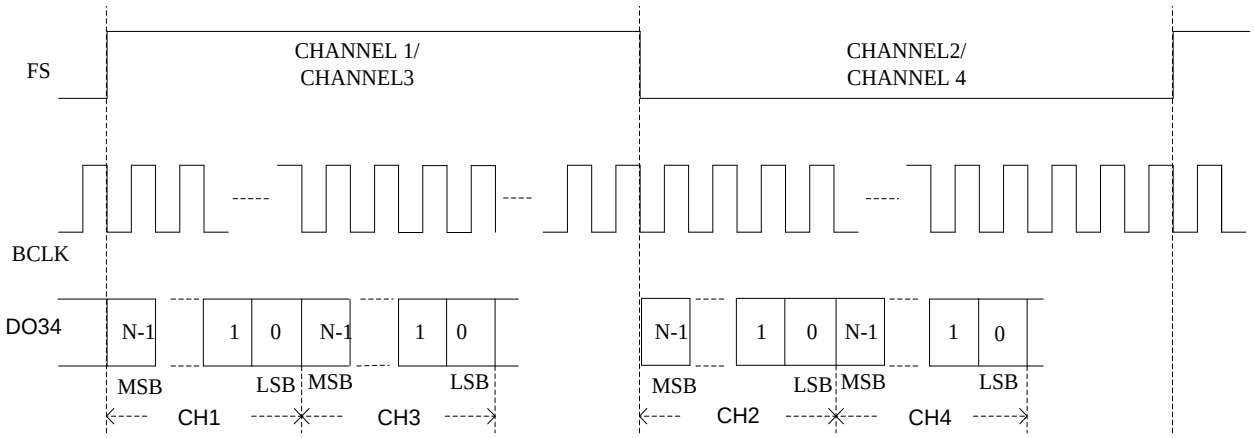


Figure 21: TDM Left Justified Audio Format

6.9 TDM I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel 1 then channel 3 channel data is transmitted and when FS is HIGH, channel 2 then channel 4 channel data is transmitted. This is shown in the figure below.

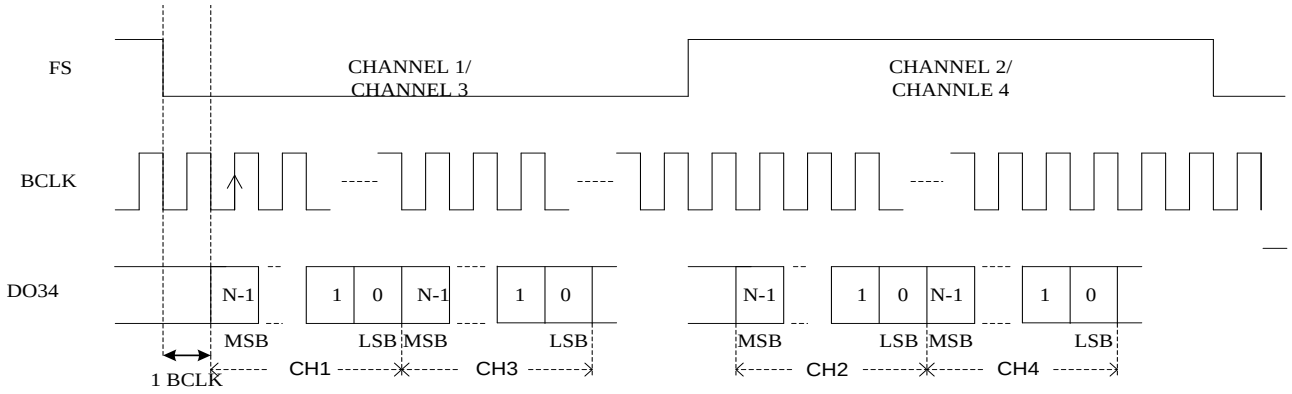


Figure 22: TDM I2S Audio Format

6.10 TDM PCM A Audio Data

In the PCM A mode, channel 1 data is transmitted first followed sequentially by channel 2, 3, and 4 immediately after. The channel 1 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

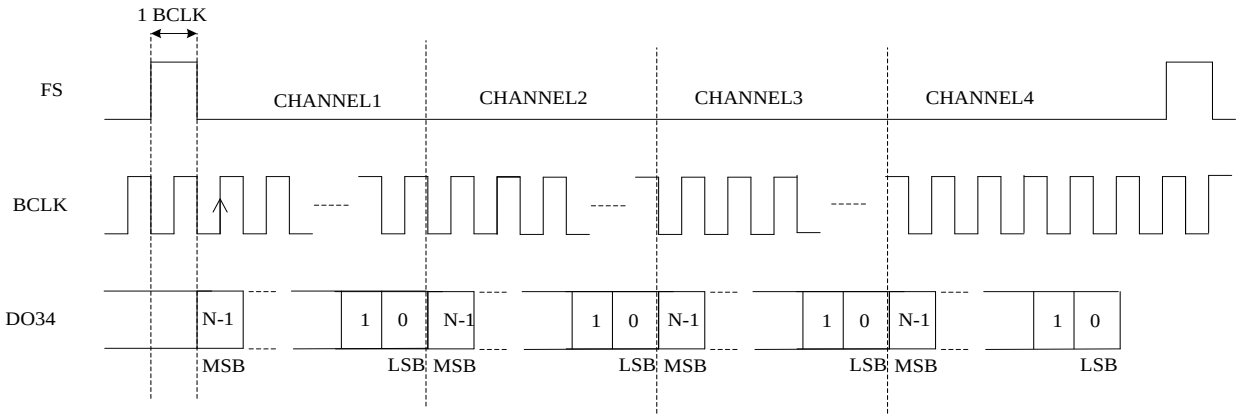


Figure 23: TDM PCM A Audio Format

6.11 TDM PCM B Audio Data

In the PCM B mode, channel 1 data is transmitted first followed sequentially by channel 2, 3, and 4 immediately after. The channel 1 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

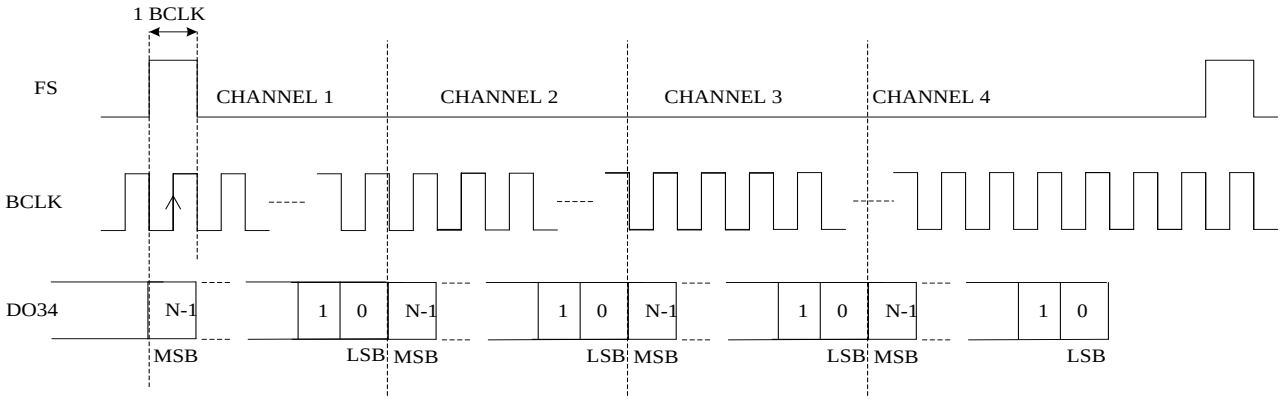


Figure 24: TDM PCM B Audio Format

6.12 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which the ADC data is clocked. This increases the flexibility of the NAU85L40 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU85L40 or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

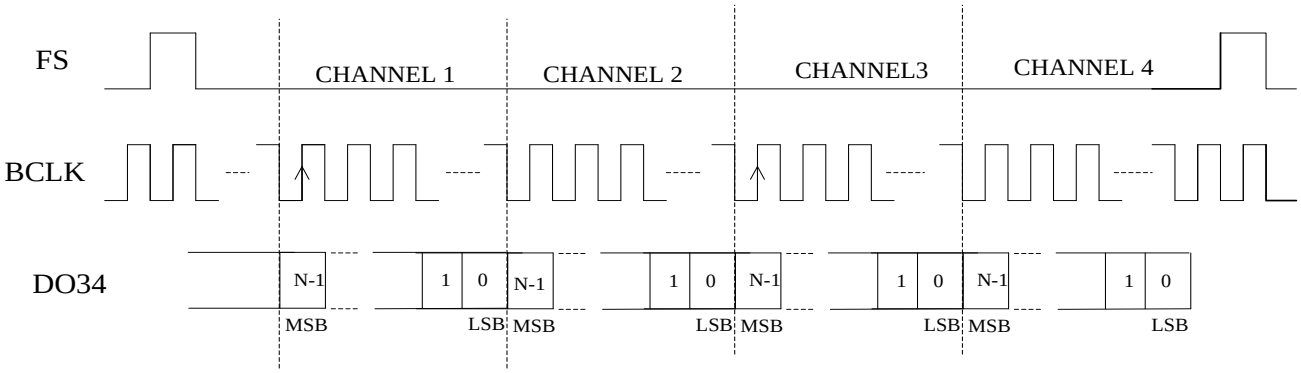


Figure 25: TDM PCM Offset Audio Format

7 Typical Application Diagrams

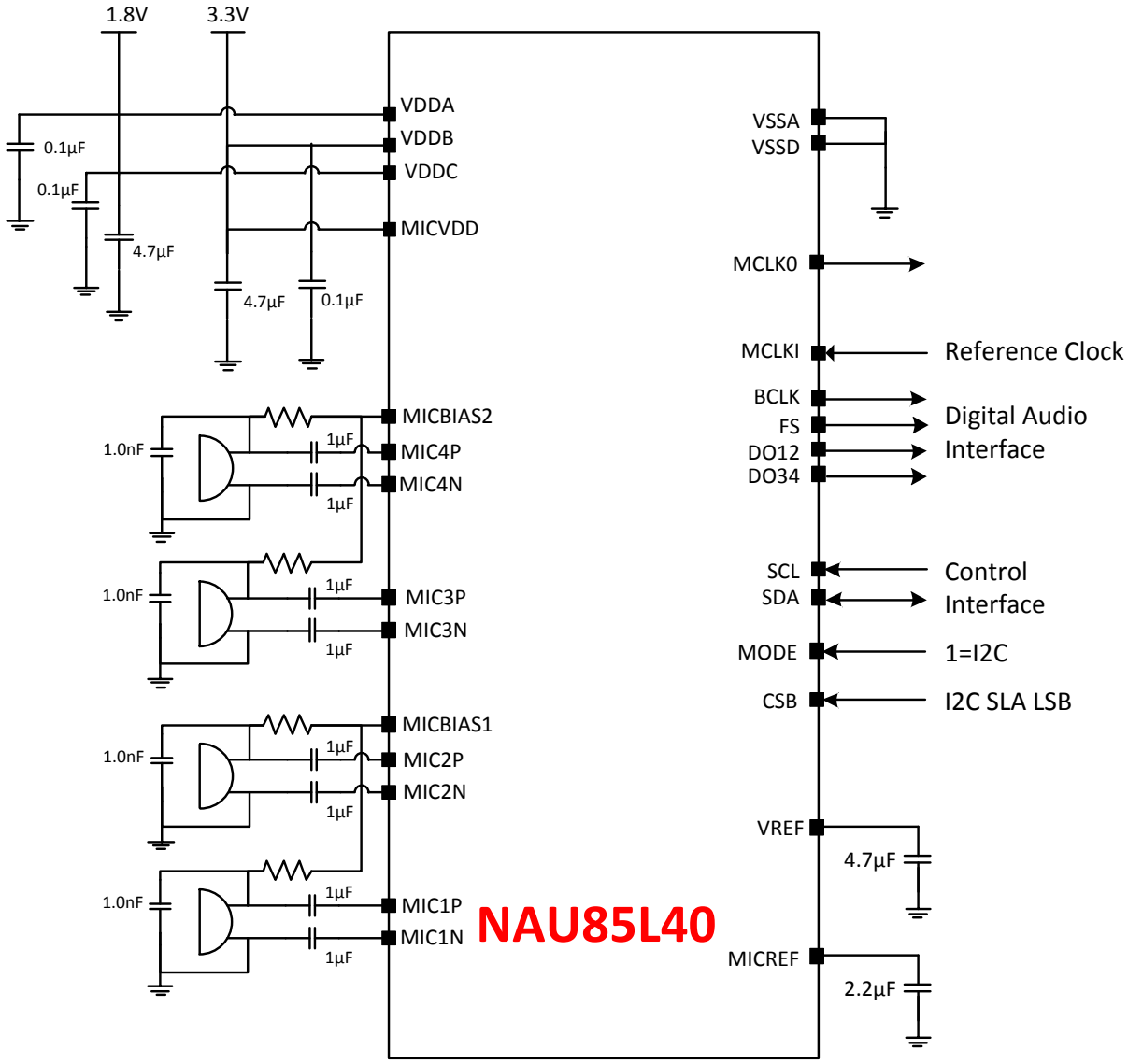


Figure 26: Typical Single-ended use Application Diagram

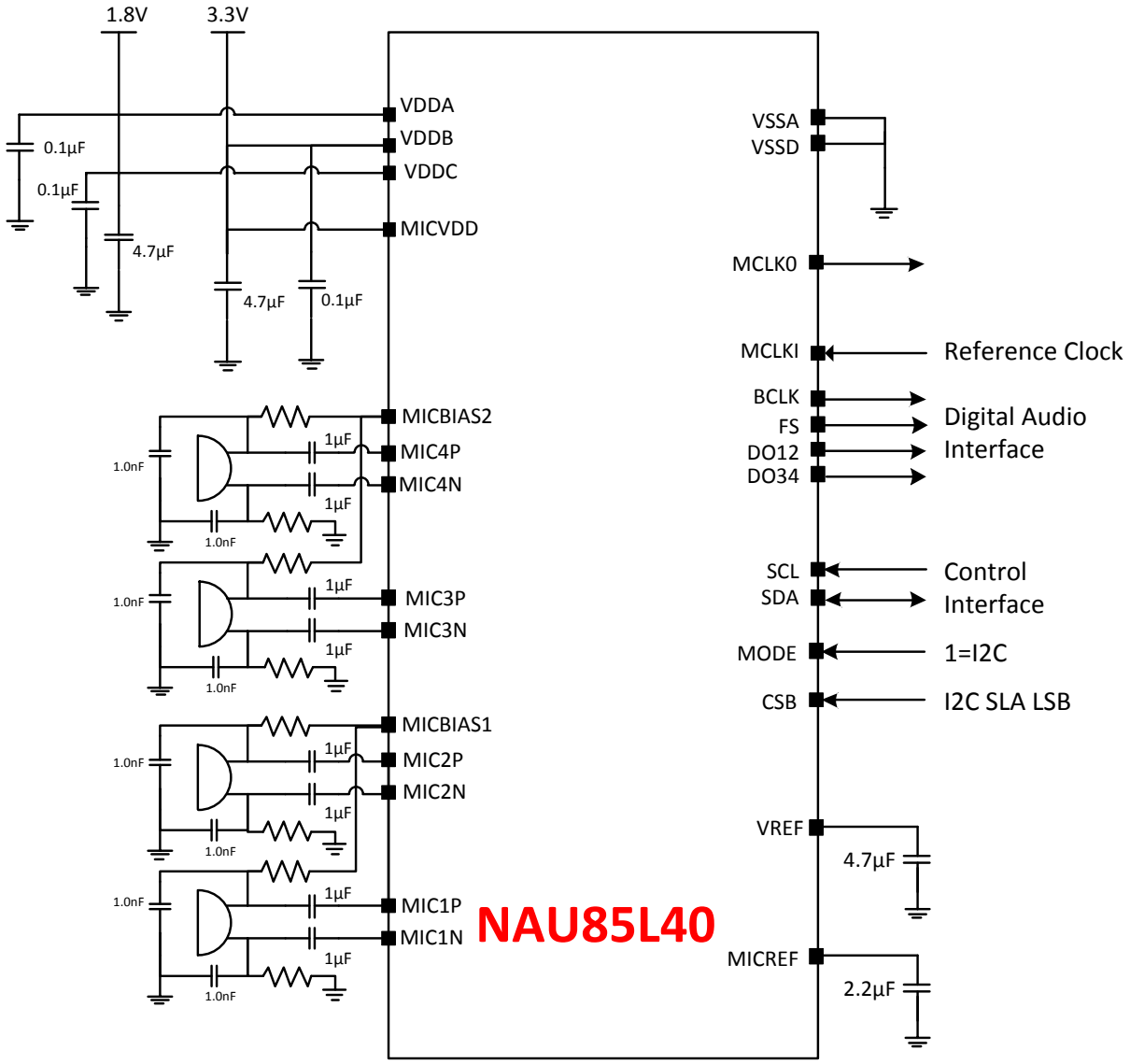
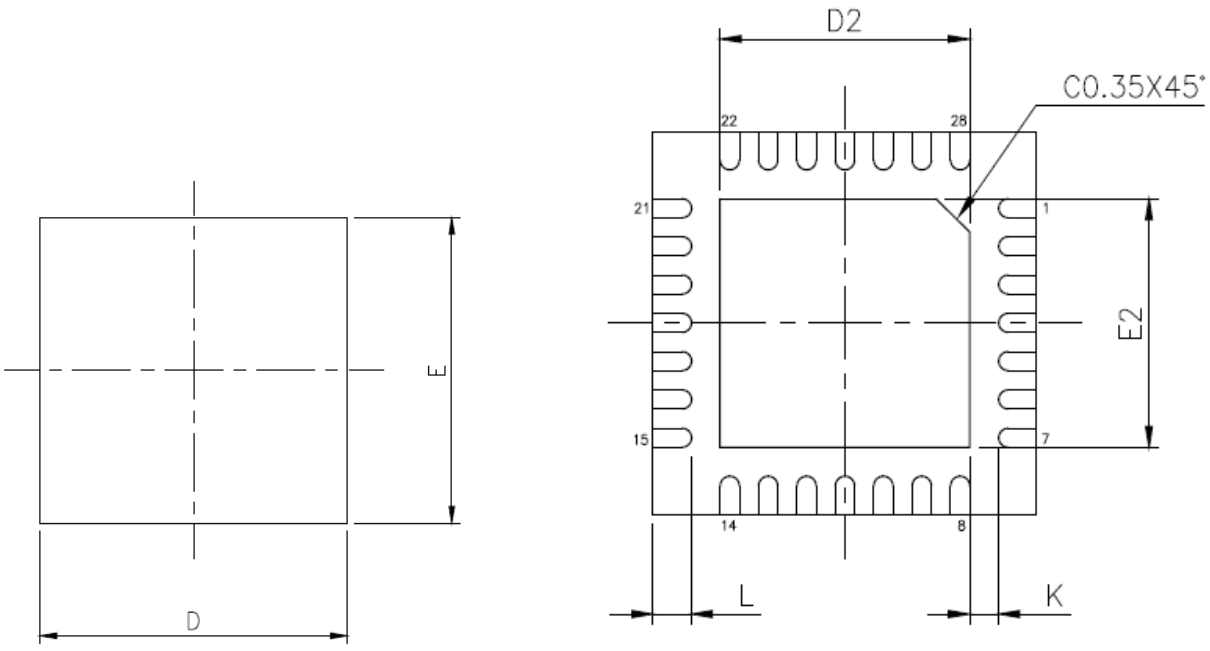


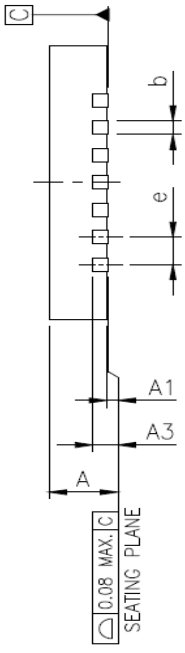
Figure 27: Typical Application Schematic for Differential Microphone Connection

8 Package Information

QFN 28L 4X4 mm^2, Thickness: 0.8 mm (Max), Pitch: 0.40 mm

EP SIZE 2.6X2.6 mm





PKG CODE	QFN 28L		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
K	0.20	—	—
D2	2.55	2.60	2.65
E2	2.55	2.60	2.65
L	0.30	0.40	0.50

9 ORDERING INFORMATION

Nuvoton Part Number Description

NAU85L40_ _

Package Material:

G = Pb-free Package

Package Type:

Y = 28-Pin QFN Package

Version History

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
0	November, 05,2014	-	Initial Preliminary Release
0.5	December, 15,2014	5,6	Updated AC/DC parameters
1.0	May 15, 2015	ALL PAGES HEADERS	Removed Preliminary
1.1	Oct 14, 2015	23	Updated Package Spec