NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

V_{DD} - V_{SS} 7.0V
All other inputs and outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current ..... ±25 mA
Current at Input Pins ..... ±2 mA
Current at Output and Supply Pins ..... ±50 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied.... -40°C to +125°C
Junction temperature ..... +150°C
ESD protection on all pins (HBM/MM)..... ≥ 4 kV/200V
ESD protection on MCP65R46 OUT pin (HBM/MM)..... ≥ 4 kV/175V

†Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN+} = V_{DD}/2, V_{IN-} = V_{SS}, R_L = 100 kΩ to V_{DD}/2 (**MCP65R41** only), and $R_{Pull-Up}$ = 2.74 kΩ to V_{DD} (**MCP65R46** only).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Comparator	I_Q	—	2.5	4	µA	I_{OUT} = 0
Input						
Input Voltage Range	V_{CMR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Common-Mode Rejection Ratio V_{DD} = 5V	CMRR	55	70	—	dB	V_{CM} = -0.3V to 5.3V
		50	65	—	dB	V_{CM} = 2.5V to 5.3V
		55	70	—	dB	**MCP65R41**, V_{CM} = -0.3V to 2.5V
		50	70	—	dB	**MCP65R46**, V_{CM} = -0.3V to 2.5V
Power Supply Rejection Ratio	PSRR	63	80	—	dB	V_{CM} = V_{SS}
Input Offset Voltage	V_{OS}	-10	±3	+10	mV	V_{CM} = V_{SS} **(Note 1)**
Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	±10	—	µV/°C	V_{CM} = V_{SS}
Input Hysteresis Voltage	V_{HYST}	1	3.3	5	mV	V_{CM} = V_{SS} **(Note 1)**
Drift with Temperature	$\Delta V_{HYST}/\Delta T$	—	6	—	µV/°C	V_{CM} = V_{SS}
Drift with Temperature	$\Delta V_{HYST}/\Delta T^2$	—	5	—	µV/°C^2	V_{CM} = V_{SS}
Input Bias Current	I_B	—	1	—	pA	V_{CM} = V_{SS}
T_A = +85°C	I_B	—	50	—	pA	V_{CM} = V_{SS}
T_A = +125°C	I_B	—	—	5000	pA	V_{CM} = V_{SS}
Input Offset Current	I_{OS}	—	±1	—	pA	V_{CM}= V_{SS}
Common Mode/ Differential Input Impedance	Z_{CM}/Z_{DIFF}	—	10^{13}||4	—	Ω||pF	

Note 1: The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: Limit the output current to Absolute Maximum Rating of 50 mA.

3: Do not short the output of the **MCP65R46** comparators above V_{SS} + 10V.

4: The low-power reference voltage pin is designed to drive small capacitive loads. See **Section 4.5.2**.

DC CHARACTERISTICS (CONTINUED)

Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN+} = V_{DD}/2, V_{IN-} = V_{SS}, R_L = 100 kΩ to V_{DD}/2 (**MCP65R41** only), and $R_{Pull-Up}$ = 2.74 kΩ to V_{DD} (**MCP65R46** only).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Push Pull Output						
High-Level Output Voltage	V_{OH}	V_{DD}–0.2	—	—	V	I_{OUT} = -2 mA, V_{DD} = 5.5V
Low-Level Output Voltage	V_{OL}	—	—	V_{SS}+0.2	V	I_{OUT} = 2 mA, V_{DD} = 5.5V
Short Circuit Current	I_{SC}	—	±50	—	mA	(**Note 2**)
Open Drain Output (MCP65R46)						
Low-Level Output Voltage	V_{OL}	—	—	V_{SS}+0.2	V	I_{OUT} = 2 mA, V_{DD} = 5.5V
Short Circuit Current	I_{SC}	—	±50	—	mA	V_{PU} = V_{DD} = 5.5V
High-Level Output Current	I_{OH}	-100	—	—	nA	V_{PU} = 10V
Pull-Up Voltage	V_{PU}	1.6	—	10	V	**Note 3**
Output Pin Capacitance	C_{OUT}	—	8	—	pF	
Reference Voltage Output						
Initial Reference Tolerance	V_{TOL}	-2	±1	+2	%	I_{REF} = 0A, V_{REF} = 1.21V and 2.4V
	V_{REF}	1.185	1.21	1.234	V	I_{REF} = 0A
		2.352	2.4	2.448	V	
Reference Output Current	I_{REF}	—	±500	—	µA	V_{TOL} = ±2% (maximum)
Drift with Temperature (characterized but not production tested)	$\Delta V_{REF}/\Delta T$	—	27	100	ppm	V_{REF} = 1.21V, V_{DD} = 1.8V
		—	22	100	ppm	V_{REF} = 1.21V, V_{DD} = 5.5V
		—	23	100	ppm	V_{REF} = 2.4V, V_{DD} = 5.5V
Capacitive Load	C_L	—	200	—	pF	**Note 4**

Note 1: The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: Limit the output current to Absolute Maximum Rating of 50 mA.

3: Do not short the output of the **MCP65R46** comparators above V_{SS} + 10V.

4: The low-power reference voltage pin is designed to drive small capacitive loads. See **Section 4.5.2**.

AC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN+} = V_{DD}/2, Step = 200 mV, Overdrive = 100 mV, R_L = 100 kΩ to V_{DD}/2 (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to V_{DD} (**MCP65R46** only), and C_L = 50 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rise Time	t_R	—	0.85	—	µs	
Fall Time	t_F	—	0.85	—	µs	
Propagation Delay (High-to-Low)	t_{PHL}	—	4	8.0	µs	
Propagation Delay (Low-to-High)	t_{PLH}	—	4	8.0	µs	
Propagation Delay Skew	t_{PDS}	—	±0.2	—	µs	**Note 1**
Maximum Toggle Frequency	f_{MAX}	—	160	—	kHz	V_{DD} = 1.8V
	f_{MAX}	—	120	—	kHz	V_{DD} = 5.5V
Input Noise Voltage	E_N	—	200	—	μV_{P-P}	10 Hz to 100 kHz

Note 1: Propagation Delay Skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

TEMPERATURE SPECIFICATIONS

Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +5.5V and V_{SS} = GND.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, SOT23-6	θ_{JA}	—	190.5	—	°C/W	

1.2 Test Circuit Configuration

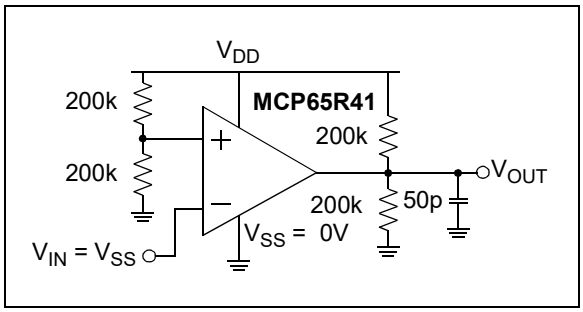


FIGURE 1-1: *Test Circuit for the Push-Pull Output Comparators.*

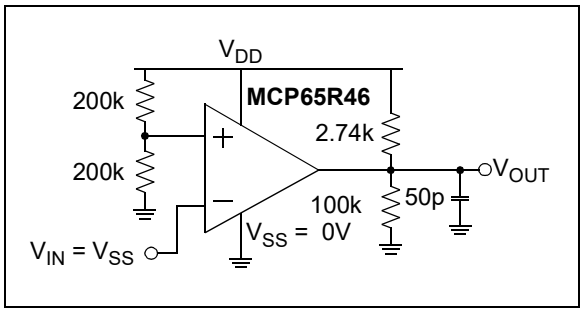


FIGURE 1-2: *Test Circuit for the Open-Drain Comparators.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 100 kΩ to V_{DD}/2 (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to V_{DD}/2 (**MCP65R46** only) and C_L = 50 pF.

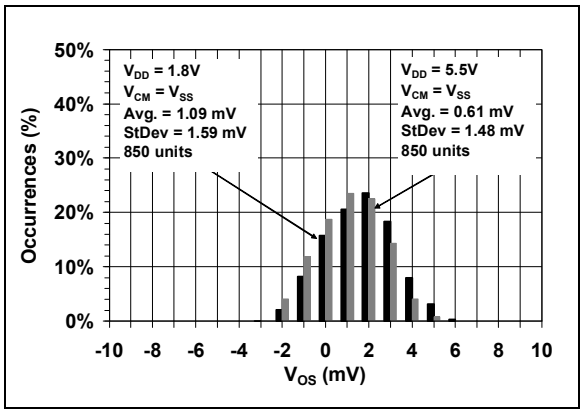


FIGURE 2-1: *Input Offset Voltage.*

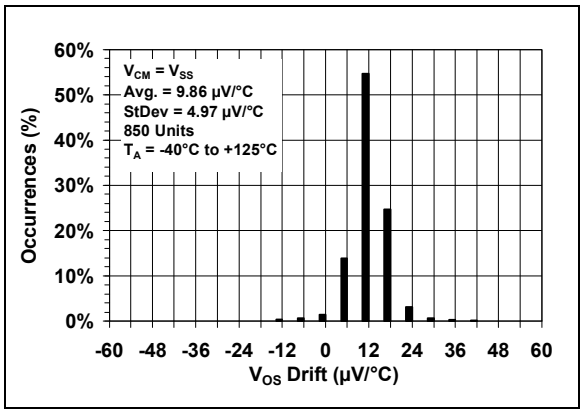


FIGURE 2-4: *Input Offset Voltage Drift.*

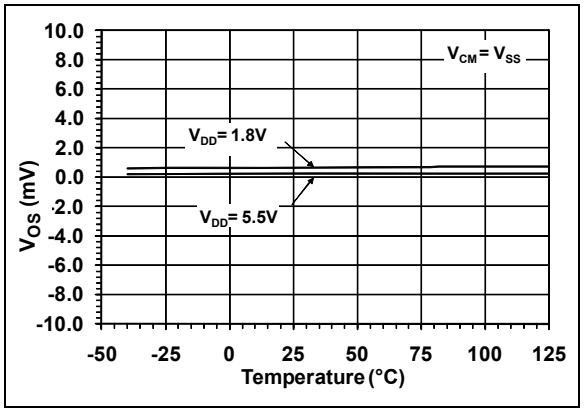


FIGURE 2-2: *Input Offset Voltage vs. Temperature.*

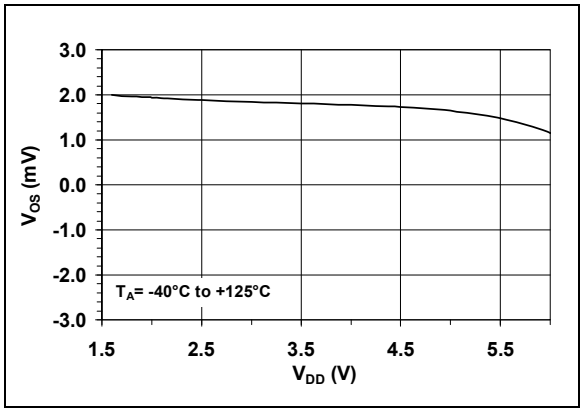


FIGURE 2-5: *Input Offset Voltage vs. Supply Voltage vs. Temperature.*

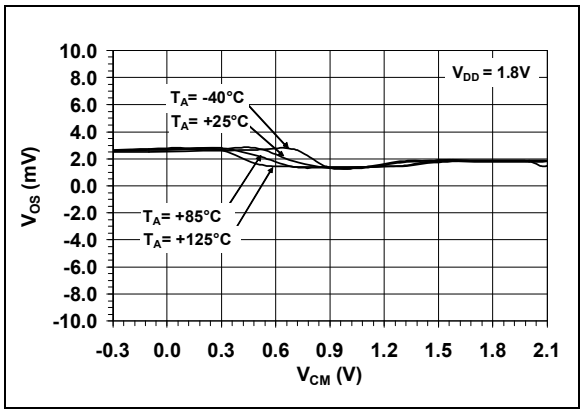


FIGURE 2-3: *Input Offset Voltage vs. Common-Mode Input Voltage.*

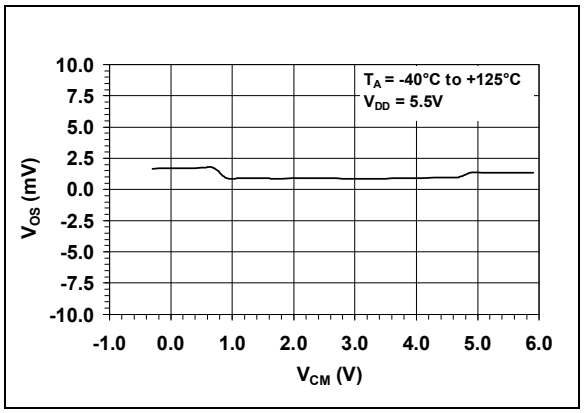


FIGURE 2-6: *Input Offset Voltage vs. Common-Mode Input Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

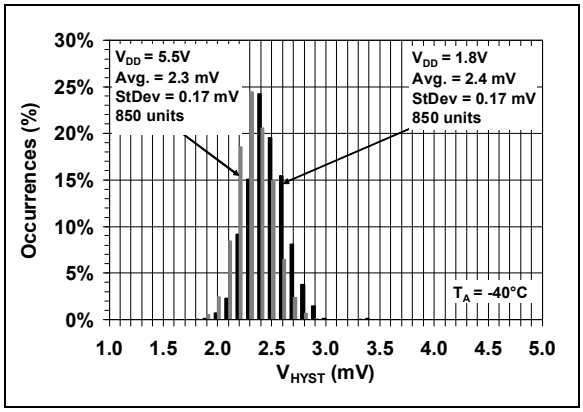


FIGURE 2-7: *Input Hysteresis Voltage at -40°C.*

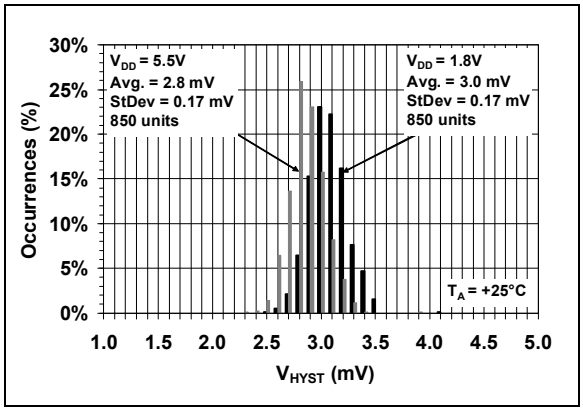


FIGURE 2-8: *Input Hysteresis Voltage at +25°C.*

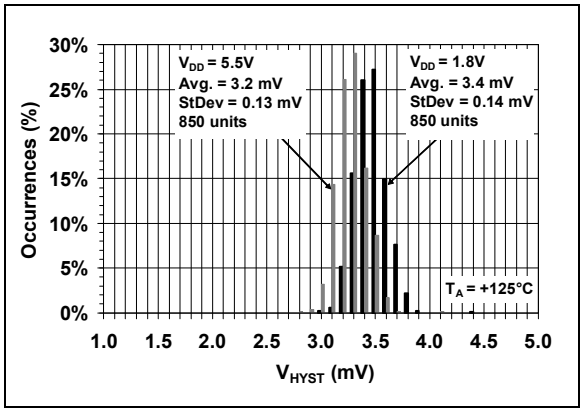


FIGURE 2-9: *Input Hysteresis Voltage at +125°C.*

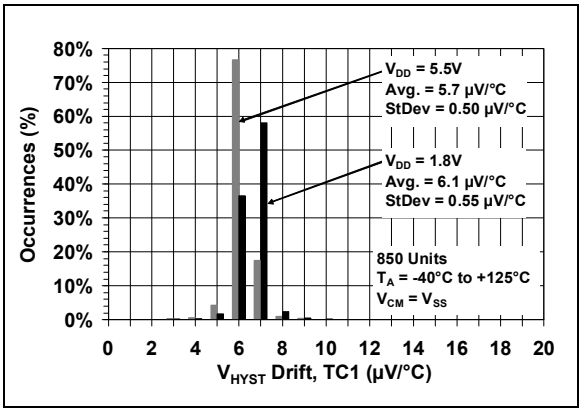


FIGURE 2-10: *Input Hysteresis Voltage Drift – Linear Temperature Compensation (TC1).*

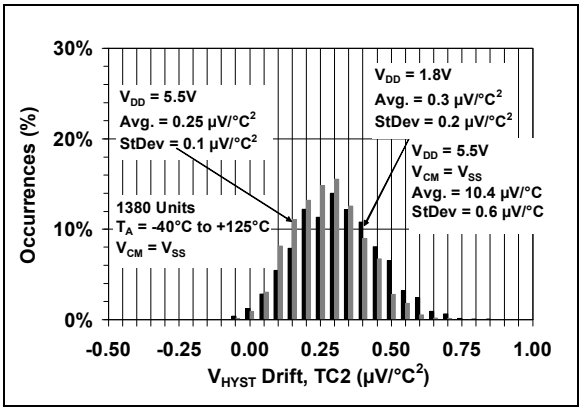


FIGURE 2-11: *Input Hysteresis Voltage Drift – Quadratic Temperature Compensation (TC2).*

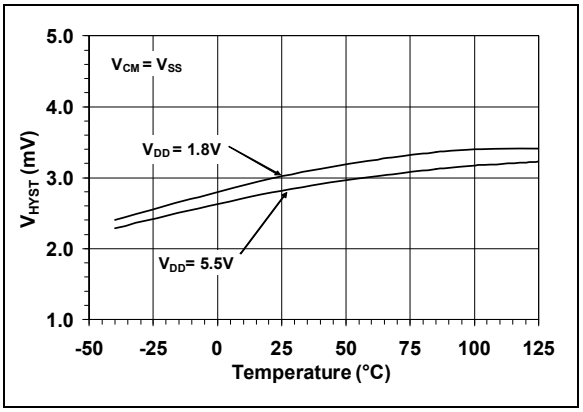


FIGURE 2-12: *Input Hysteresis Voltage vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

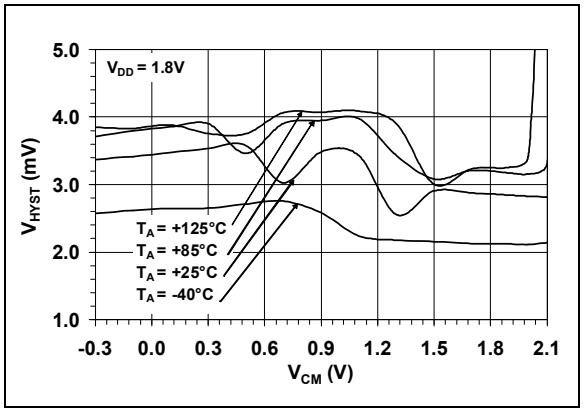


FIGURE 2-13: *Input Hysteresis Voltage vs. Common-Mode Input Voltage.*

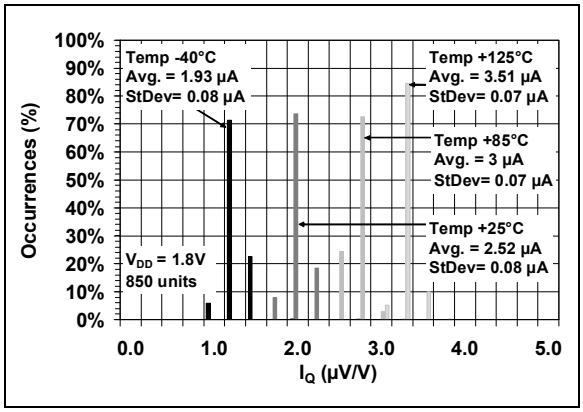


FIGURE 2-16: *Quiescent Current.*

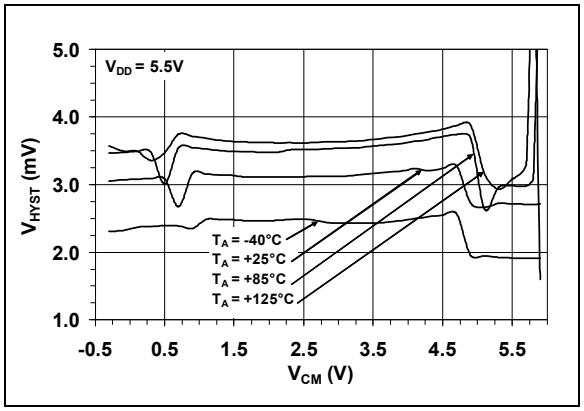


FIGURE 2-14: *Input Hysteresis Voltage vs. Common-Mode Input Voltage.*

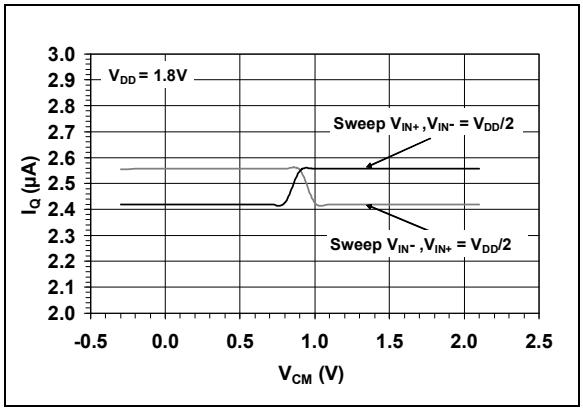


FIGURE 2-17: *Quiescent Current vs. Common-Mode Input Voltage.*

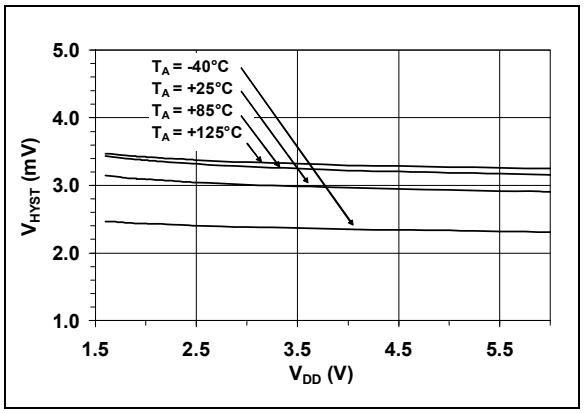


FIGURE 2-15: *Input Hysteresis Voltage vs. Supply Voltage vs. Temperature.*

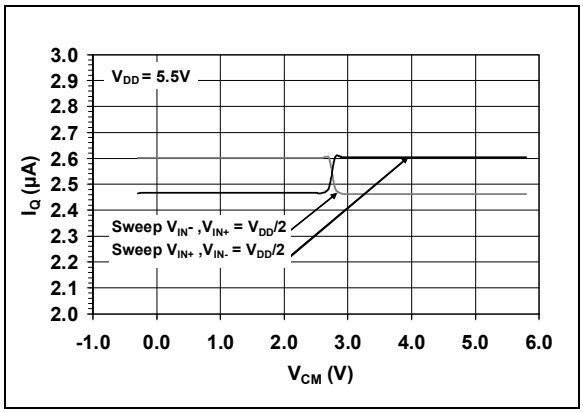


FIGURE 2-18: *Quiescent Current vs. Common-Mode Input Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

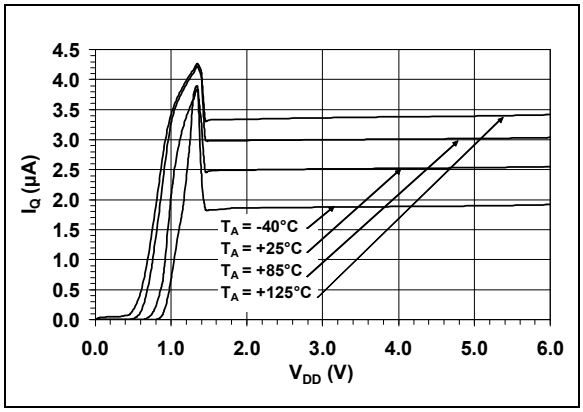


FIGURE 2-19: *Quiescent Current vs. Supply Voltage vs. Temperature.*

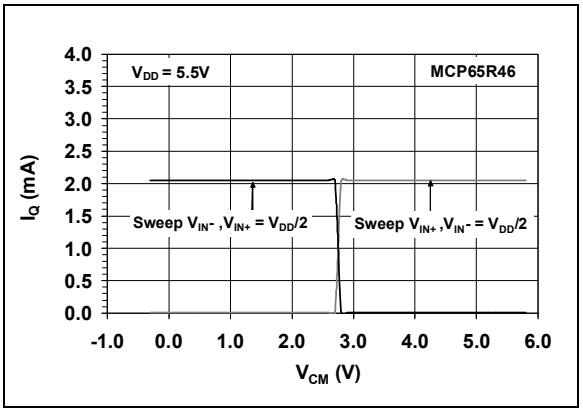


FIGURE 2-22: *Quiescent Current vs. Common-Mode Input Voltage.*

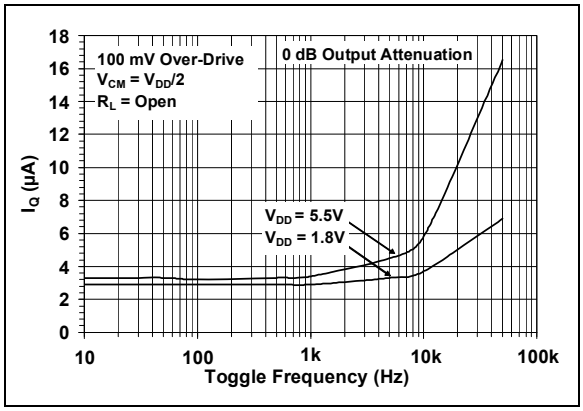


FIGURE 2-20: *Quiescent Current vs. Toggle Frequency.*

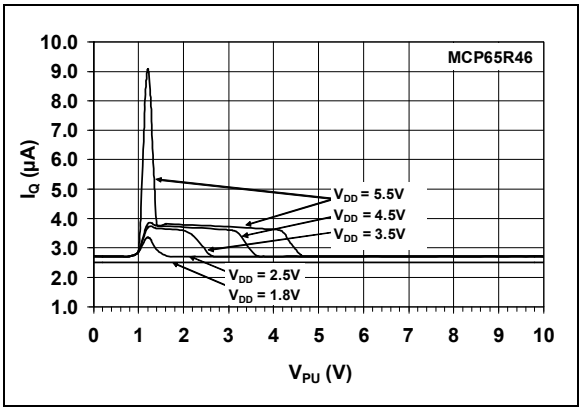


FIGURE 2-23: *Quiescent Current vs. Pull-Up Voltage.*

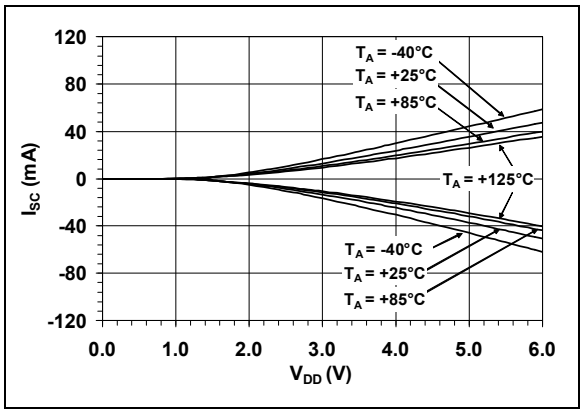


FIGURE 2-21: *Short Circuit Current vs. Supply Voltage vs. Temperature.*

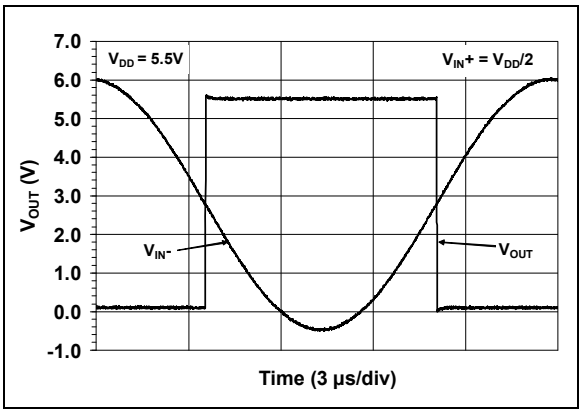


FIGURE 2-24: *No Phase Reversal.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

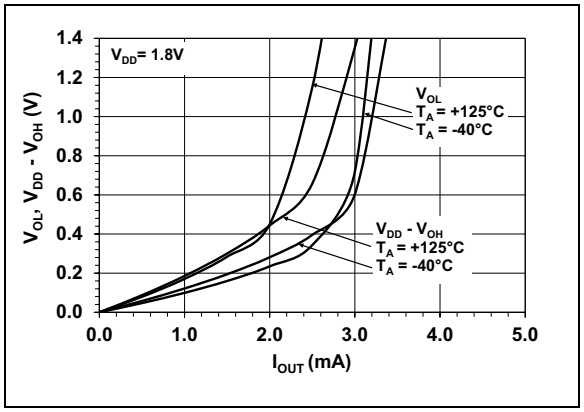


FIGURE 2-25: *Output Headroom vs. Output Current.*

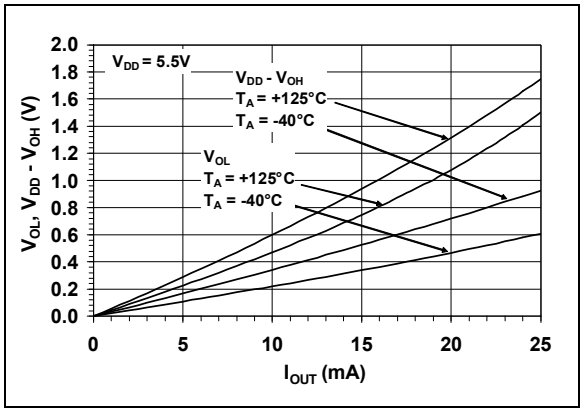


FIGURE 2-28: *Output Headroom vs. Output Current.*

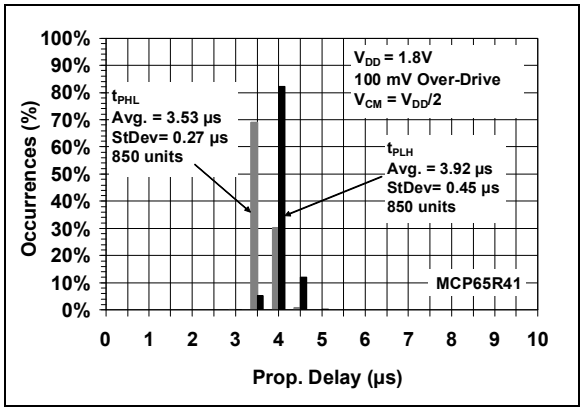


FIGURE 2-26: *Low-to-High and High-to-Low Propagation Delays.*

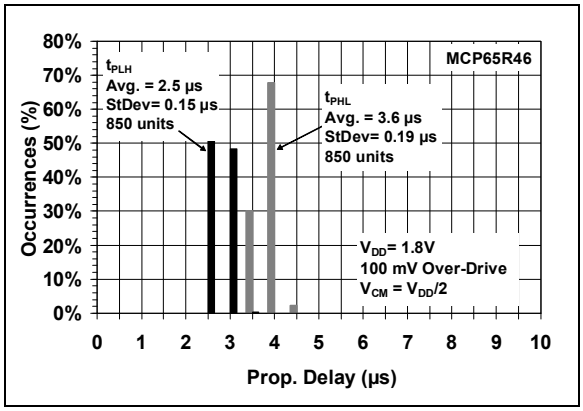


FIGURE 2-29: *Low-to-High and High-to-Low Propagation Delays.*

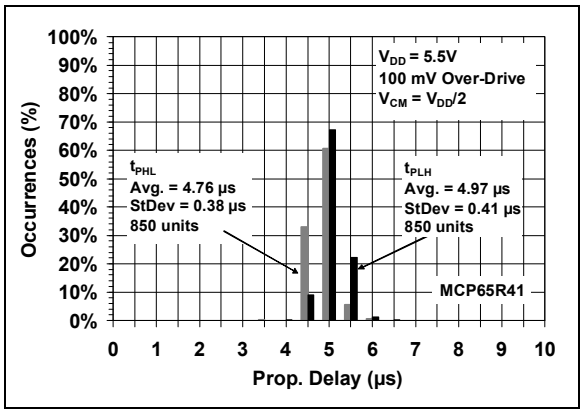


FIGURE 2-27: *Low-to-High and High-to-Low Propagation Delays.*

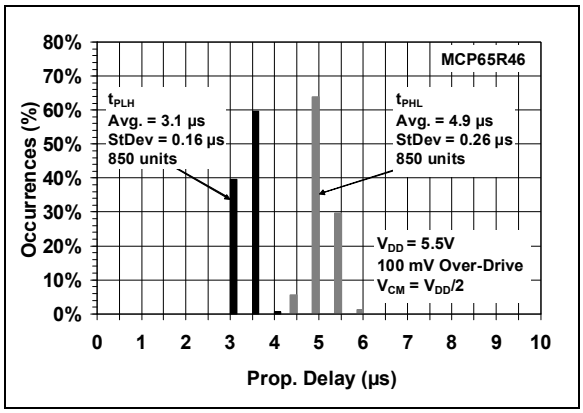


FIGURE 2-30: *Low-to-High and High-to-Low Propagation Delays.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

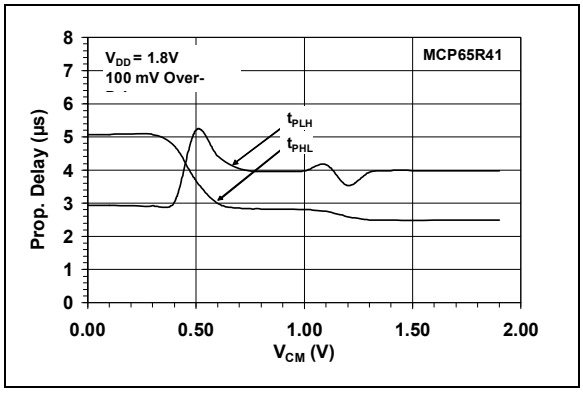


FIGURE 2-31: *Propagation Delay vs. Common-Mode Input Voltage.*

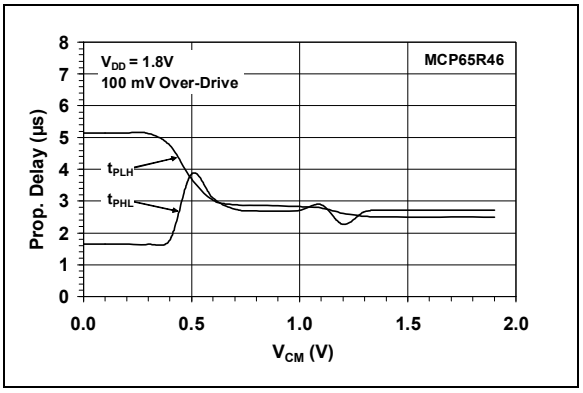


FIGURE 2-34: *Propagation Delay vs. Common-Mode Input Voltage.*

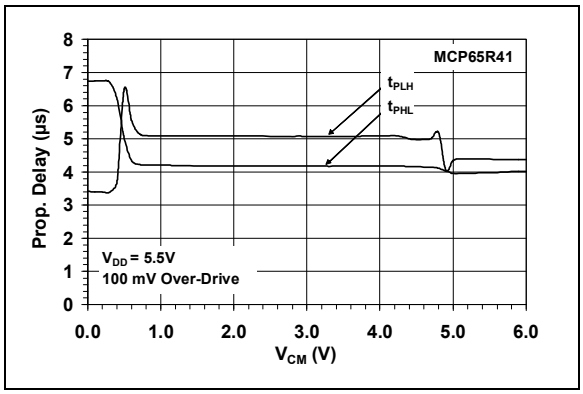


FIGURE 2-32: *Propagation Delay vs. Common-Mode Input Voltage.*

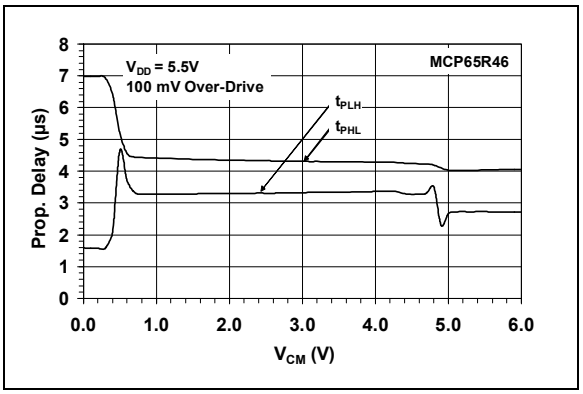


FIGURE 2-35: *Propagation Delay vs. Common-Mode Input Voltage.*

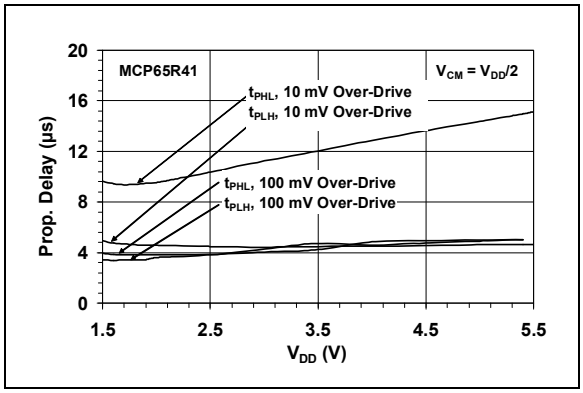


FIGURE 2-33: *Propagation Delay vs. Supply Voltage.*

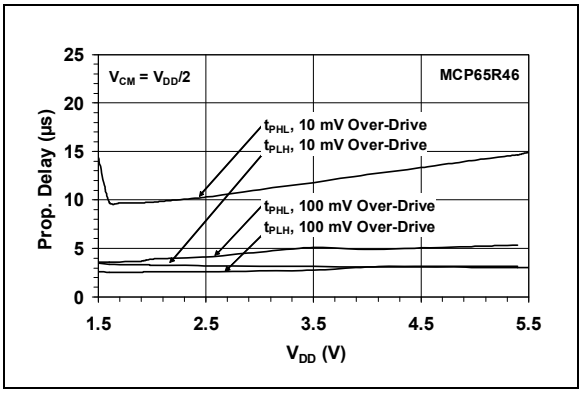


FIGURE 2-36: *Propagation Delay vs. Supply Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 100 kΩ to V_{DD}/2 (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to V_{DD}/2 (**MCP65R46** only) and C_L = 50 pF.

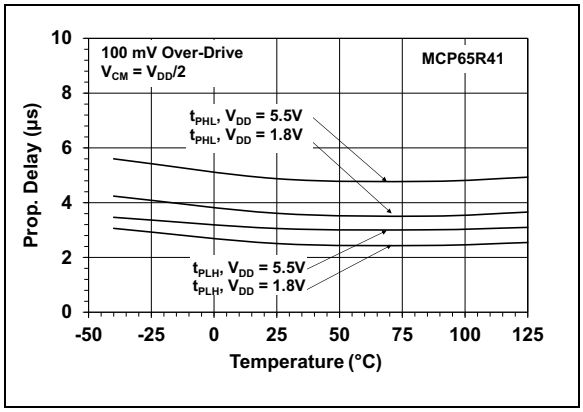


FIGURE 2-37: *Propagation Delay vs. Temperature.*

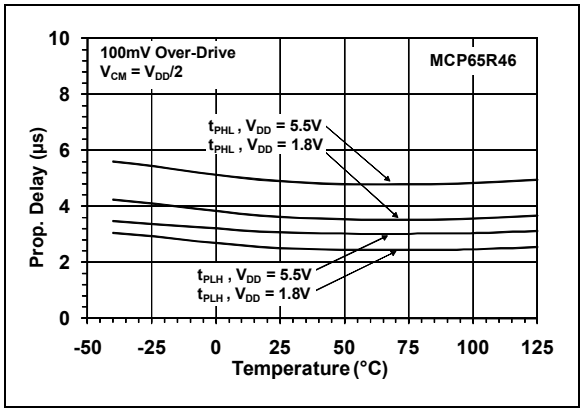


FIGURE 2-40: *Propagation Delay vs. Temperature.*

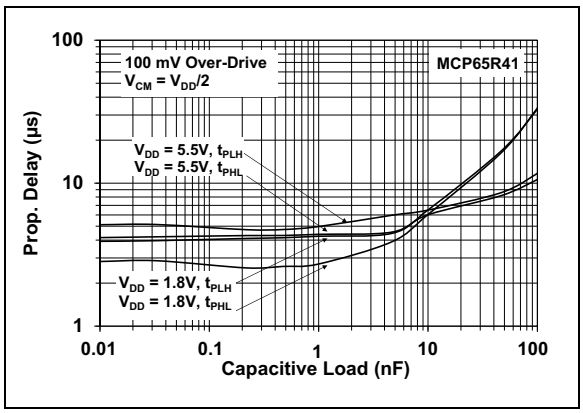


FIGURE 2-38: *Propagation Delay vs. Capacitive Load.*

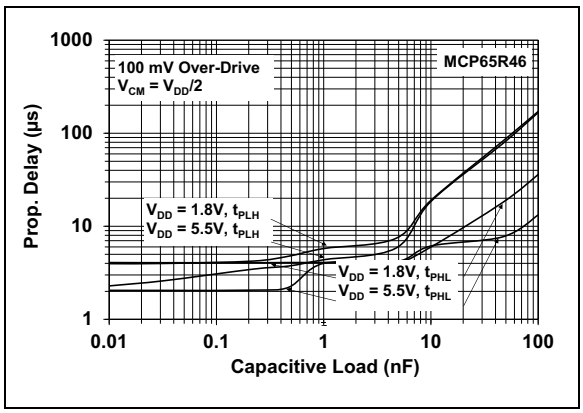


FIGURE 2-41: *Propagation Delay vs. Capacitive Load.*

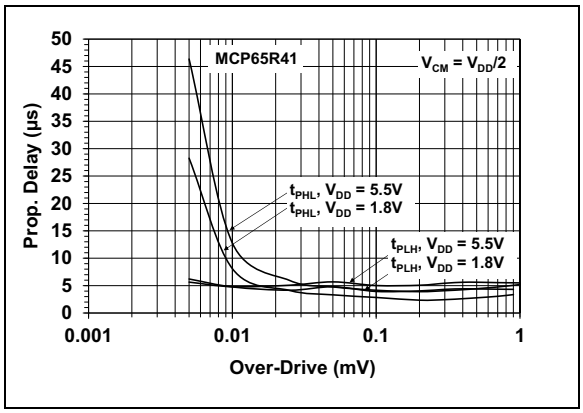


FIGURE 2-39: *Propagation Delay vs. Input Overdrive.*

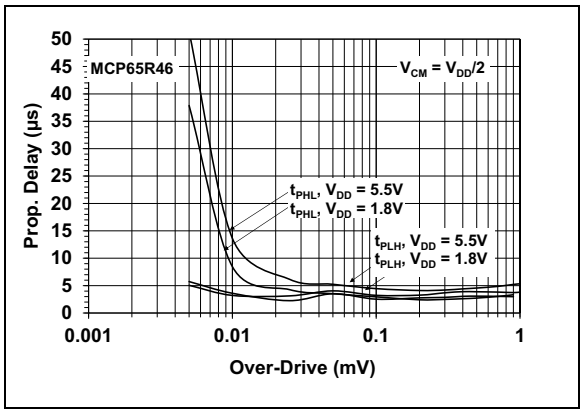


FIGURE 2-42: *Propagation Delay vs. Input Overdrive.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

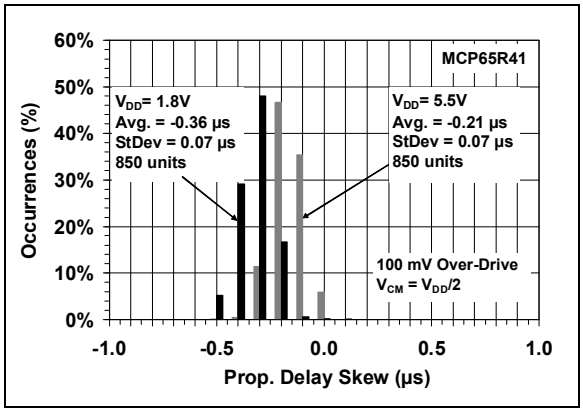


FIGURE 2-43: *Propagation Delay Skew.*

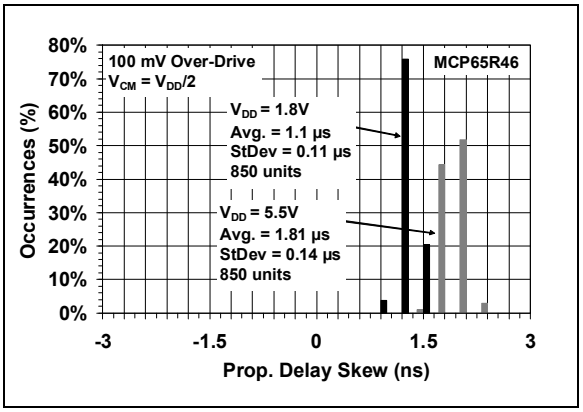


FIGURE 2-46: *Propagation Delay Skew.*

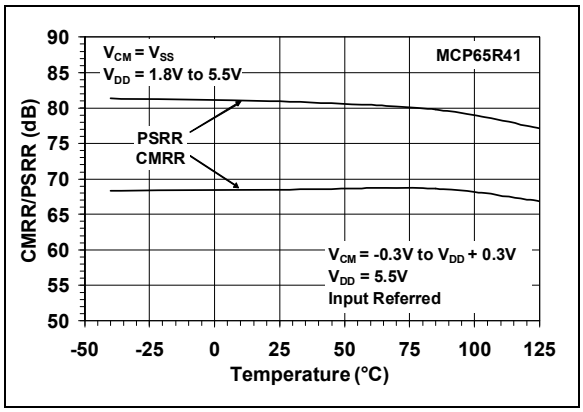


FIGURE 2-44: *Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.*

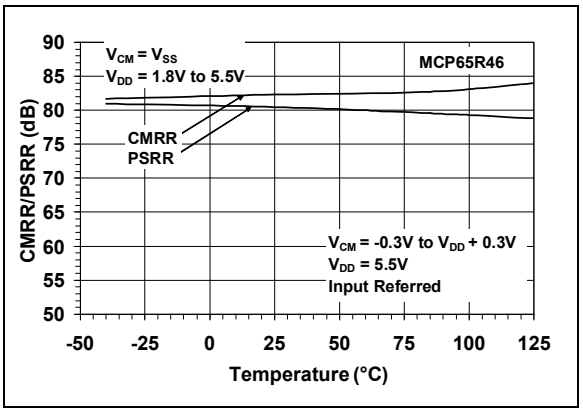


FIGURE 2-47: *Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.*

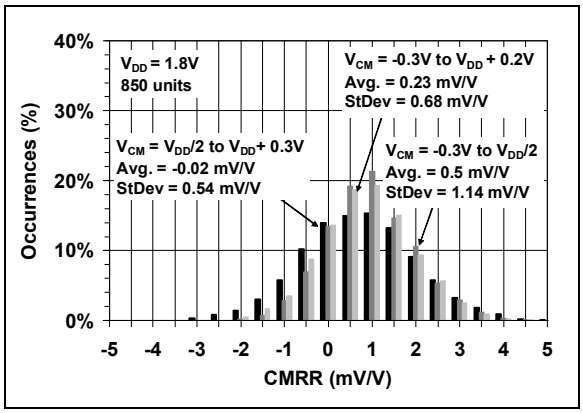


FIGURE 2-45: *Common-Mode Rejection Ratio.*

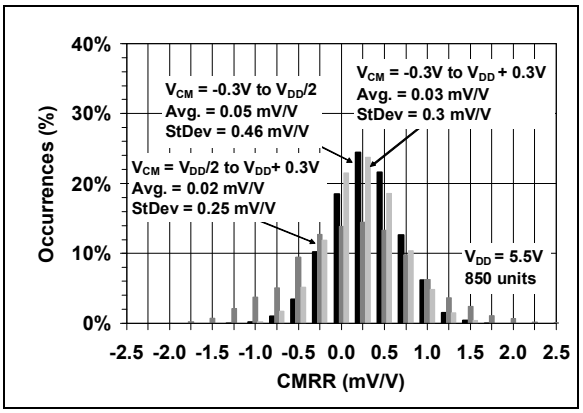


FIGURE 2-48: *Common-Mode Rejection Ratio.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

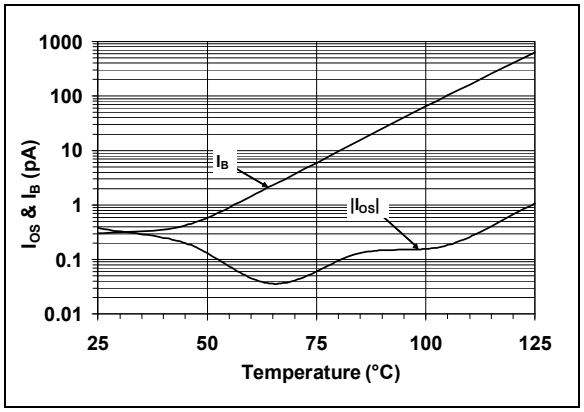


FIGURE 2-49: *Input Offset Current and Input Bias Current vs. Temperature.*

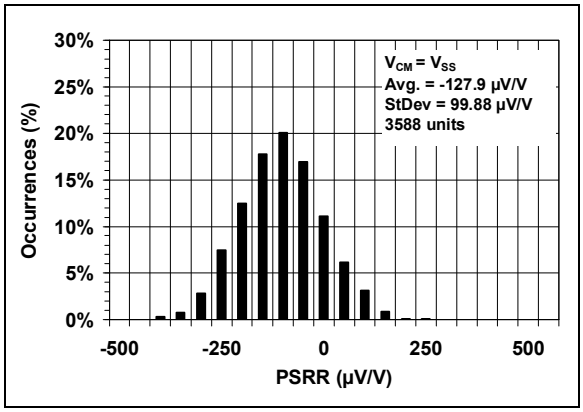


FIGURE 2-52: *Power Supply Rejection Ratio.*

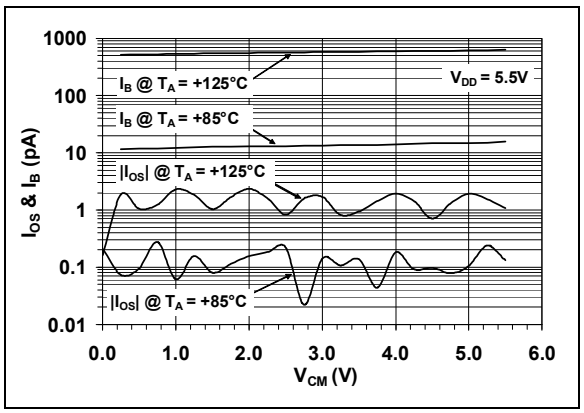


FIGURE 2-50: *Input Offset Current and Input Bias Current vs. Common-Mode Input Voltage vs. Temperature.*

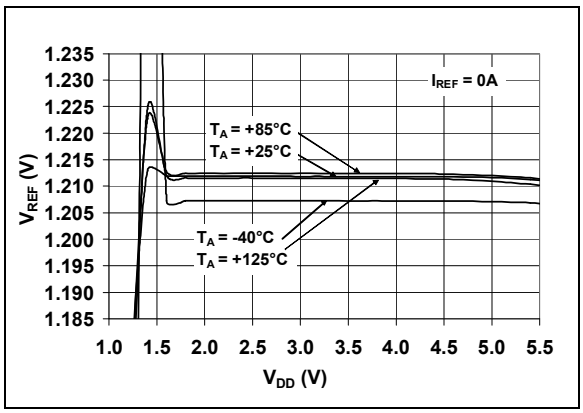


FIGURE 2-53: *V_{REF} vs. V_{DD}.*

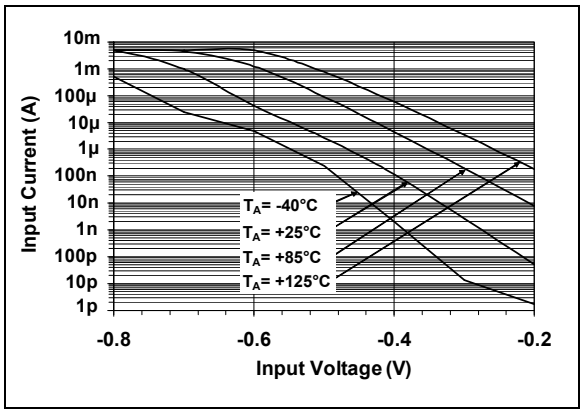


FIGURE 2-51: *Input Bias Current vs. Input Voltage below V_{SS} vs. Temperature.*

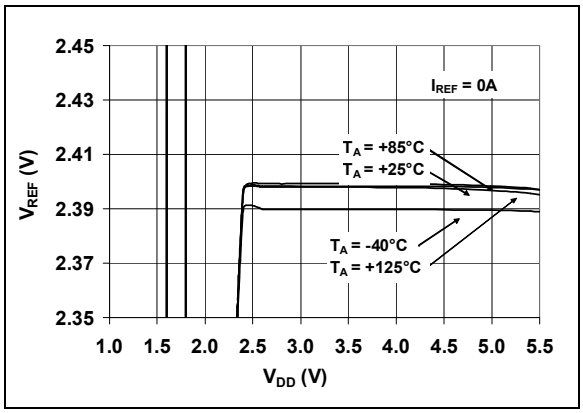


FIGURE 2-54: *V_{REF} vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 100 kΩ to V_{DD}/2 (**MCP65R41** only), $R_{Pull\text{-}Up}$ = 2.74 kΩ to V_{DD}/2 (**MCP65R46** only) and C_L = 50 pF.

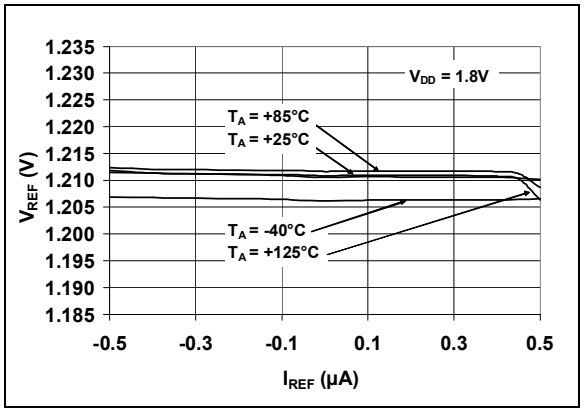


FIGURE 2-55: *V_{REF} vs. I_{REF} over Temperature.*

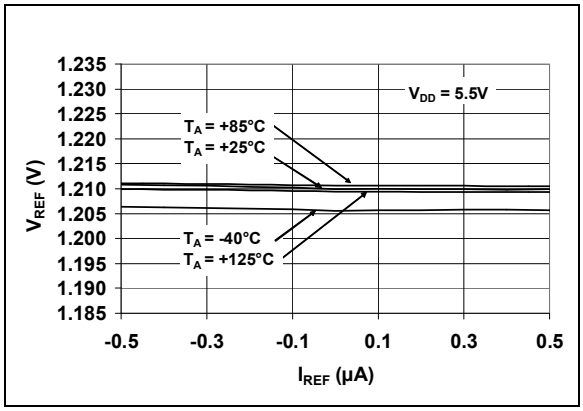


FIGURE 2-56: *V_{REF} vs. I_{REF} over Temperature.*

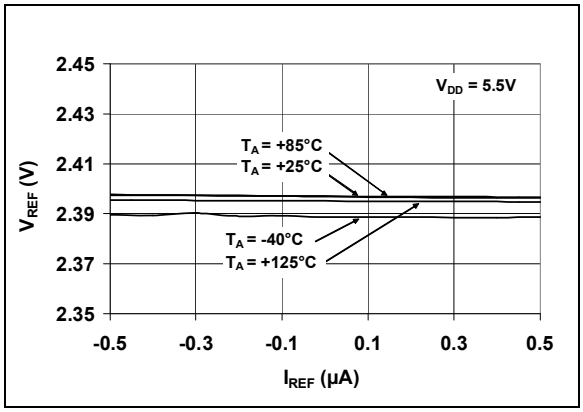


FIGURE 2-57: *V_{REF} vs. I_{REF} over Temperature.*

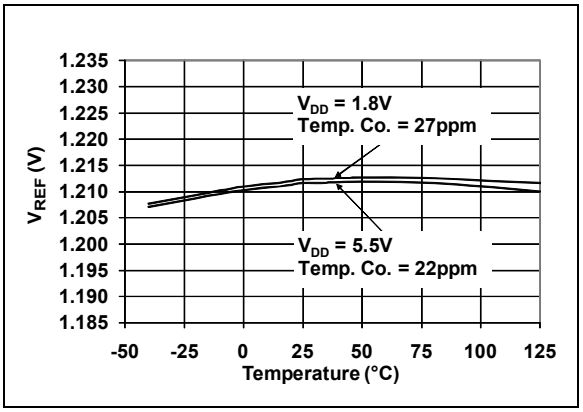


FIGURE 2-58: *V_{REF} vs. Temperature.*

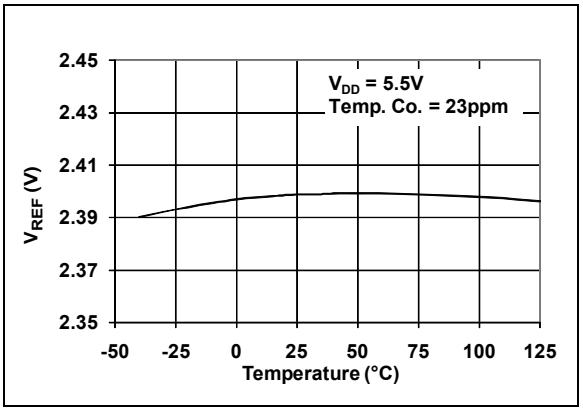


FIGURE 2-59: *V_{REF} vs. Temperature.*

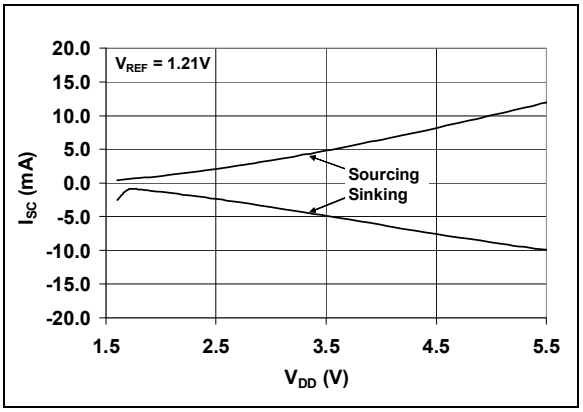


FIGURE 2-60: *Short Circuit Current vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 100 kΩ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up}$ = 2.74 kΩ to $V_{DD}/2$ (**MCP65R46** only) and C_L = 50 pF.

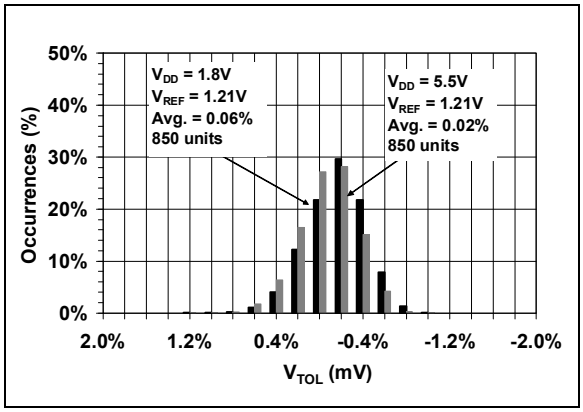


FIGURE 2-61: *Reference Voltage Tolerance.*

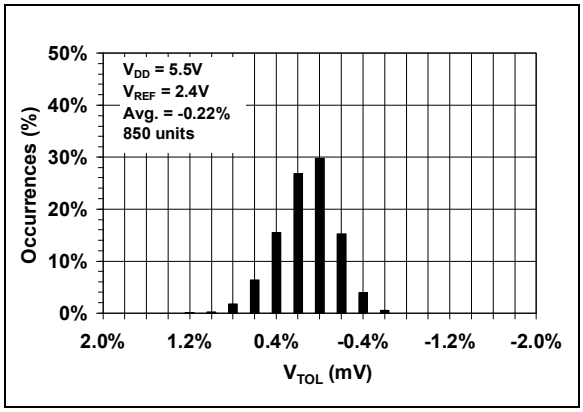


FIGURE 2-62: *Reference Voltage Tolerance.*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP65R41/6 SOT23-6	Symbol	Description
1	OUT	Digital Output
2	V_{SS}	Ground
3	$V_{IN}+$	Noninverting Input
4	$V_{IN}-$	Inverting Input
5	V_{REF}	Reference Voltage Output
6	V_{DD}	Positive Power Supply

3.1 Analog Inputs

The comparator noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 Digital Outputs

The comparator outputs are CMOS/TTL compatible push-pull and open-drain digital outputs. The push-pull is designed to directly interface to a CMOS/TTL compatible pin while the open-drain output is designed for level shifting and wired-OR interfaces.

3.3 Analog Outputs

The V_{REF} Output pin outputs a reference voltage of 1.21V or 2.4V.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.8V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These can share a bulk capacitor with the nearby analog parts (within 100 mm), but it is not required.

NOTES:

4.0 APPLICATIONS INFORMATION

The MCP65R41/6 family of push-pull and open-drain output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of high-speed applications requiring low power consumption.

4.1 Comparator Inputs

4.1.1 NORMAL OPERATION

The input stage of this family of devices uses three differential input stages in parallel: one operates at low input voltages, one at high input voltages, and one at mid input voltages. With this topology, the input voltage range is 0.3V above V_{DD} and 0.3V below V_{SS}, while providing low offset voltage throughout the Common mode range. The input offset voltage is measured at both V_{SS} - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The MCP65R41/6 family has internally-set hysteresis V_{HYST} that is small enough to maintain input offset accuracy, and large enough to eliminate the output chattering caused by the comparator's own input noise voltage E_{NI}. Figure 4-1 depicts this behavior. Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points.

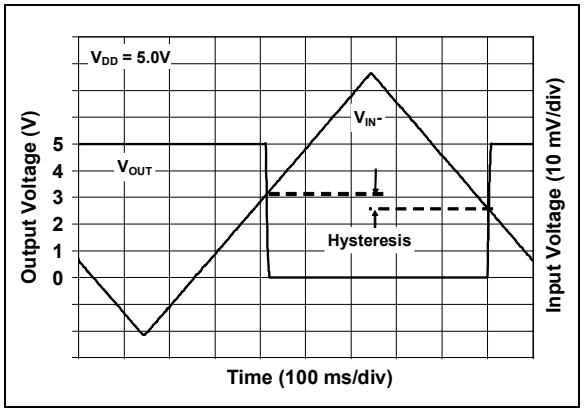


FIGURE 4-1: *The MCP65R41/6 Comparators' Internal Hysteresis Eliminates Output Chatter Caused by Input Noise Voltage.*

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize the input bias current (I_B). The input ESD diodes clamp the inputs when trying to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow a normal operation, and low enough to bypass the ESD events within the specified limits.

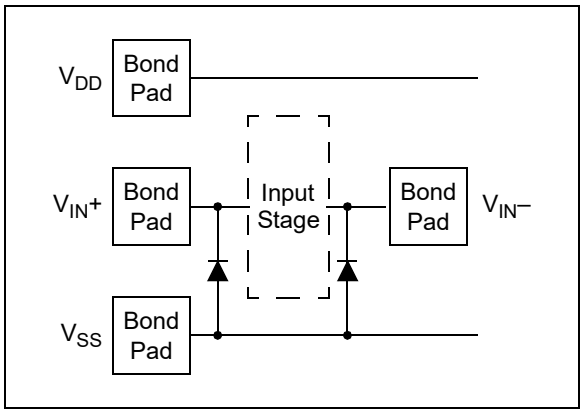
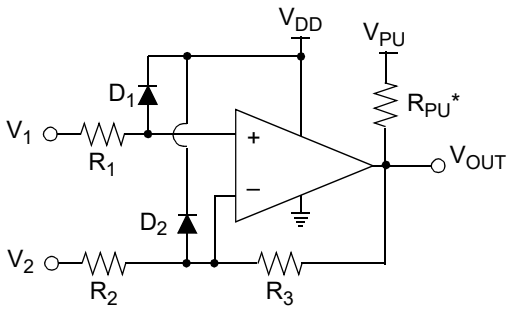


FIGURE 4-2: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these comparators, the circuit they are connected to limit the currents (and voltages) at the V_{IN}+ and V_{IN}- pins (see **Absolute Maximum Ratings†**). Figure 4-3 shows the recommended approach to protect these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pin. Diodes D_1 and D_2 prevent the input pin (V_{IN}+ and V_{IN}-) from going too far above V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 \geq \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 \geq \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

* Pull-up resistor required for the MCP65R46 only.

FIGURE 4-3: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistor then serves as an in-rush current limiter; the DC current into the input pins (V_{IN}+ and V_{IN}-) should be very small.

A significant amount of current can flow out of the inputs when the Common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 4-3. The applications that are high impedance may need to limit the usable voltage range.

4.1.3 PHASE REVERSAL

The MCP65R41/6 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give a rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply to supply) when the output is transitioned from high-to-low, or from low-to-high (see Figures 2-17 and 2-18 for more information).

4.3 Externally Set Hysteresis

A greater flexibility in selecting the hysteresis (or the input trip points) is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is preferable not to cycle between high and low states too frequently (e.g., air conditioner thermostatic controls). Output chatter also increases the dynamic supply current.

4.3.1 NONINVERTING CIRCUIT

Figure 4-4 shows a noninverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

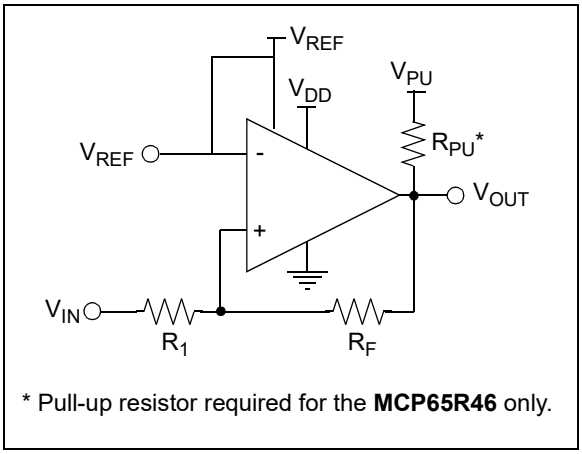


FIGURE 4-4: *Noninverting Circuit with Hysteresis for Single-Supply.*

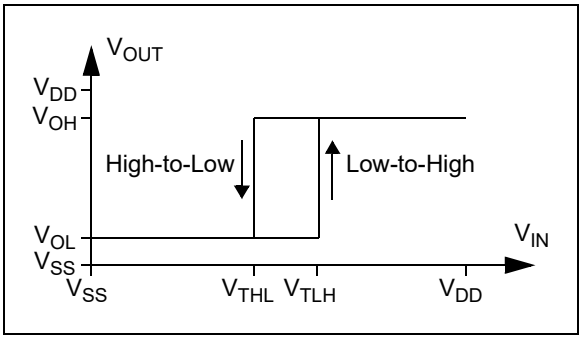


FIGURE 4-5: *Hysteresis Diagram for the Noninverting Circuit.*

The trip points for Figures 4-4 and 4-5 are:

EXAMPLE 4-1:

$$V_{TLH} = V_{REF}\left(1 + \frac{R_1}{R_F}\right) - V_{OL}\left(\frac{R_1}{R_F}\right)$$

$$V_{THL} = V_{REF}\left(1 + \frac{R_1}{R_F}\right) - V_{OH}\left(\frac{R_1}{R_F}\right)$$

Where:

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

4.3.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

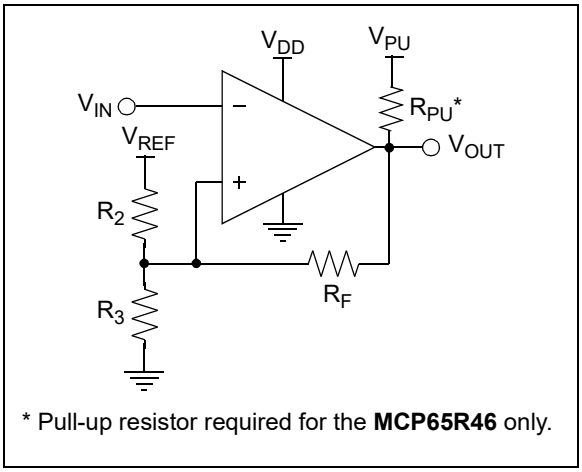


FIGURE 4-6: *Inverting Circuit with Hysteresis.*

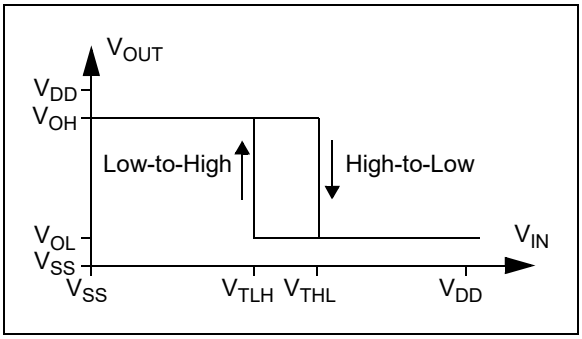
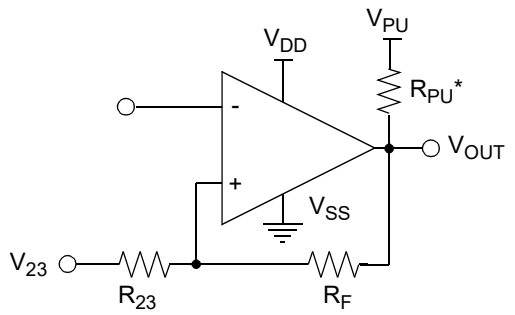


FIGURE 4-7: *Hysteresis Diagram for the Inverting Circuit.*

To determine the trip voltages (V_{TLH} and V_{THL}) for the circuit shown in Figure 4-6, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{REF}, as shown in Figure 4-8:



Where:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{REF}$$

* Pull-up resistor required for the **MCP65R46** only.

FIGURE 4-8: *Thevenin Equivalent Circuit.*

By using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION 4-1:

$$V_{THL} = V_{OH}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

$$V_{TLH} = V_{OL}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

Where:

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

Figures 2-25 and 2-28 can be used to determine the typical values for V_{OH} and V_{OL}.

4.4 Bypass Capacitors

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

4.5 Capacitive Loads

4.5.1 OUT PIN

Reasonable capacitive loads (i.e., logic gates) have little impact on the propagation delay (see Figure 2-34). The supply current increases with the increasing toggle frequency (Figure 2-22), especially with higher capacitive loads. The output slew rate and propagation delay performance will be reduced with higher capacitive loads.

4.5.2 V_{REF} PIN

The reference output is designed to interface to the comparator input pins, either directly or with some resistive network (e.g., a voltage divider network) with minimal capacitive load. The recommended capacitive load is 200 pF (typical). Capacitive loads greater than 2000 pF may cause the V_{REF} output to oscillate at power up.

4.6 PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other type of contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP65R41/6 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce the surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

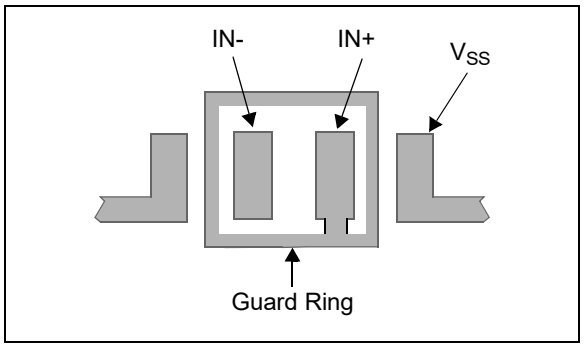


FIGURE 4-9: *Example of a Guard Ring Layout for Inverting Circuit.*

Use the following steps for an inverting configuration (Figures 4-6):

1. Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., $V_{DD}/2$ or ground).
2. Connect the inverting pin (V_{IN}-) to the input pad without touching the guard ring.

Use the following steps for a noninverting configuration (Figure 4-4):

1. Connect the noninverting pin (V_{IN}+) to the input pad without touching the guard ring.
2. Connect the guard ring to the inverting input pin (V_{IN}-).

4.7 Typical Applications

4.7.1 PRECISE COMPARATOR

Some applications require a higher DC precision. A simple way to address this need is using an amplifier (such as the MCP6041 – a 600 nA low power and 14 kHz bandwidth op amp) to gain-up the input signal before it reaches the comparator. Figure 4-10 shows an example of this approach, which also level shifts to V_{PU} using the Open-Drain option, the MCP65R46.

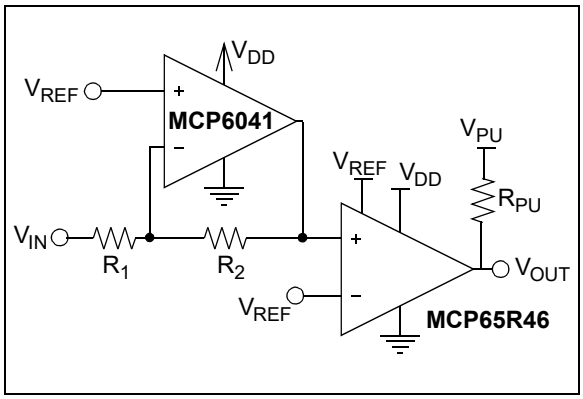


FIGURE 4-10: *Precise Inverting Comparator.*

4.7.2 BISTABLE MULTI-VIBRATOR

A simple bistable multi-vibrator design is shown in Figure 4-11. V_{REF} needs to be between ground and the maximum comparator internal V_{REF} of 2.4V to achieve oscillation. The output duty cycle changes with V_{REF}.

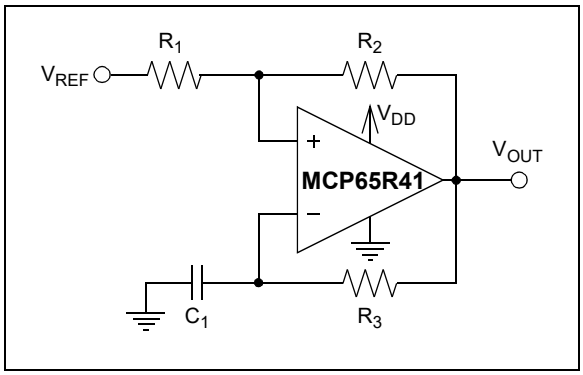


FIGURE 4-11: *Bistable Multi-Vibrator.*

4.7.3 OVERTEMPERATURE PROTECTION CIRCUIT

The MCP65R41 device can be used as an overtemperature protection circuit using a thermistor. The 2.4V V_{REF} can be used as stable reference to the thermistor, the alert threshold and hysteresis threshold. This is ideal for battery powered applications, where the change in temperature and output toggle thresholds would remain fixed as battery voltage decays over time.

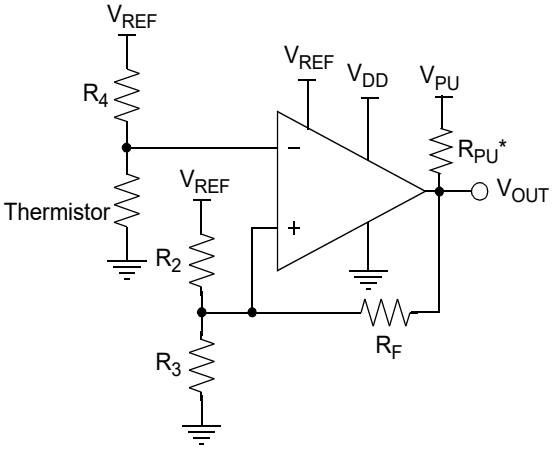
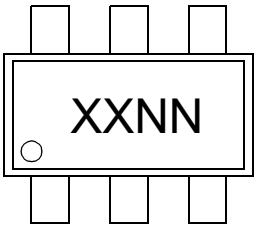


FIGURE 4-12: *Overtemperature Alert Circuit.*

5.0 PACKAGING INFORMATION

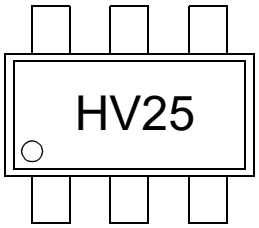
5.1 Package Marking Information

6-Lead SOT-23



Part Number	Code
MCP65R41T-1202E/CHY	HVNN
MCP65R41T-2402E/CHY	HWNN
MCP65R46T-1202E/CHY	HXNN
MCP65R46T-2402E/CHY	HYNN

Example

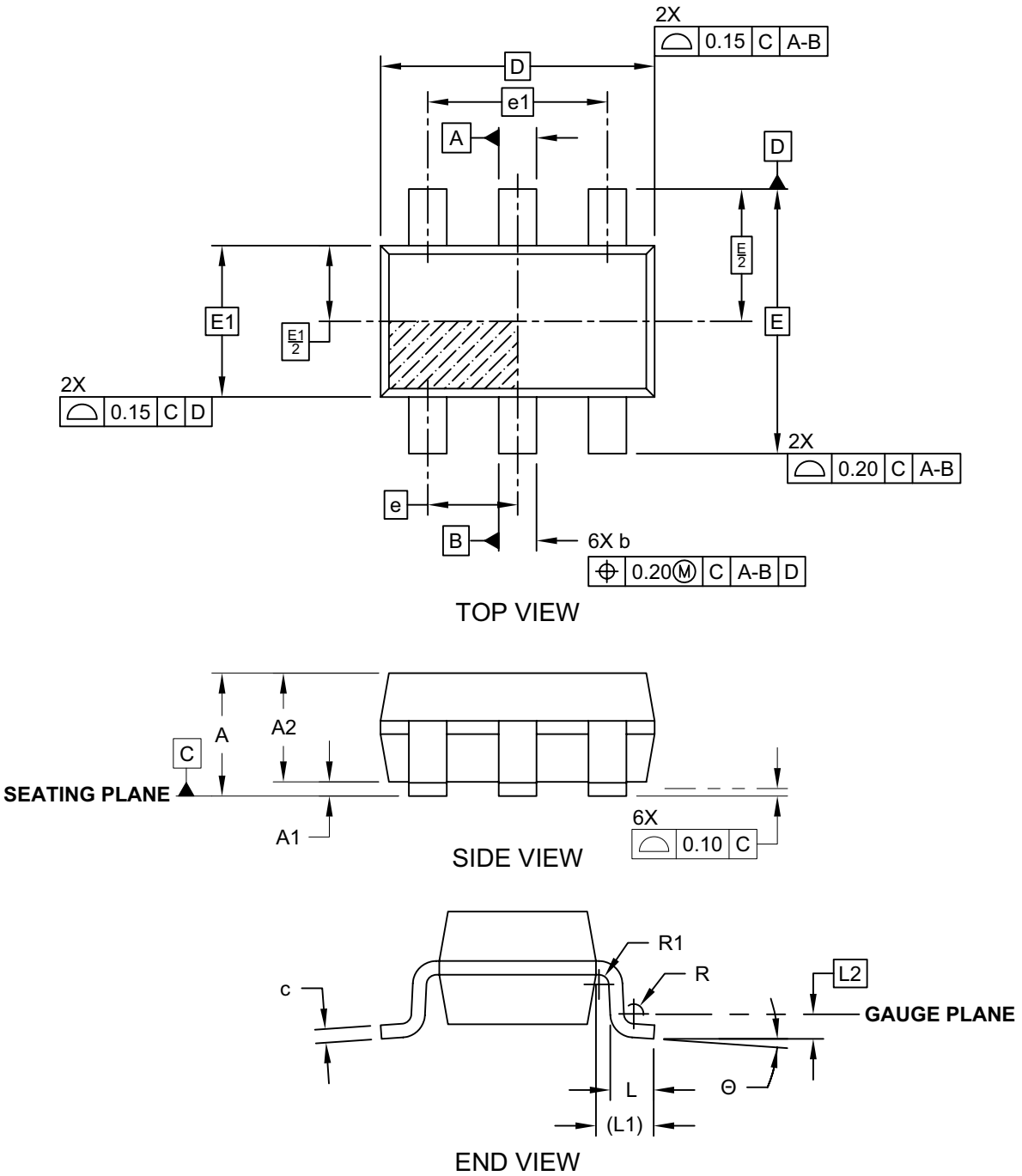


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

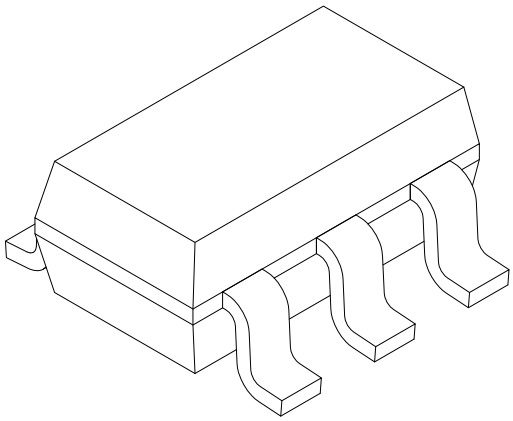
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-028C (CH) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Seating Plane to Gauge Plane	L1		0.25 BSC	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

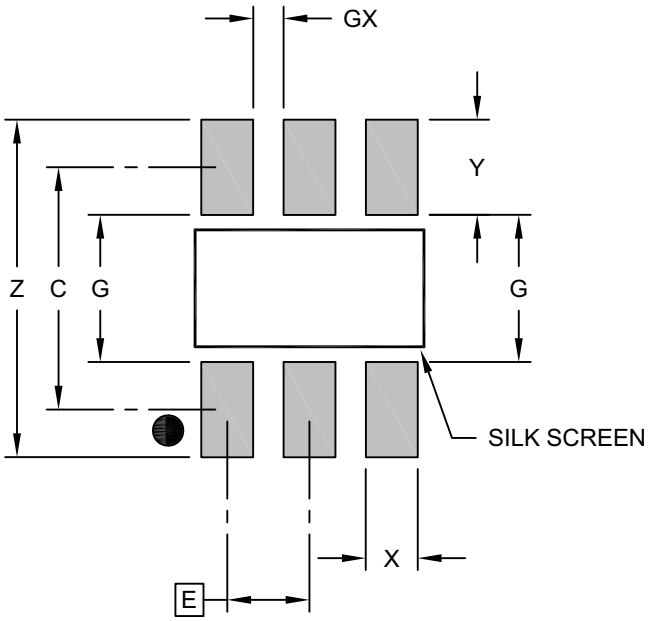
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028C (CH) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (CH, CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028B (CH)

APPENDIX A: REVISION HISTORY

Revision C (June 2020)

The following is the list of modifications:

1. Updated **DC Characteristics**.
2. Updated Figure 2-25 in **Section 2.0, Typical Performance Curves**.
3. Updated **Section 4.2, Push-Pull Output**.

Revision B (September 2011)

The following modification was made to this document:

- Updated the DC Characteristics table.

Revision A (December 2010)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-XX	XX	X	/XX
Device	Tape and	Reference Voltage	Reference Tolerance	Temperature Range	Package

Device:	MCP65R41T: Push-Pull Output Comparator MCP65R46T: Open-Drain Output Comparator
Reference Voltage:	12 = 1.21V (typical) Initial Reference Voltage 24 = 2.4V (typical) Initial Reference Voltage
Reference Tolerance:	02 = 2% Reference Voltage Tolerance
Temperature Range:	E = -40°C to+125°C(Extended)
Package:	CHY= Plastic Small Outline Transistor, 6-Lead

Examples:

a) MCP65R41T-1202E/CHY: Push-Pull Output, 1.2VREF, Tape and Reel, 6LD SOT-23 package

b) MCP65R41T-2402E/CHY: Push-Pull Output, 2.4VREF, Tape and Reel, 6LD SOT-23 package

c) MCP65R46T-1202E/CHY: Open-Drain Output, 1.2VREF, Tape and Reel, 6LD SOT-23 package

d) MCP65R46T-2402E/CHY: Open-Drain Output, 2.4VREF,Tape and Reel, 6LD SOT-23 package.

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