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1 MCF51JM128 Family Configurations

1.1 Device Comparison

The MCF51JM128 series consists of the devices compared in Table 1.

Table 1. MCF51JM128 Series Device Comparison

Feature	MCF51JM128			MCF51JM64			MCF51JM32		
	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin
Flash memory size (KB)	128			64			32		
RAM size (KB)	16			16			16		
V1 ColdFire core with BDM (background debug module)	Yes								
ACMP (analog comparator)	Yes								
ADC channels (12-bit)	12		8	12		8	12		8
CAN (controller area network)	Yes	Yes	No	Yes	Yes	No	Yes	Yes	No
RNGA + CAU	Yes[1]								
CMT (carrier modulator timer)	Yes								
COP (computer operating properly)	Yes								
IIC1 (inter-integrated circuit)	Yes								
IIC2	Yes	No		Yes	No		Yes	No	
IRQ (interrupt request input)	Yes								
KBI (keyboard interrupts)	8	8	6	8	8	6	8	8	6
LVD (low-voltage detector)	Yes								
MCG (multipurpose clock generator)	Yes								
Port I/O[2]	66	51	33	66	51	33	66	51	33
RGPIO (rapid general-purpose I/O)	16	6	0	16	6	0	16	6	0
RTC (real-time counter)	Yes								
SCI1 (serial communications interface)	Yes								
SCI2	Yes								
SPI1 (serial peripheral interface)	Yes								
SPI2	Yes								
TPM1 (timer/pulse-width modulator) channels	6	6	4	6	6	4	6	6	4
TPM2 channels	2								
USBOTG (USB On-The-Go dual-role controller)	Yes								
XOSC (crystal oscillator)	Yes								

[1] Only existed on special part number

2 Up to 16 pins on Ports A, H, and J are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51JM128 series pins and modules.

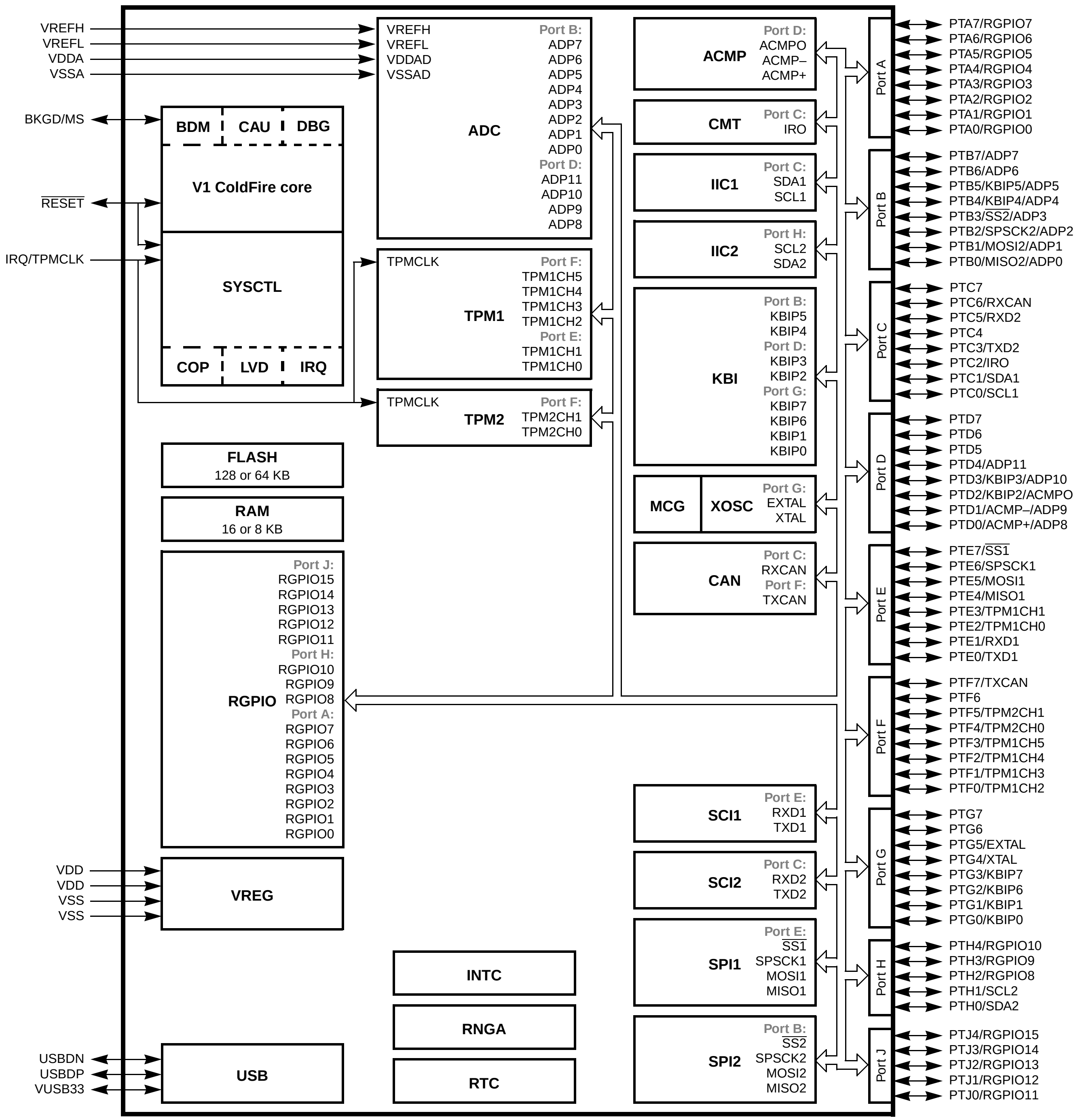


Figure 1. MCF51JM128 Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51JM128 series.

Table 2. MCF51JM128 Series Functional Units

Unit	Function
CF1CORE (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides a single-pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
SYSCTL (system control)	Provides LVD, COP, external interrupt request, and so on
FLASH (flash memory)	Provides storage for program code and constants
RAM (random-access memory)	Provides storage for program code, constants, and variables
RGPIO (rapid general-purpose input/output)	Allows I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management throughout the device
USBOTG (USB On-The-Go)	Supports the USB On-The-Go dual-role controller
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
TPM1, TPM2 (timer/pulse-width modulators)	Provide a variety of timing-based features
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
CAU (cryptographic acceleration unit)	Co-processor support for DES, 3DES, AES, MD5, and SHA-1
RNGA (random number generator accelerator)	32-bit random number generator that complies with FIPS-140
RTC (real-time counter)	Provides a constant-time base with optional interrupt
ACMP (analog comparator)	Compares two analog inputs
CMT (carrier modulator timer)	Infrared output used for the Remote Controller
IIC1, IIC2 (inter-integrated circuits)	Supports the standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
XOSC (crystal oscillator)	Supports low/high range crystals
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs that can support RS-232 and LIN protocols
SPI1, SPI2 (serial peripheral interfaces)	Provide a 4-pin synchronous serial interface

1.3.1 Feature List

- 32-bit Version 1 ColdFire Central Processor Unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Performance (Dhrystone 2.1):
    - 0.94 Dhrystone 2.1 MIPS per MHz when running from internal RAM
    - 0.76 Dhrystone 2.1 MIPS per MHz when running from flash
  - Implements Instruction Set Revision C (ISA_C)
  - Supports up to 30 peripheral interrupt requests and seven software interrupts
- On-chip memory
  - Up to 128 KB Flash memory with read/program/erase over full operating voltage and temperature range
  - Up to 16 KB static random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-saving modes
  - Two low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; this behavior allows clocks to remain enabled to specific perhipherals in Stop3 mode
  - Very lower power real-time counter for use in run, wait, and stop modes with internal and external clock sources
- Four Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - FLL/PLL controlled by internal or external reference
  - Trimmable internal reference allows 0.2% resolution and 2% deviation
- System protection features
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire Background debug interface
  - 4 Program Counters plus two address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
  - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Universal Serial Bus (USB) On-The-Go dual-role controller
  - Full-speed USB device controller
    - Fully compliant with USB specification 1.1 and 2.0
    - 16 bidirectional endpoints, with double buffering to provide the maximum throughput
    - Supports control, bulk, interrupt, and isochronous endpoints
    - Supports bus-powered capability with low-power consumption
  - Full-speed / low-speed host controller
    - Host mode allows control, bulk, interrupt, and isochronous transfers
  - OTG protocol logic
  - On-chip USB transceiver
  - On-chip 3.3 V USB regulator and pull-up resistors save system cost

- Controller area network (MSCAN)
  - Implementation of the CAN protocol — Version 2.0A/B
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization using a “local priority” concept
  - Flexible maskable identifier filter programmable as 2x32-bit, 4x16-bit, or 8x8-bit
  - Programmable wakeup functionality with integrated low-pass filter
  - Programmable loopback mode supports self-test operation
  - Programmable bus-off recovery functionality
  - Internal timer for time-stamping of received and transmitted messages
- Cryptographic acceleration unit (CAU)
  - Co-processor support of DES, 3DES, AES, MD5, and SHA-1
- Random number generator accelerator (RNGA)
  - 32-bit random number generator that complies with FIPS-140
- Analog-to-digital converter (ADC)
  - 12-channel, 12-bit resolution
  - Output formatted in 12-, 10-, or 8-bit right-justified format
  - Single or continuous conversion, and selectable asynchronous hardware conversion trigger
  - Operation in Stop3 mode
  - Automatic compare function
  - Internal temperature sensor
- Analog comparators (ACMP)
  - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - Option to compare to fixed internal bandgap reference voltage
  - Option to route output to TPM module
  - Operation in Stop3 mode
- Inter-integrated circuit (IIC)
  - Up to 100 kbps with maximum bus loading
  - Multi-master operation
  - Programmable slave address
  - Supports broadcast mode and 10-bit address extension
- Serial communications interfaces (SCI)
  - Two SCIs with full-duplex, non-return-to-zero (NRZ) format
  - LIN master extended break generation
  - LIN slave extended break detection
  - Programmable 8-bit or 9-bit character length
  - Wake up on active edge
- Serial peripheral interfaces (SPI)
  - Two serial peripheral interfaces with full-duplex or single-wire bidirectional
  - Double-buffered transmit and receive
  - Programmable transmit bit rate, phase, polarity, and Slave Select output
  - MSB-first or LSB-first shifting
- Timer/pulse width modulator (TPM)
  - 16-bit free-running or modulo up/down count operation
  - Up to eight channels, where each channel can be an input capture, output compare, or edge-aligned PWM
  - One interrupt per channel plus terminal count interrupt

- RTC
  - 8-bit modulus counter with binary- or decimal-based prescaler
  - External clock source for precise time base, time-of-day, calendar or task scheduling functions
  - Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Carrier modulator timer (CMT)
  - carrier generator, modulator, and transmitter drive the infrared out (IRO) pin
  - operation in independent high/low time control, baseband, FSK, and direct IRO control modes
- Input/Output
  - 66 GPIOs
  - Eight keyboard interrupt pins with selectable polarity
  - Hysteresis and configurable pull-up device on all input pins; configurable slew rate and drive strength on all output pins
  - 16 bits of Rapid GPIO connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51JM128EVLK	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128VLK	MCF51JM128 ColdFire Microcontroller	128 / 16	80 LQFP	–40 to +105 °C
MCF51JM128EVLH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128VLH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 LQFP	–40 to +105 °C
MCF51JM128EVQH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128VQH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 QFP	–40 to +105 °C
MCF51JM128EVLD	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM128VLD	MCF51JM128 ColdFire Microcontroller	128 / 16	44 LQFP	–40 to +105 °C
MCF51JM64EVLK	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64VLK	MCF51JM64 ColdFire Microcontroller	64 / 16	80 LQFP	–40 to +105 °C
MCF51JM64EVLH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64VLH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 LQFP	–40 to +105 °C
MCF51JM64EVQH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 QFP	–40 to +105 °C
MCF51JM64VQH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 QFP	–40 to +105 °C

Table 3. Orderable Part Number Summary (continued)

MCF51JM64EVLD	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM64VLD	MCF51JM64 ColdFire Microcontroller	64 / 16	44 LQFP	–40 to +105 °C
MCF51JM32EVLK	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32VLK	MCF51JM32 ColdFire Microcontroller	32 / 16	80 LQFP	–40 to +105 °C
MCF51JM32EVLH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32VLH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 LQFP	–40 to +105 °C
MCF51JM32EVQH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32VQH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 QFP	–40 to +105 °C
MCF51JM32EVLD	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	44 LQFP	–40 to +105 °C
MCF51JM32VLD	MCF51JM32 ColdFire Microcontroller	32 / 16	44 LQFP	–40 to +105 °C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

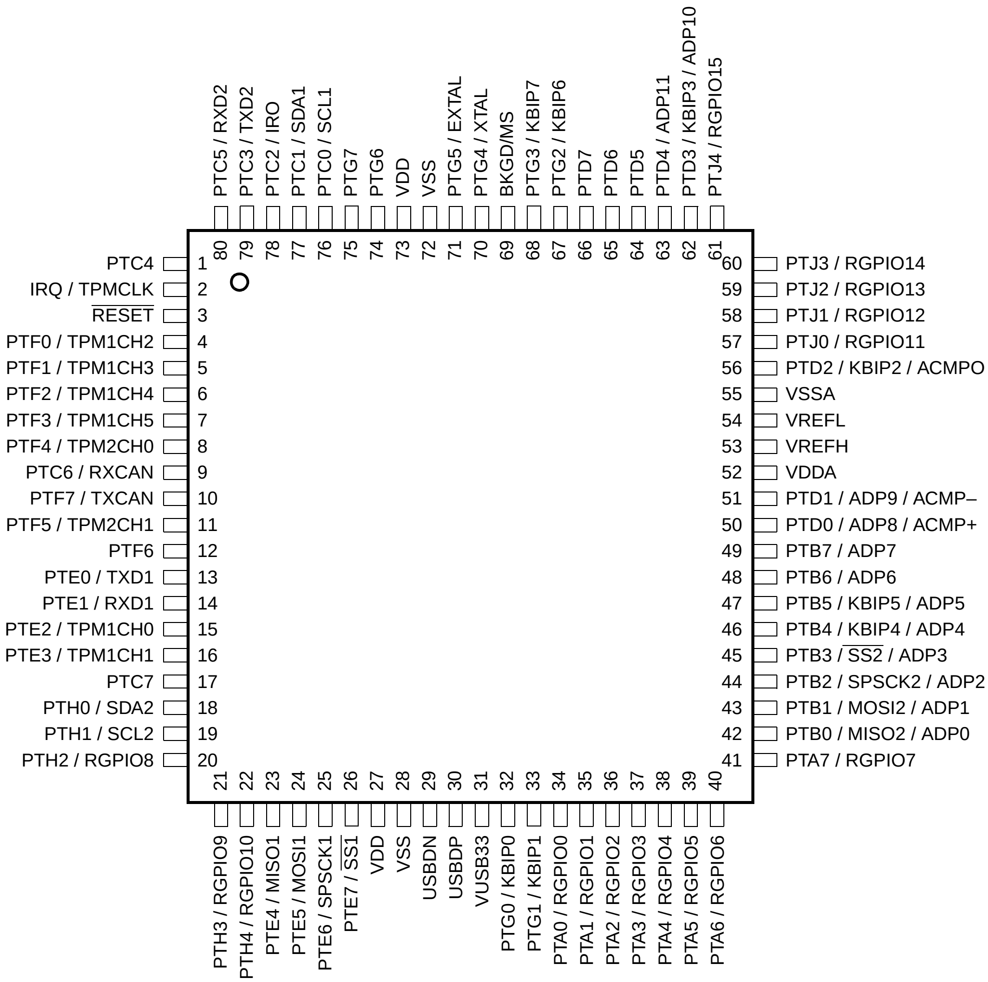


Figure 2. 80-pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

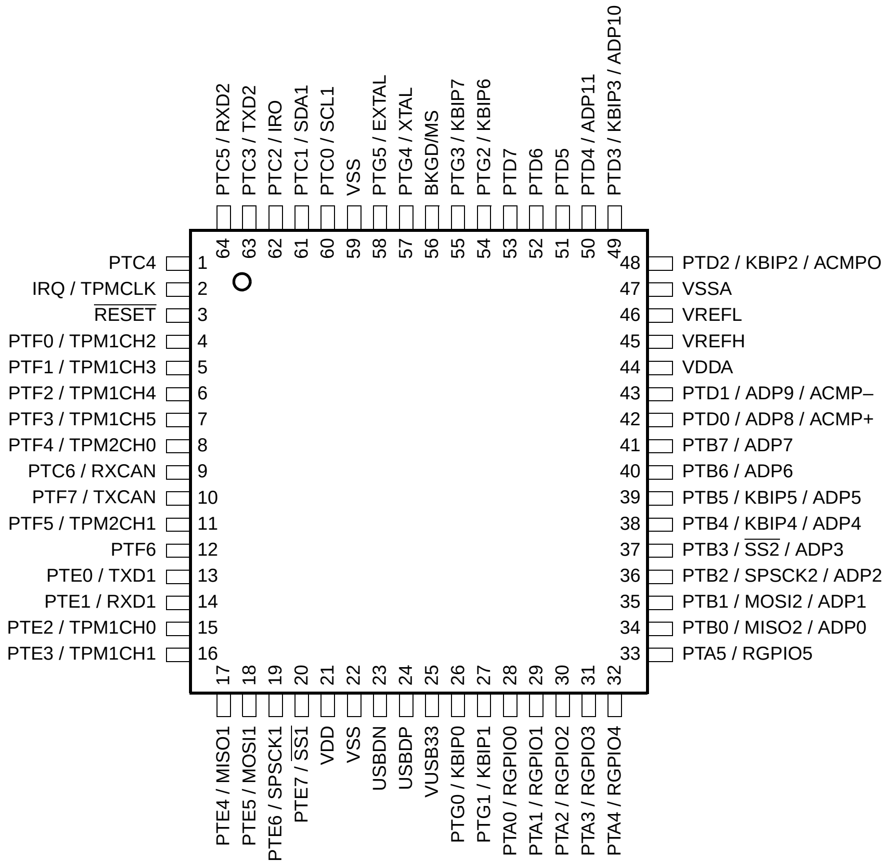


Figure 3. 64-pin QFP and LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

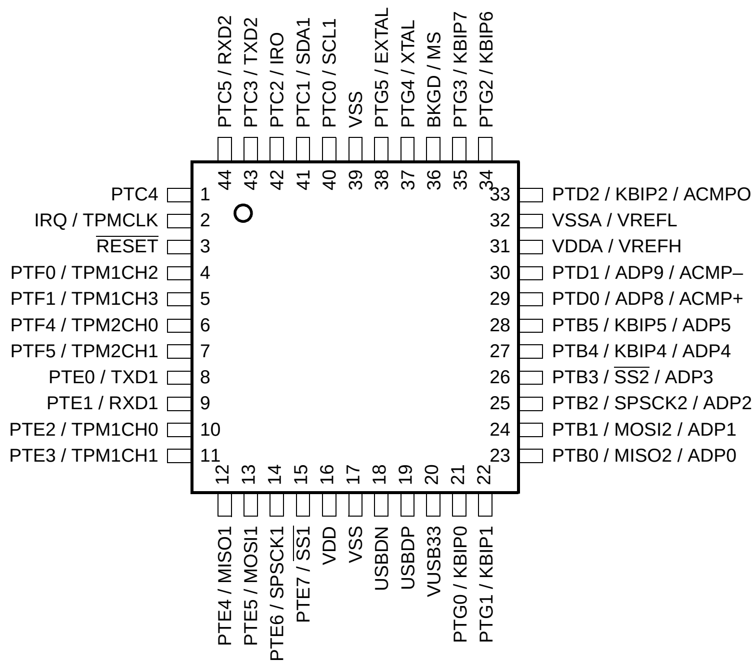


Figure 4. 44-pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Assignments by Package and Pin Sharing Priority

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
1	1	1	PTC4		—
2	2	2	—	IRQ	TPMCLK
3	3	3	—	RESET	—
4	4	4	PTF0	TPM1CH2	—
5	5	5	PTF1	TPM1CH3	—
6	6	—	PTF2	TPM1CH4	—
7	7	—	PTF3	TPM1CH5	—
8	8	6	PTF4	TPM2CH0	BUSCLK_OUT
9	9	—	PTC6	RXCAN	—
10	10	—	PTF7	TXCAN	—
11	11	7	PTF5	TPM2CH1	—
12	12	—	PTF6	—	—
13	13	8	PTE0	TXD1	—
14	14	9	PTE1	RXD1	—
15	15	10	PTE2	TPM1CH0	—

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
16	16	11	PTE3	TPM1CH1	—
17	—	—	PTC7	—	—
18	—	—	PTH0	SDA2	—
19	—	—	PTH1	SCL2	—
20	—	—	PTH2	RGPIO8	—
21	—	—	PTH3	RGPIO9	—
22	—	—	PTH4	RGPIO10	—
23	17	12	PTE4	MISO1	—
24	18	13	PTE5	MOSI1	—
25	19	14	PTE6	SPSCK1	—
26	20	15	PTE7	$\overline{\text{SS1}}$	—
27	21	16	—	—	VDD
28	22	17	—	—	VSS
29	23	18	—	—	USBDN
30	24	19	—	—	USBDP
31	25	20	—	—	VUSB33
32	26	21	PTG0	KBIP0	USB_ALT_CLK
33	27	22	PTG1	KBIP1	—
34	28	—	PTA0	RGPIO0	USB_SESSVLD
35	29	—	PTA1	RGPIO1	USB_SESSEND
36	30	—	PTA2	RGPIO2	USB_VBUSVLD
37	31	—	PTA3	RGPIO3	USB_PULLUP(D+)
38	32	—	PTA4	RGPIO4	USB_DM_DOWN
39	33	—	PTA5	RGPIO5	USB_DP_DOWN
40	—	—	PTA6	RGPIO6	USB_ID
41	—	—	PTA7	RGPIO7	—
42	34	23	PTB0	MISO2	ADP0
43	35	24	PTB1	MOSI2	ADP1
44	36	25	PTB2	SPSCK2	ADP2
45	37	26	PTB3	$\overline{\text{SS2}}$	ADP3
46	38	27	PTB4	KBIP4	ADP4
47	39	28	PTB5	KBIP5	ADP5
48	40	—	PTB6	ADP6	—

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest **Priority** --> Highest		
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
49	41	—	PTB7	ADP7	—
50	42	29	PTD0	ADP8	ACMP+
51	43	30	PTD1	ADP9	ACMP–
52	44	31	—	—	VDDA
53	45		—	—	VREFH
54	46	32	—	—	VREFL
55	47		—	—	VSSA
56	48	33	PTD2	KBIP2	ACMPO
57	—	—	PTJ0	RGPIO11	—
58	—	—	PTJ1	RGPIO12	—
59	—	—	PTJ2	RGPIO13	—
60	—	—	PTJ3	RGPIO14	—
61	—	—	PTJ4	RGPIO15	—
62	49	—	PTD3	KBIP3	ADP10
63	50	—	PTD4	ADP11	—
64	51	—	PTD5	—	—
65	52	—	PTD6	—	—
66	53	—	PTD7	—	—
67	54	34	PTG2	KBIP6	—
68	55	35	PTG3	KBIP7	—
69	56	36	—	BKGD	MS
70	57	37	PTG4	XTAL	
71	58	38	PTG5	EXTAL	
72	59	39	—	—	VSS
73	—	—	—	—	VDD
74	—	—	PTG6	—	—
75	—	—	PTG7	—	—
76	60	40	PTC0	SCL1	—
77	61	41	PTC1	SDA1	—
78	62	42	PTC2	IRO	—
79	63	43	PTC3	TXD2	—
80	64	44	PTC5	RXD2	—

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JM128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled C in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to + 5.8	V
Input voltage	V_{In}	– 0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to +150	°C
Maximum junction temperature	T_J	150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunt current is greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples: if no system clock is present or if the clock rate is low, which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is small.

Table 7. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to +105	°C
Thermal resistance [1,2,3,4]		θ_{JA}		°C/W
80-pin LQFP	1s		52	
	2s2p		40	
64-pin LQFP	1s		65	
	2s2p		47	
64-pin QFP	1s		54	
	2s2p		40	
44-pin LQFP	1s		69	
	2s2p		48	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

[3] 1s - Single Layer Board, one signal layer
[4] 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °Cθ_{JA} = Package thermal resistance, junction-to-ambient, °C/WP_D = P_{int} + $P_{I/O}$$P_{int}$ = $I_{DD} \times V_{DD}$, Watts — chip internal power$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	+/– 2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	+/– 500	—	V
3	Latch-up Current at T_A = 105°C	I_{LAT}	+/– 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Operating voltage[2]		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 4mA 3 V, I_{Load} = 2 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA	V_{OL}		 — — — —	 1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 15 mA 3 V, I_{Load} = 8 mA 5 V, I_{Load} = 8 mA 3 V, I_{Load} = 4 mA			 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs V_{DD} = 5V V_{DD} = 3V	V_{IH}	 3.25 2.10	 — —	 — —	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
7	P	Input low voltage; all digital inputs V_{DD} = 5V V_{DD} = 3V	V_{IL}	—	—	1.75 1.05	V
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13		Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	900 1425	1300 2400	1575 3090	kΩ
14	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	D	RAM retention voltage[6]	V_{RAM}	—	0.6	1.0	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	μs
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV

[1] Typical values are based on characterization data at 25°C unless otherwise stated.
[2] Operating voltage with USB enabled can be found in Section 2.14, "USB Electricals."
[3] Measured with $V_{In} = V_{DD}$ or V_{SS}.
[4] Measured with $V_{In} = V_{SS}$.
[5] Measured with $V_{In} = V_{DD}$.
[6] This is the voltage below which the contents of RAM are not guaranteed to be maintained.

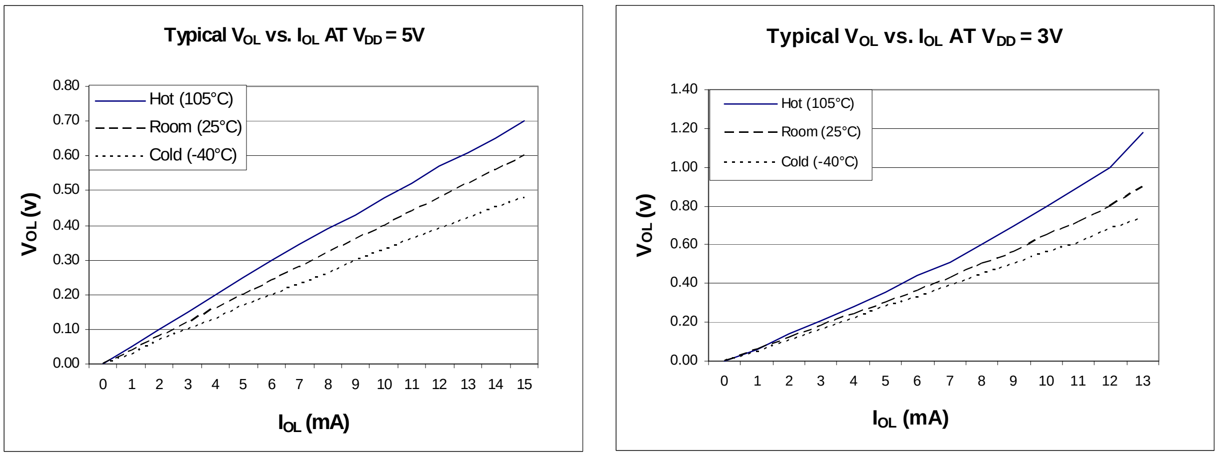


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

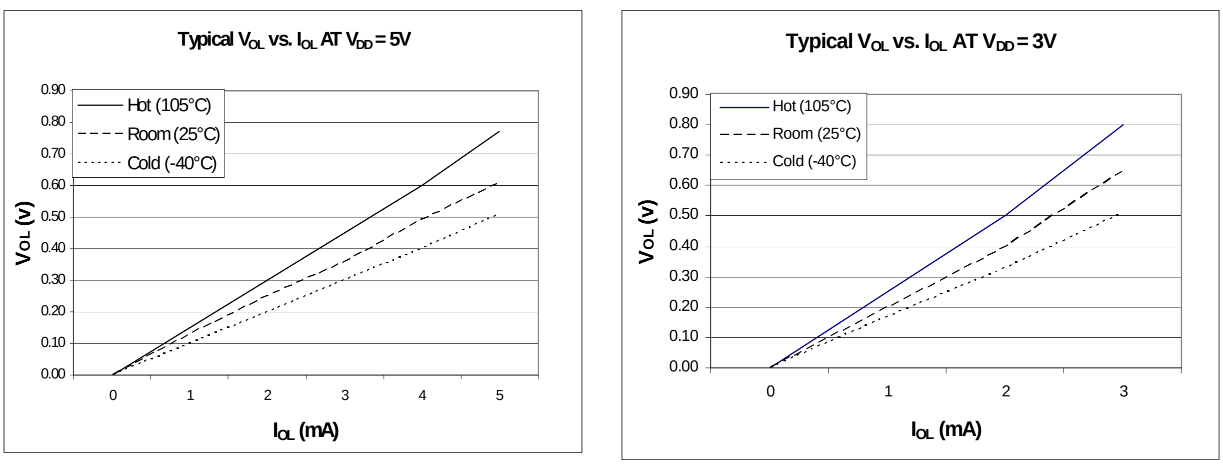


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

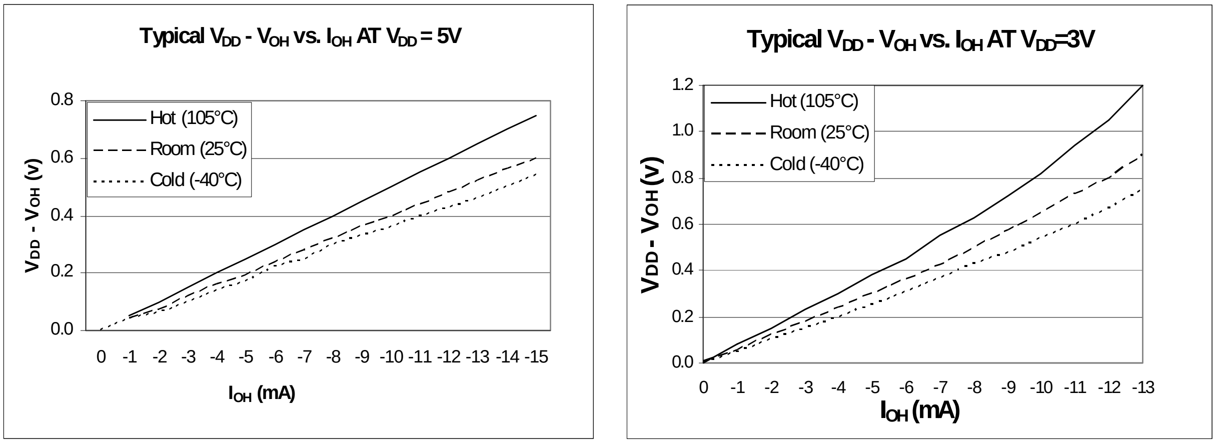


Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

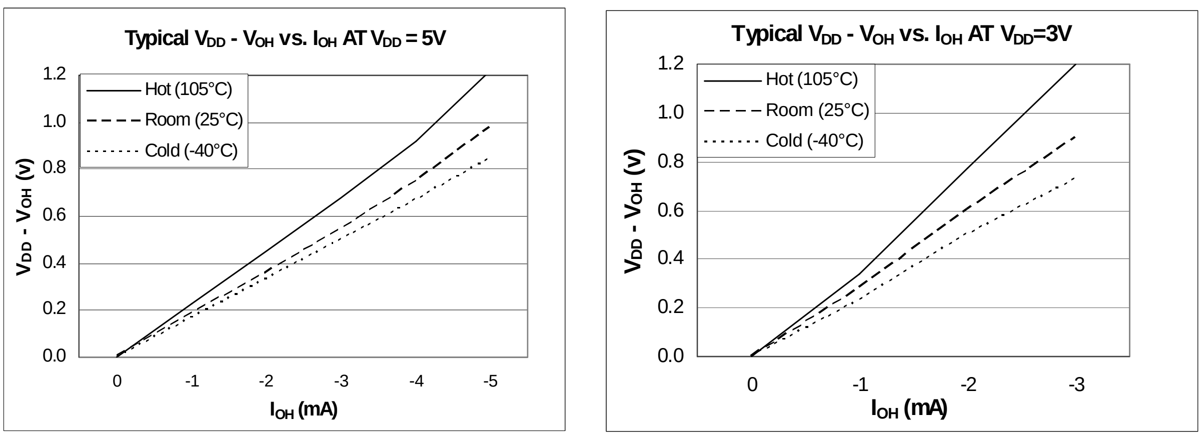


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)		5	4.0	7	mA
				3	4.0	7	
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	19	30	mA
				3	18.7	30	
3	C	Run supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)		5	45	70	mA
				3	44	70	

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
4	C	Wait mode supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	WI_{DD}	5	2.03	3	mA
				3	2	3	
5	C	Wait mode supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	7.73	12	mA
				3	7.7	12	
6	C	Wait mode supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz)		5	22	30	mA
				3	21.9	30	
7	C	Stop2 mode supply current –40 °C 25 °C 105 °C	$S2I_{DD}$	5	1.35	3 3 35	µA
		–40 °C 25 °C 105 °C		3	1.25	3 3 35	µA
8	P	Stop3 mode supply current –40 °C 25 °C 105 °C	$S3I_{DD}$	5	1.41	3 3 35	µA
		–40 °C 25 °C 105 °C		3	1.35	3 3 35	µA
9	C	Stop4 mode supply current –40 °C 25 °C 105 °C	$S4I_{DD}$	5	106	200	µA
		–40 °C 25 °C 105 °C		3	96	200	µA
10	P	RTC adder to stop2 or stop3[4], 25°C	$S23I_{DDRTC}$	5	300	—	nA
				3	300	—	nA
11	P	Adder to stop3 for oscillator enabled[5] (ERCLKEN =1 and EREFSTEN = 1)	$S23I_{DDOSC}$	5	5	—	µA
				3	5	—	µA

1 Typicals are measured at 25°C.
2 Values given here are preliminary estimates prior to completing characterization.
3 All modules' clocks are switched on, code runs from flash, in FEI mode, and there are no DC loads on port pins.
4 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.
5 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0)

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1		Supply voltage	V_{DD}	2.7	—	5.5	V
2		Supply current (active)	I_{DDAC}	—	20	35	μA
3		Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4		Analog input offset voltage	V_{AIO}		20	40	mV
5		Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV
6		Analog input leakage current	I_{ALKG}	--	--	1.0	μA
7		Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs
8		Bandgap Voltage Reference Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C	V_{BG}	1.19	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} (V_{DD}-V_{DDA})[2]	ΔV_{DDA}	–100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	–100	0	+100	mV	
Ref Voltage High		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	3	5	kΩ	
Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

[1] Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

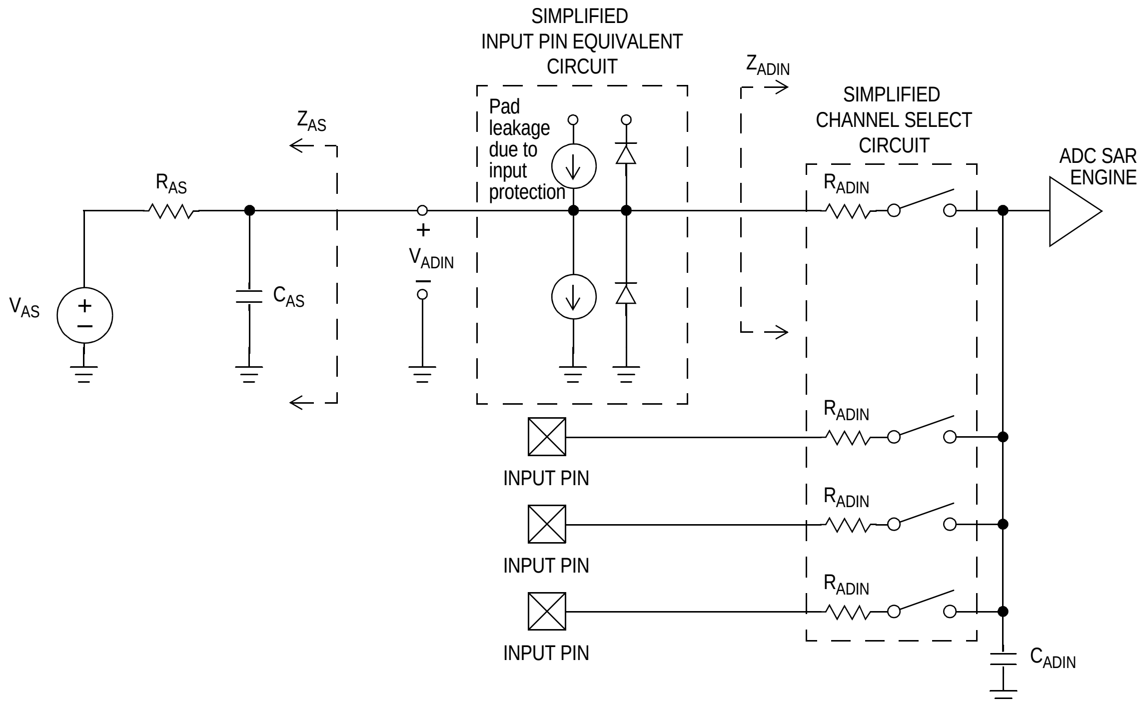


Figure 9. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	133	—	µA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	218	—	µA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	327	—	µA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		P	I_{DDAD}	—	0.582	1	mA	
Supply Current	Stop, Reset, Module Off		I_{DDAD}	—	0.011	1	µA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	T	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)			1.25	2	3.3		

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	T	t_{ADC}	—	20	—	ADCK cycles	See Table 9 for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	T		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	$V_{ADIN} = V_{SSAD}$
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1	—	LSB[2]	$V_{ADIN} = V_{DDAD}$
	10 bit mode	T		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
	10 bit mode			—	±0.2	±2.5		
	8 bit mode			—	±0.1	±1		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	
Temp Sensor Slope	-40°C - 25°C	D	m	—	3.266	—	mV/°C	
	25°C - 125°C			—	3.638	—		

1 Typical values assume V_{DDA} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105°C Ambient)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1		Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode [2] • High range (RANGE = 1) PEE or PBE mode [3] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	f_{lo} $f_{hi\text{-}fll}$ $f_{hi\text{-}pll}$ $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	32 1 1 1 1	— — — — —	38.4 5 16 16 8	kHz MHz MHz MHz MHz
2		Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3		Feedback resistor • Low range (32 kHz to 38.4 kHz) • High range (1 MHz to 16 MHz)	R_F		10 1		MΩ MΩ
4	—	Series resistor • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz • High range, low gain (RANGE = 1, HGO = 0) • High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	0 100 0 0 0 0	— — — 0 10 20	kΩ
5	T	Crystal start-up time [4] • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1) • High range, low gain (RANGE = 1, HG0 = 0)[5] • High range, high gain (RANGE = 1, HG0 = 1)[5]	$t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	— — — —	200 400 5 15	— — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) • FEE or FBE mode [2] • PEE or PBE mode [3] • BLPE mode	f_{extal}	0.03125 1 0	— — —	5 16 40	MHz MHz MHz

[1] Data in Typical column was characterized at 5.0 V, 25°C or is typical recommended value.

[2] When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

[3] When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

[4] This parameter is characterized and not tested on each device. Proper PC board-layout procedures must be followed to achieve specifications.

[5] 4 MHz crystal

2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	P	DCO output frequency range - untrimmed [2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 – 70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time [3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time [4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
14	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[5]	—	$\%f_{pll}$
15	D	Lock entry frequency tolerance [7]		D_{lock}	±1.49	—	±2.98	%
16	D	Lock exit frequency tolerance [8]		D_{unl}	±4.47	—	±5.97	%
17	D	Lock time — FLL		t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time — PLL		t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency – RANGE = 0		f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[5] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

[6] 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

[7] Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

[8] Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1		Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2		Internal low-power oscillator period	t_{LPO}	700		1300	μs
3		External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100		—	ns
4		Reset low drive	t_{rstdrv}	66 x t_{cyc}		—	ns
5		Active background debug mode latch setup time	t_{MSSU}	500		—	ns
6		Active background debug mode latch hold time	t_{MSH}	100		—	ns
7		IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns
8		KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns
9		Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	— —	11 35 40 75		ns

[1] Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

[2] This is the shortest pulse guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

[3] This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

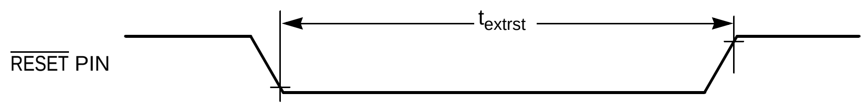


Figure 10. Reset Timing

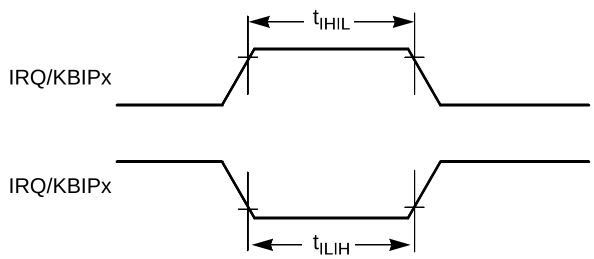


Figure 11. IRQ/KBIPx Timing

2.11.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

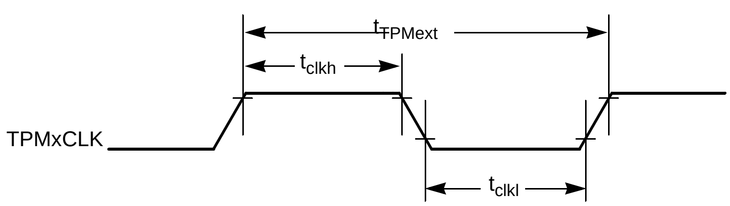


Figure 12. Timer External Clock

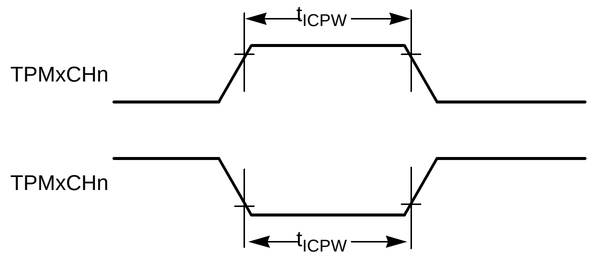


Figure 13. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	D	MSCAN Wake-up dominant pulse pass	t_{WUP}	5		5	µs

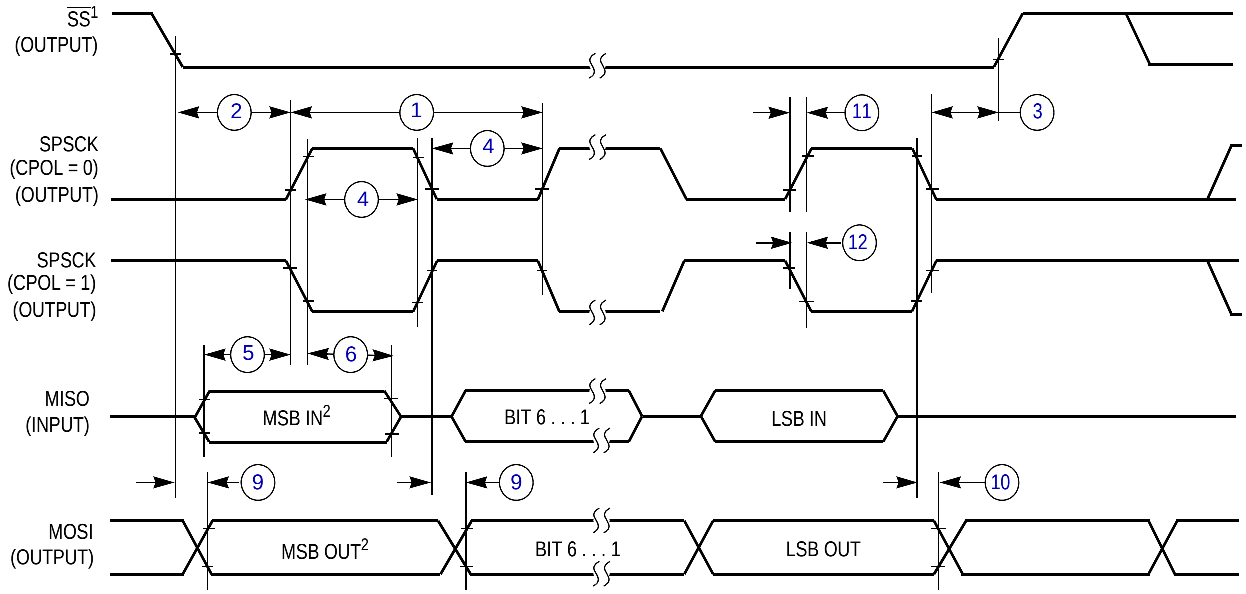
[1] Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2.12 SPI Characteristics

Table 20 and Figure 14 through Figure 17 describe the timing requirements for the SPI system.

Table 20. SPI Timing

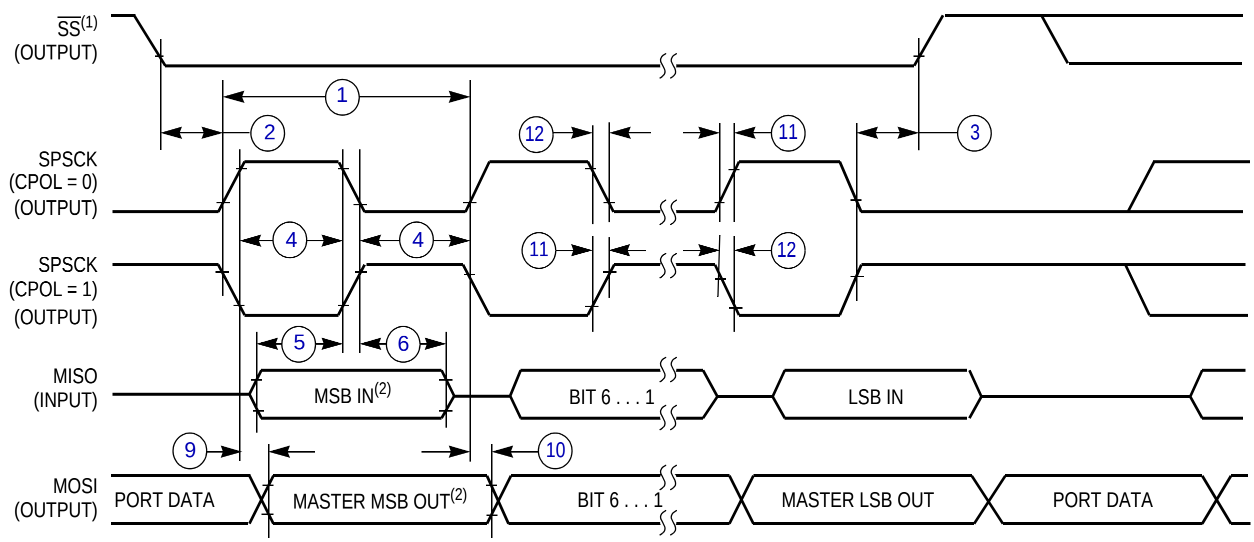
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} – 30$ $t_{cyc} – 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} – 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} – 25$ 25	ns ns



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 1)

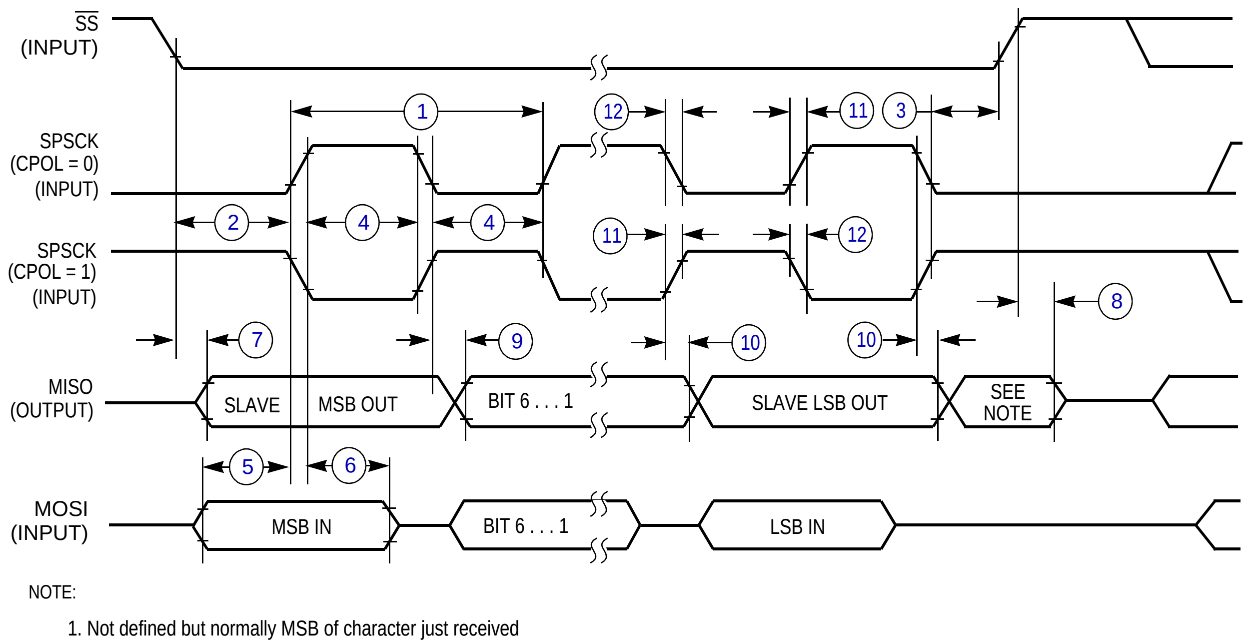


Figure 16. SPI Slave Timing (CPHA = 0)

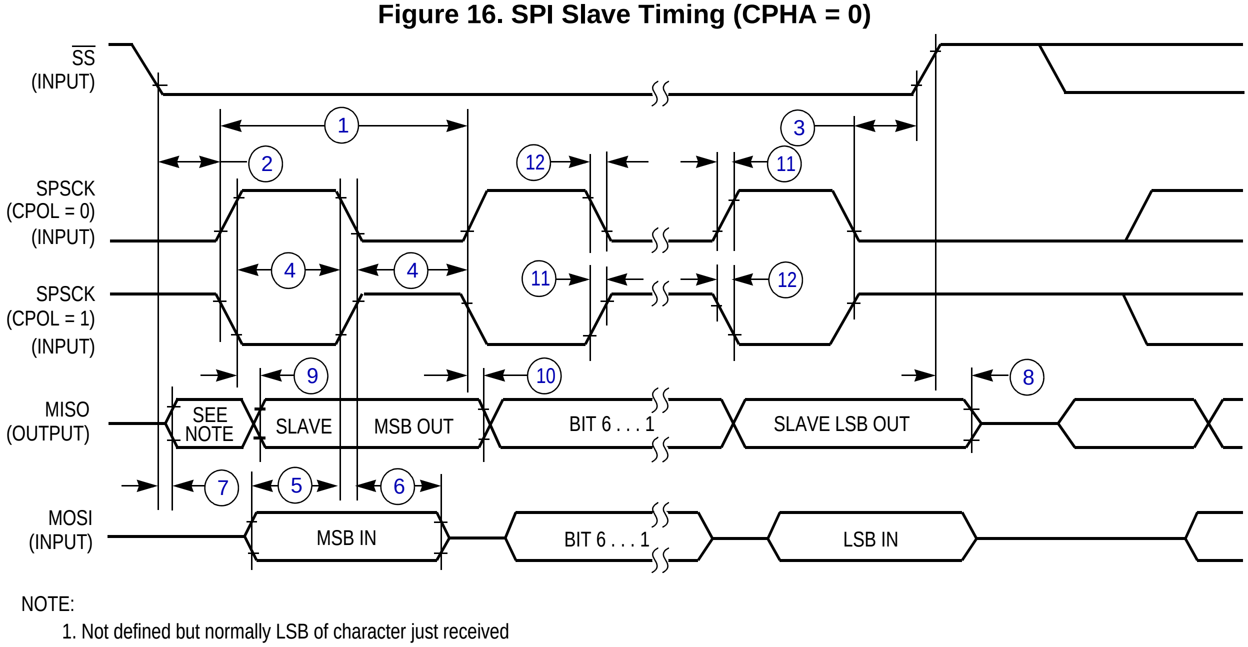


Figure 17. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2		Supply voltage for read operation	V_{Read}	2.7		5.5	V
3		Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4		Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
5		Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6		Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7		Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8		Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles
10		Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 Typical endurance for Flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, Typical Data Retention for Nonvolatile Memory.

2.14 USB Electricals

The USB electricals for the USBOTG module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USBOTG implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

Table 22. Internal USB 3.3V Voltage Regulator Characteristics

	Symbol	Unit	Min	Typ	Max
Regulator operating voltage	V_{regin}	V	3.9	—	5.5
Vreg output	V_{regout}	V	3	3.3	3.6
Vusb33 input with internal Vreg disabled	$V_{usb33in}$	V	3	3.3	3.6
VREG Quiescent Current	I_{VRQ}	mA	—	0.5	—

2.15 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.15.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

3.1 80-pin LQFP

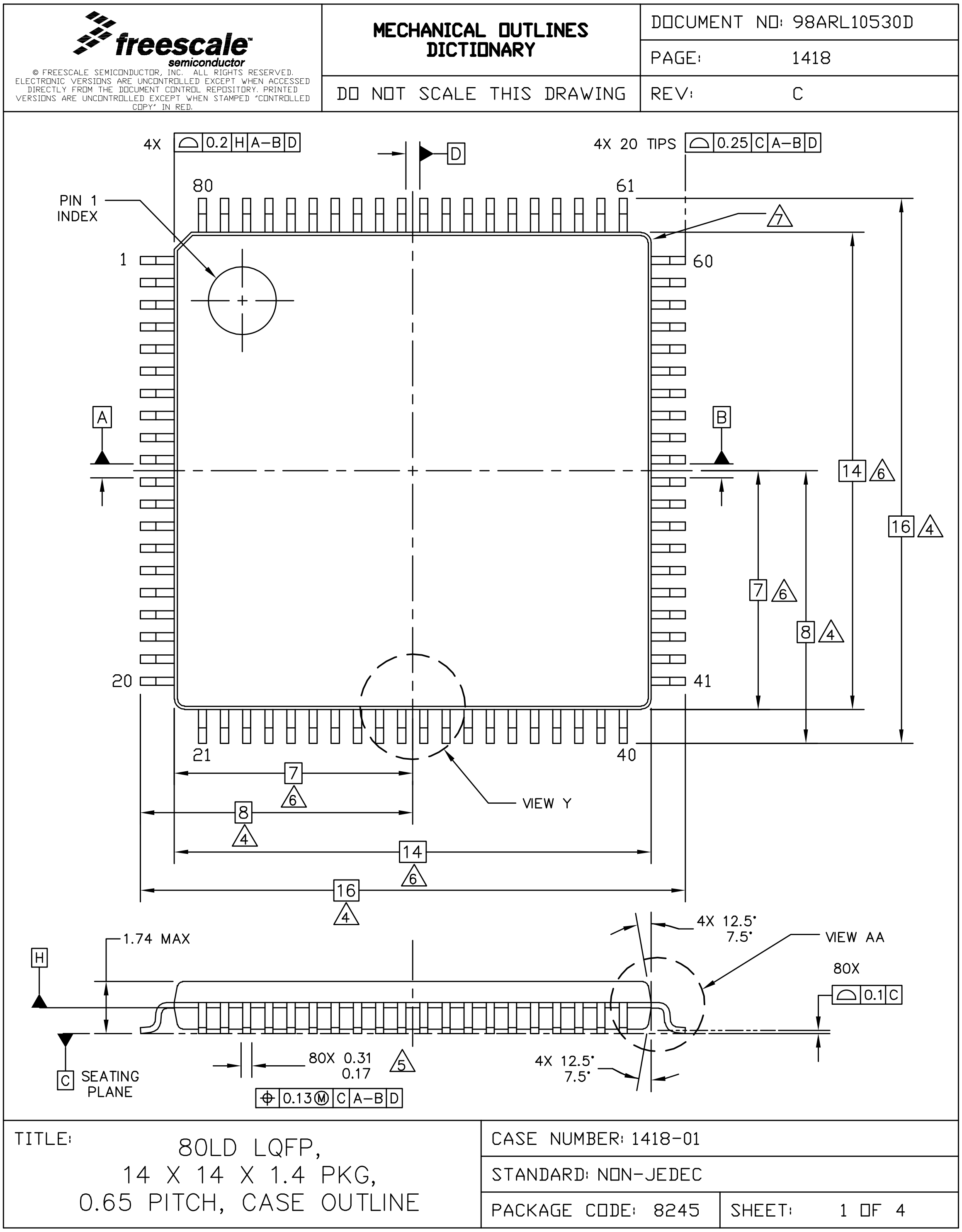


Figure 18. 80-pin LQFP Diagram - I

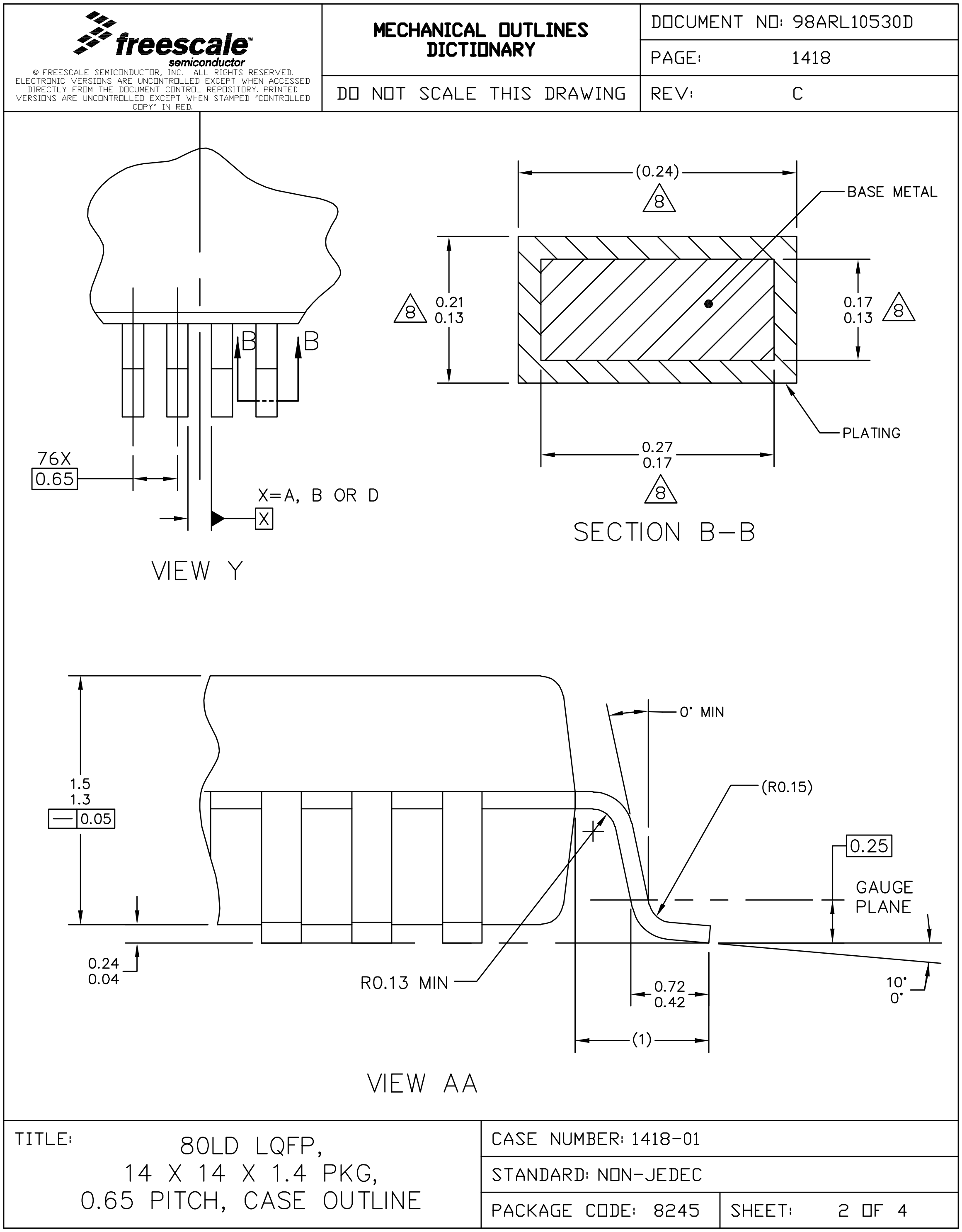


Figure 19. 80-pin LQFP Diagram - II

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARL10530D
		PAGE: 1418
	DO NOT SCALE THIS DRAWING	REV: C

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 80LD LQFP, 14 X 14 X 1.4 PKG, 0.65 PITCH, CASE OUTLINE	CASE NUMBER: 1418−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 8245	SHEET: 3 OF 4

Figure 20. 80-pin LQFP Diagram - III

3.2 64-pin LQFP

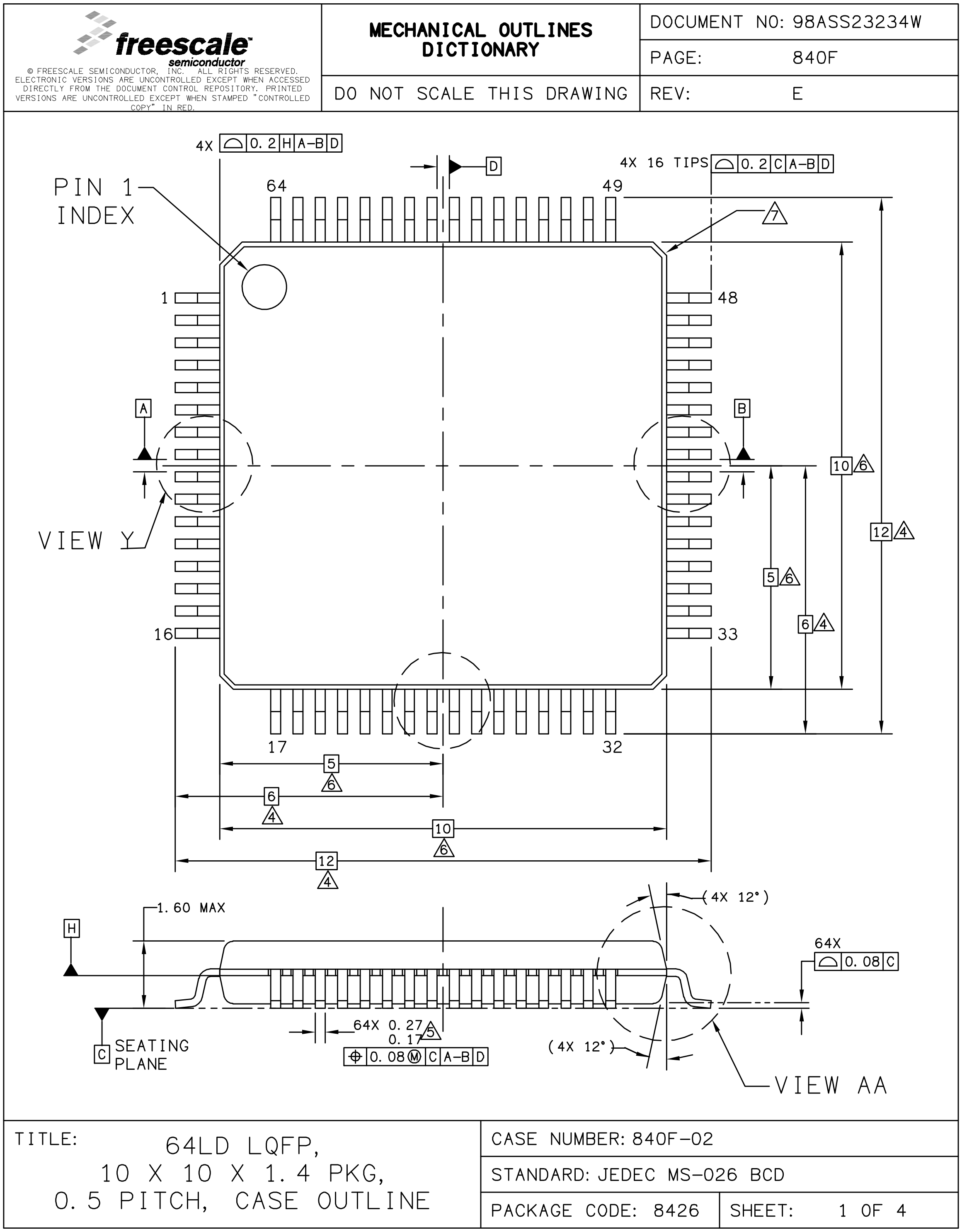


Figure 21. 64-pin LQFP Diagram - I

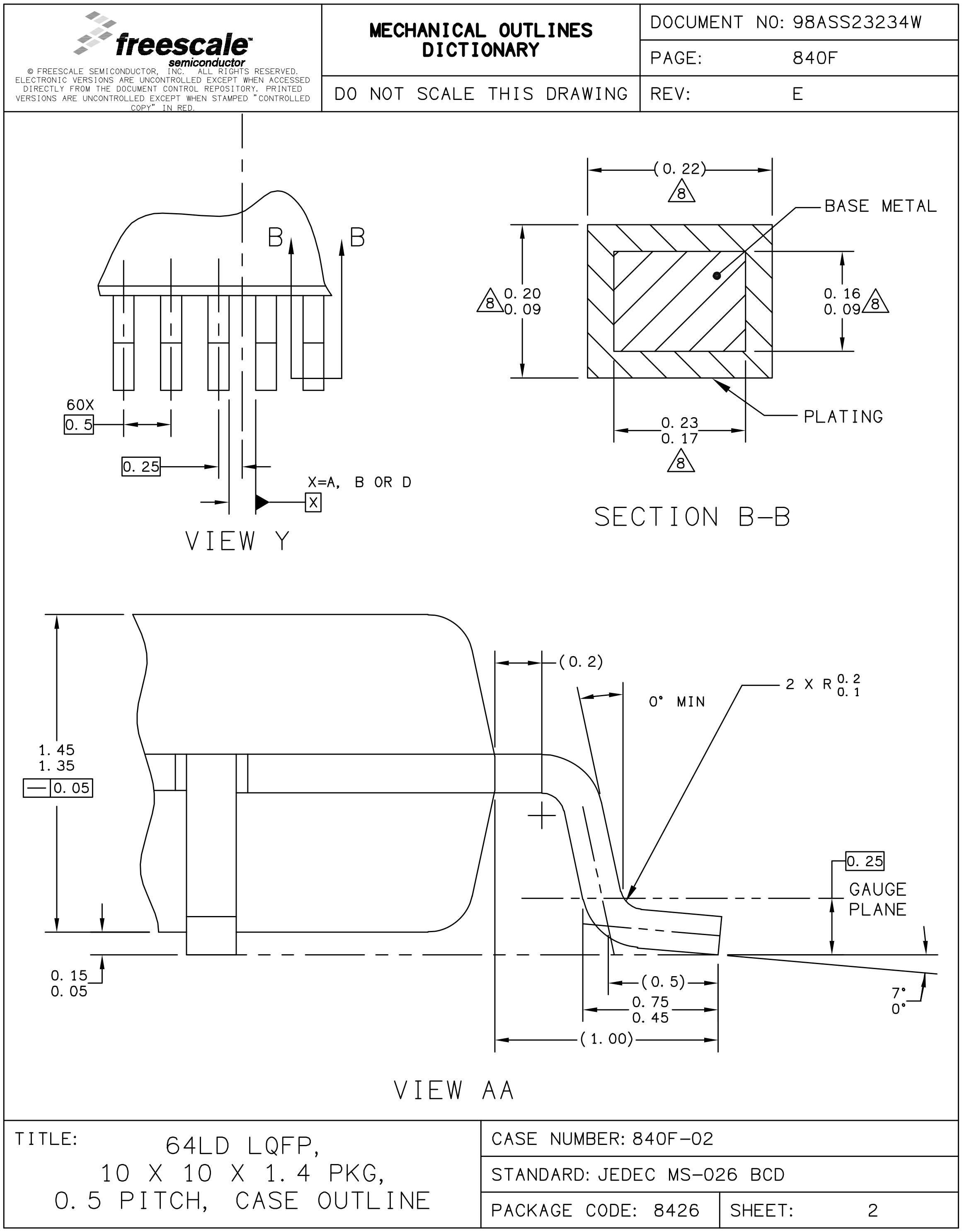


Figure 22. 64-pin LQFP Diagram - II

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		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. (△) DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. (△) THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. (△) THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. (△) EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. (△) THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02	
	STANDARD: JEDEC MS-026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

Figure 23. 64-pin LQFP Diagram - III

3.3 64-pin QFP

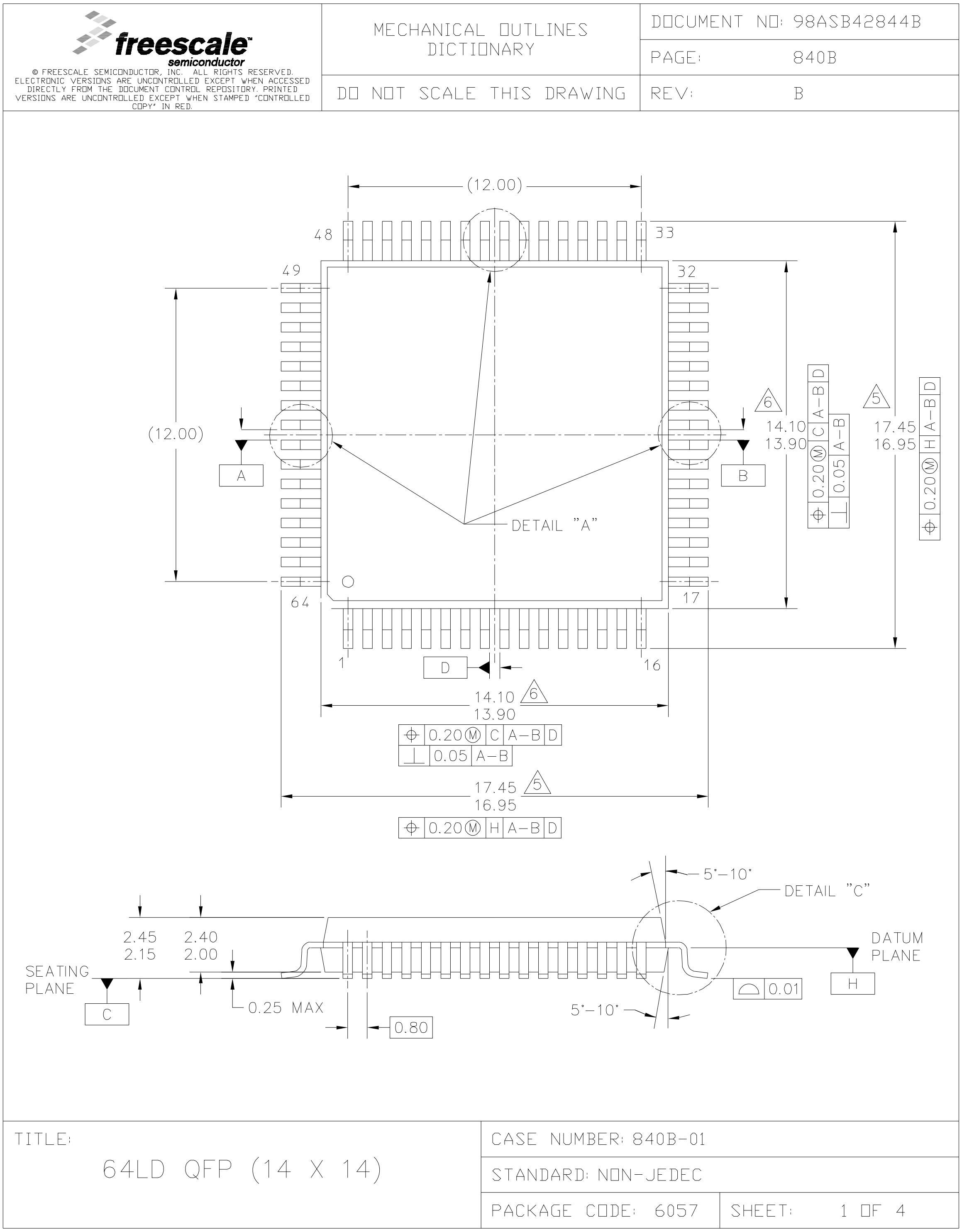

Figure 24. 64-pin QFP Diagram - I

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		PAGE: 840B
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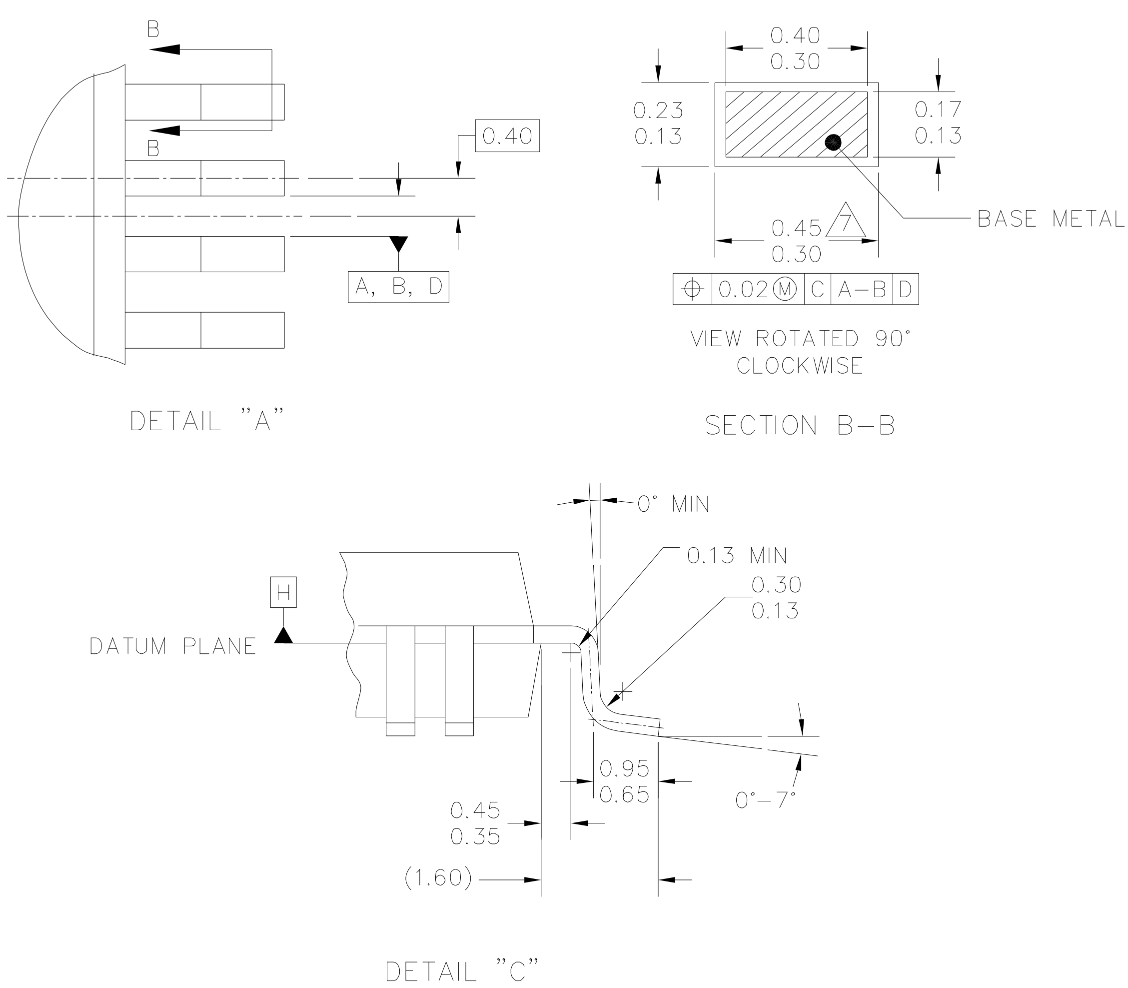

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 2 OF 4

Figure 25. 64-pin QFP Diagram - II

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		PAGE: 840B
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

Figure 26. 64-pin QFP Diagram - III

3.4 44-pin LQFP

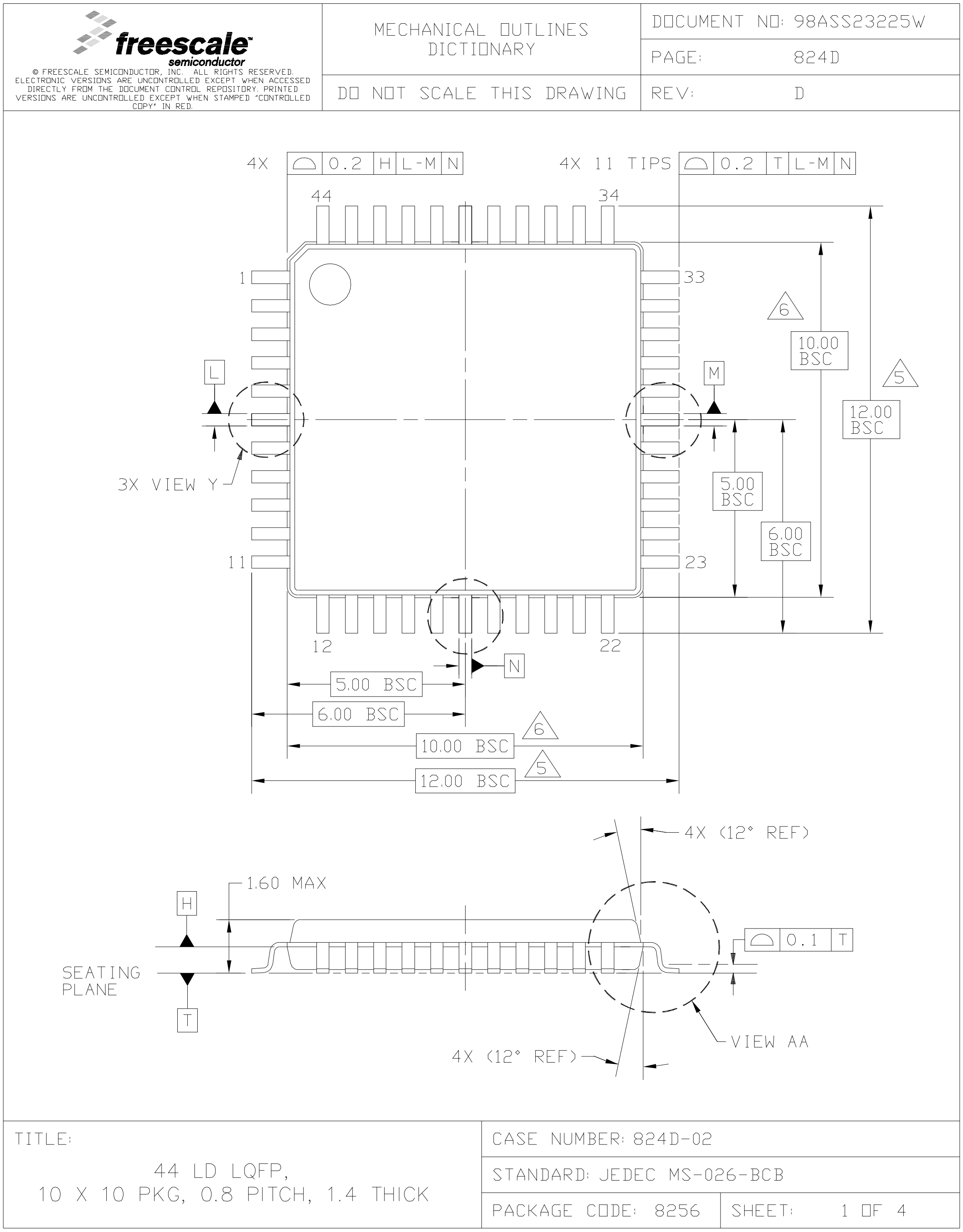

Figure 27. 44-pin LQFP Diagram - I

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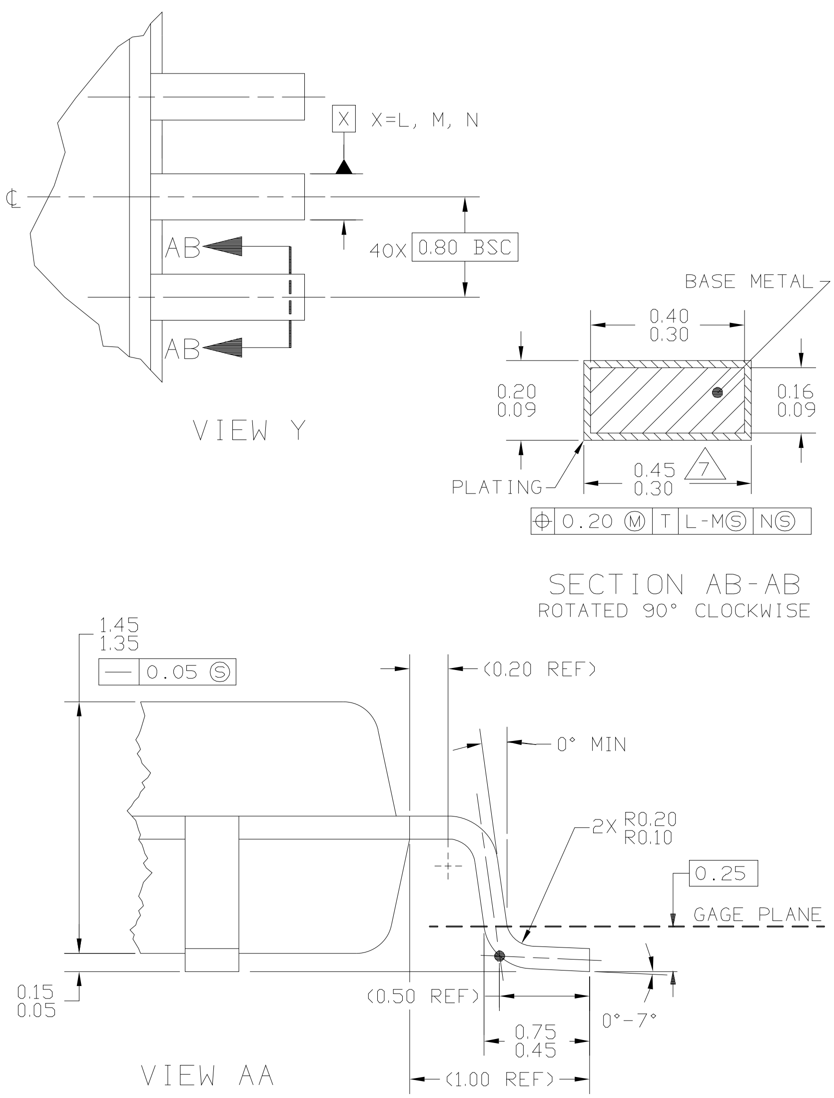
		PAGE: 824D
	DO NOT SCALE THIS DRAWING	REV: D



TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	CASE NUMBER: 824D-02	
	STANDARD: JEDEC MS-026 BCB	
	PACKAGE CODE: 8256	SHEET: 2 OF 4

Figure 28. 44-pin LQFP Diagram - II

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		PAGE: 824D
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NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M−1994.

2. CONTROLLING DIMENSION: MILLIMETER

3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	CASE NUMBER: 824D−02	
	STANDARD: JEDEC MS−026 BCB	
	PACKAGE CODE: 8256	SHEET: 3 OF 4

Figure 29. 44-pin LQFP Diagram - III

4 Revision History

This section lists major changes between versions of the MCF51JM128 Data Sheet document.

Table 23. Changes Between Revisions

Revision	Description
1	Updated features list Updated the figures Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1), Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0), and Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1) Added the figure Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0) Updated the table Supply Current Characteristics Updated the table Oscillator Electrical Specifications (Temperature Range = –40 to 105×C Ambient) Updated the table SPI Electrical Characteristic, DC Characteristics
2	Updated the table Orderable Part Number Summary, DC Characteristics, and Supply Current Characteristics
3	Updated the table Orderable Part Number Summary, MCG Characteristics, SPI Characteristics, and Supply Current Characteristics Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA} Updated the table Device comparison
4	Added “RAM retention voltage” parameter in “DC Characteristics” table, alongwith a table note. Added “Temp sensor voltage” parameter in “5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)” table. Added “ “Temp sensor slope” parameter in 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) table. Also, corrected unit of “Temp sensor voltage” parameter in 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) table.

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