Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{DD} .....-0.3V to +6V
H, W, L (charge pump enabled) .....-0.3V to +5.5V
H, W, L (charge pump disabled)..... -0.3V to the lower of (V_{DD} + 0.3V) or +6V
ADDR0 ..... -0.3V to the lower of (V_{DD} + 0.3V) or +6V
All Other Pins .....-0.3V to +6V
Continuous Current into H, W, and L
MAX5395L.....5mA
MAX5395M.....2mA
MAX5395N 1mA
Maximum Current into Any Input.....50mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 11.9mW/°C above +70°C).....953.5mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range..... -65°C to + 150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+ 300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....83.9°C/W
Junction-to-Ambient Thermal Resistance (θ_{JC}) .....37.0°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 1.7V to 5.5V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESOLUTION							
256-Tap Family	N			256			Tap
DC PERFORMANCE (Voltage-Divider Mode)							
Integral Nonlinearity (Note 3)	INL			-1.0		+1.0	LSB
Differential Nonlinearity	DNL	(Note 3)		-0.5		+0.5	LSB
Ratiometric Resistor Tempco		(DV_W/V_W)/DT, V_H = V_{DD}, V_L = GND, No Load			5		ppm/°C
Full-Scale Error (Code FFh)		Charge pump enabled, 1.7V < V_{DD} < 5.5V		-0.5			LSB
		Charge pump disabled, 2.6V < V_{DD} < 5.5V	MAX5395M MAX5395N	-0.5			
			MAX5395L	-1.0			
Zero-Scale Error (Code 00h)		Charge pump enabled, 1.7V < V_{DD} < 5.5V				+0.5	LSB
		Charge pump disabled, 2.6V < V_{DD} < 5.5V	MAX5395M MAX5395N			+0.5	
			MAX5395L			+1.0	
DC PERFORMANCE (Variable Resistor Mode)							
Integral Nonlinearity (Note 4)	R-INL	Charge pump enabled, 1.7V < V_{DD} < 5.5V		-1.0		+1.0	LSB
		Charge pump disabled, 2.6V < V_{DD} < 5.5V	MAX5395M MAX5395N	-1.0		+1.0	
			MAX5395L	-1.5		+1.5	
Differential Nonlinearity	R-DNL	(Note 4)		-0.5		+0.5	LSB
Wiper Resistance (Note 5)	R_{WL}	Charge pump enabled, 1.7V < V_{DD} < 5.5V			25	50	Ω
		Charge pump disabled, 2.6V < V_{DD} < 5.5V				200	

Electrical Characteristics (continued)

(V_{DD} = 1.7V to 5.5V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE (Resistor Characteristics)							
Terminal Capacitance	C_H, C_L	Measured to GND			10		pF
Wiper Capacitance	C_W	Measured to GND			20		pF
End-to-End Resistor Tempco	T_{CR}	No load			50		ppm/°C
End-to-End Resistor Tolerance		Wiper not connected		-25		+25	%
AC PERFORMANCE							
-3dB Bandwidth	BW	Code = 80h, 10pF load, V_{DD} = 1.8V	10kΩ		1600		kHz
			50kΩ		340		
			100kΩ		165		
Total Harmonic Distortion Plus Noise	THD+N	(Note 6)			0.035		%
Wiper Settling Time	t_S	(Note 7)	10kΩ		190		ns
			50kΩ		400		
			100kΩ		664		
Charge-Pump Feedthrough at W	V_{RW}				600		nV_{RMS}
POWER SUPPLIES							
Supply Voltage Range	V_{DD}			1.7		5.5	V
Terminal Voltage Range (H, W, L to GND)		Charge pump enabled, 1.7V < V_{DD} < 5.5V		0		5.25	V
		Charge pump disabled, 2.6V < V_{DD} < 5.5V		0		V_{DD}	
Supply Current (Note 8)	I_{VDD}	Charge pump disabled, 1.7V			0.3	1.4	µA
		Charge pump disabled, 2.5V			0.4	1.7	
		Charge pump disabled, 5.5V			1.0	4.0	
		Charge pump enabled, 1.7V < V_{DD} < 5.5V	V_{DD} = 5.5V		25	50	
			V_{DD} = 1.7V		20	45	
DIGITAL INPUTS							
Minimum Input High Voltage	V_{IH}	2.6V < V_{DD} < 5.5V		70			% x V_{DD}
		1.7V < V_{DD} < 2.6V		80			
Maximum Input Low Voltage	V_{IL}	2.6V < V_{DD} < 5.5V				30	% x V_{DD}
		1.7V < V_{DD} < 2.6V				20	
Input Leakage Current				-1		+1	µA
Input Capacitance					5		pF
ADDR0 Pullup/Pulldown Strength	$R_{PUR}R_{PD}$	(Note 9)			60		kΩ
TIMING CHARACTERISTICS (Note 10)							
Maximum SCL Frequency	f_{SCL}					400	kHz
Setup Time for START Condition	$t_{SU:STA}$			0.6			µs

Electrical Characteristics (continued)

(V_{DD} = 1.7V to 5.5V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time for START Condition	$t_{HD:STA}$		0.6			µs
SCL High Time	t_{HIGH}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0			µs
SDA, SCL Rise Time	t_R				0.3	µs
SDA, SCL Fall Time	t_F				0.3	µs
Setup Time for STOP Conditions	$t_{SU:STO}$		0.6			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Pulse-Suppressed Spike Width	t_{SP}			50		ns
Capacitive Load for Each Bus	C_B			400		pF

Note 2: All devices are production tested at T_A = +25°C and are guaranteed by design and characterization for T_A = -40°C to +125°C.

Note 3: DNL and INL are measured with the potentiometer configured as a voltage-divider with V_H = 5.25V (QP enabled) or V_{DD} (QP disabled) and V_L = GND. The wiper terminal is unloaded and measured with an ideal voltmeter.

Note 4: R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). H is unconnected and L = GND.
For charge pump enabled, V_{DD} = 1.7V to 5.5V, the wiper terminal is driven with a source current of 400µA for the 10kΩ configuration, 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration.
For charge pump disabled and V_{DD} = 5.5V, the wiper terminal is driven with a source current of 400µA for the 10kΩ configuration, 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration.
For charge pump disabled and V_{DD} = 2.6V, the wiper terminal is driven with a source current of 200µA for the 10kΩ configuration, 40µA for the 50kΩ configuration, and 20µA for the 100kΩ configuration.

Note 5: The wiper resistance is the maximum value measured by injecting the currents given in Note 4 into W with L = GND. $R_W = (V_W - V_H)/I_W$.

Note 6: Measured at W with H driven with a 1kHz, 0V to V_{DD} amplitude tone and V_L = GND. Wiper at midscale with a 10pF load.

Note 7: Wiper-settling time is the worst-case 0-to-50% rise time, measured between tap 0 and tap 127. H = V_{DD}, L = GND, and the wiper terminal is loaded with 10pF capacitance to ground.

Note 8: Digital Inputs at V_{DD} or GND.

Note 9: An unconnected condition on the ADDR0 pin is sensed via a pullup and pulldown operation. For proper operation, the ADDR0 pin should be tied to V_{DD}, GND, or left unconnected with minimal capacitance.

Note 10: Digital timing is guaranteed by design and characterization, and is not production tested.

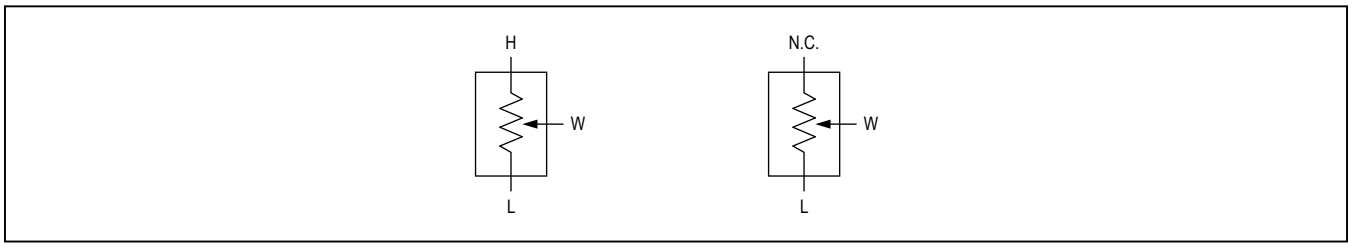
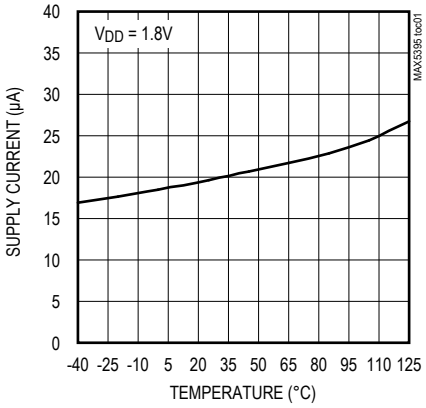


Figure 1. Voltage-Divider and Variable Resistor Configurations

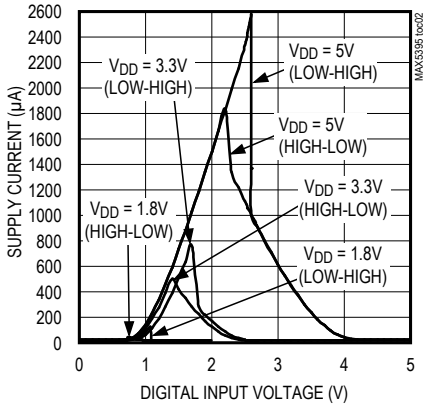
Typical Operating Characteristics

(V_{DD} = 1.8V, T_A = +25°C, unless otherwise noted.)

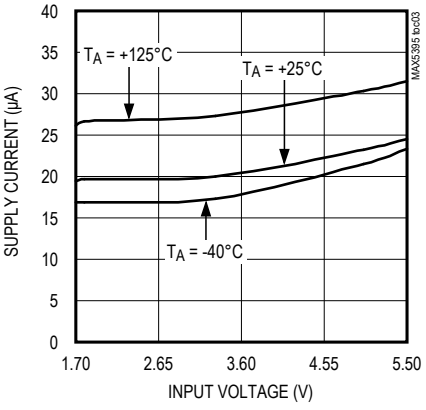
SUPPLY CURRENT vs. TEMPERATURE



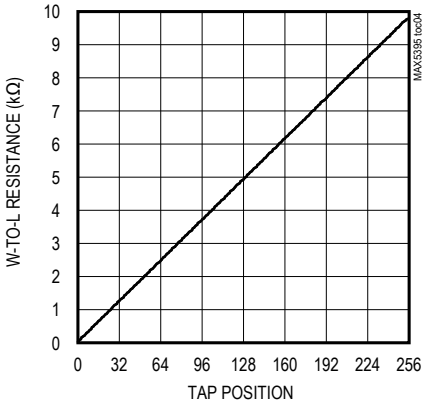
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



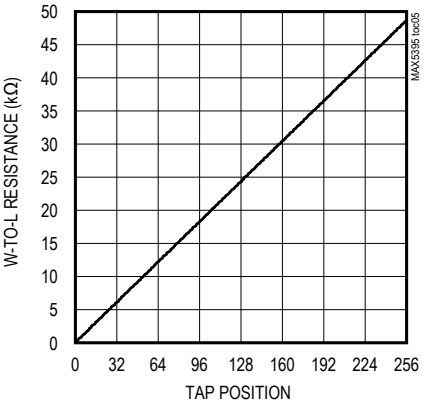
SUPPLY CURRENT vs. INPUT VOLTAGE



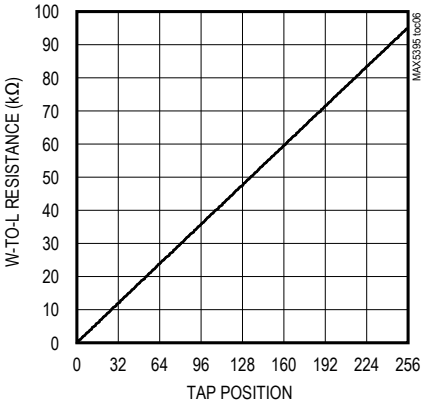
RESISTANCE (W-TO-L) vs. TAP POSITION (10kΩ)



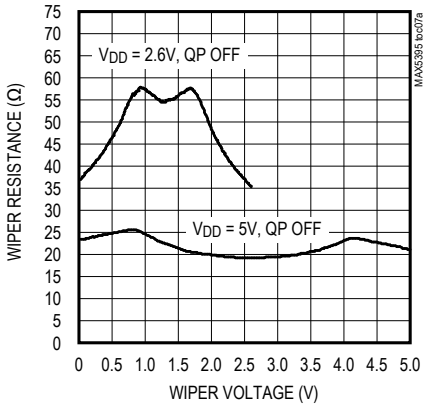
RESISTANCE (W-TO-L) vs. TAP POSITION (50kΩ)



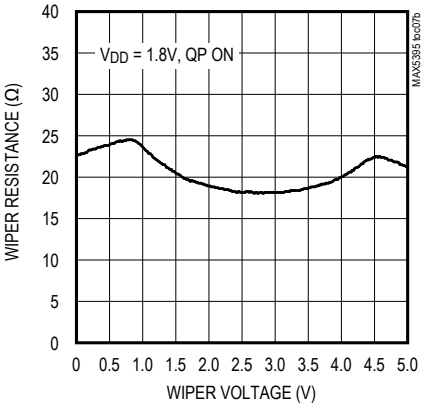
RESISTANCE (W-TO-L) vs. TAP POSITION (100kΩ)



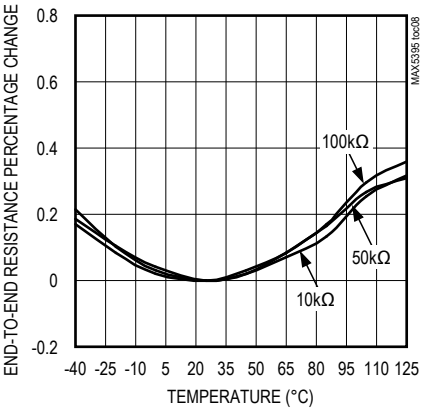
WIPER RESISTANCE vs. WIPER VOLTAGE



WIPER RESISTANCE vs. WIPER VOLTAGE



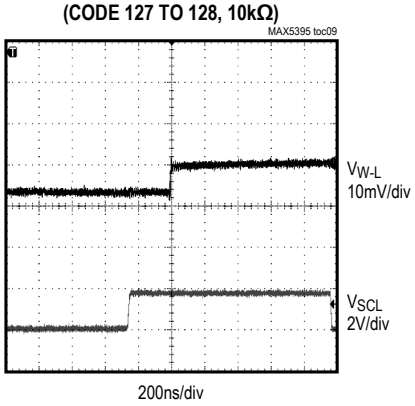
END-TO-END RESISTANCE PERCENTAGE CHANGE vs. TEMPERATURE



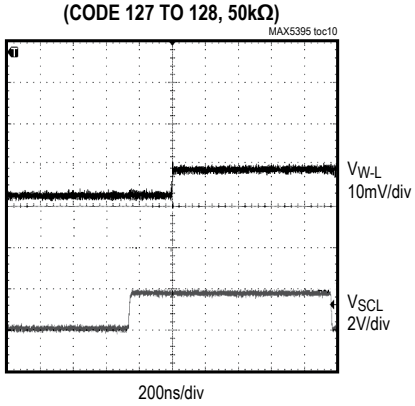
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, T_A = +25°C, unless otherwise noted.)

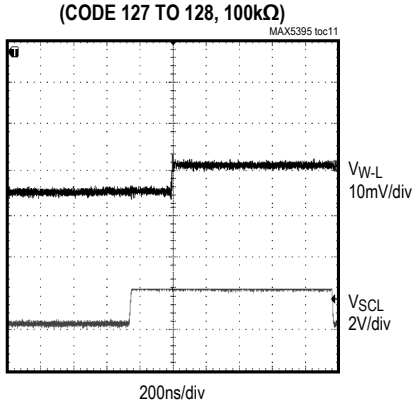
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128, 10kΩ)



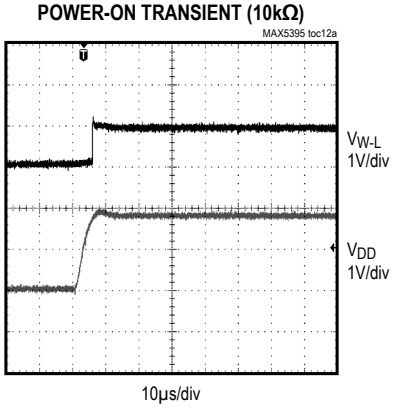
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128, 50kΩ)



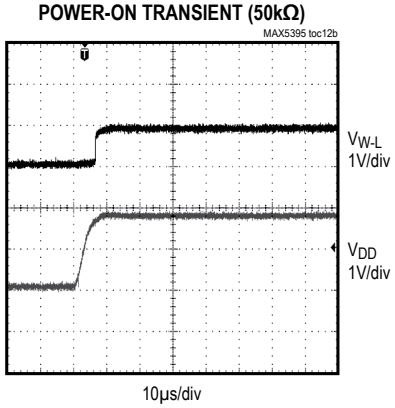
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128, 100kΩ)



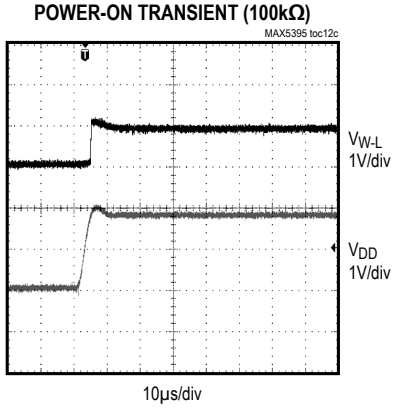
POWER-ON TRANSIENT (10kΩ)



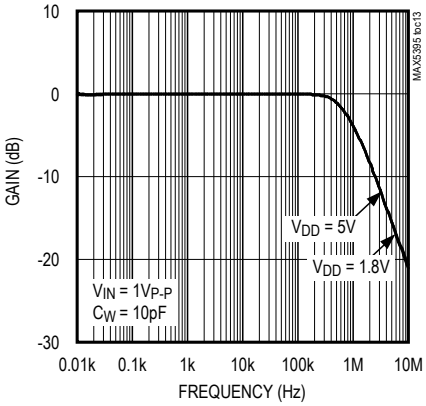
POWER-ON TRANSIENT (50kΩ)



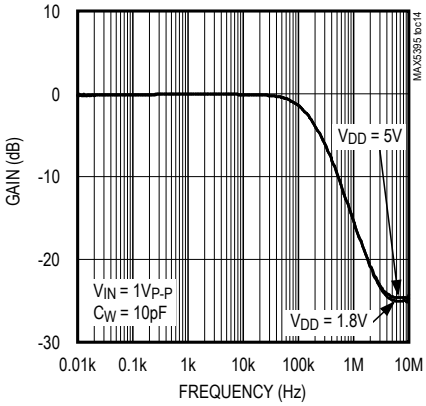
POWER-ON TRANSIENT (100kΩ)



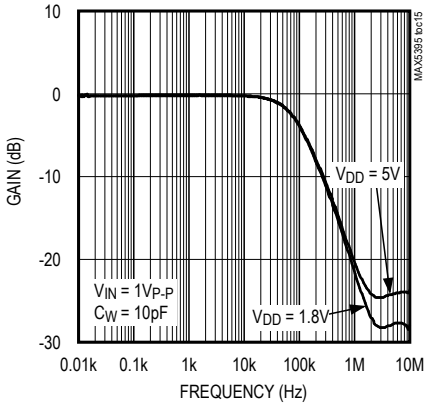
MIDSCALE FREQUENCY RESPONSE (10kΩ)



MIDSCALE FREQUENCY RESPONSE (50kΩ)



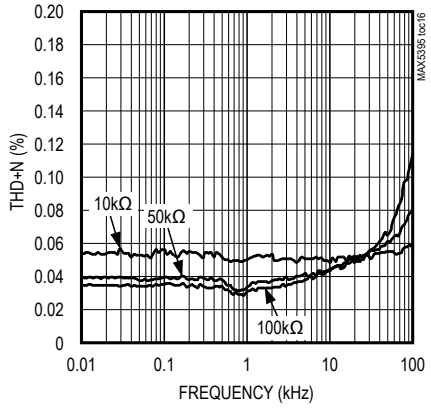
MIDSCALE FREQUENCY RESPONSE (100kΩ)



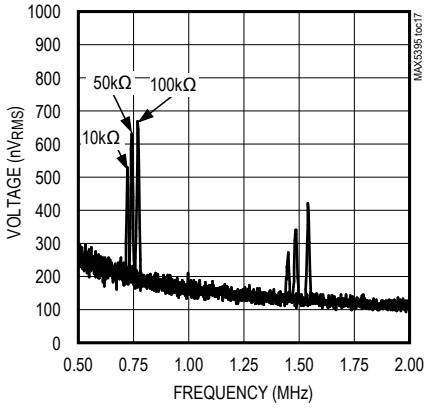
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, T_A = +25°C, unless otherwise noted.)

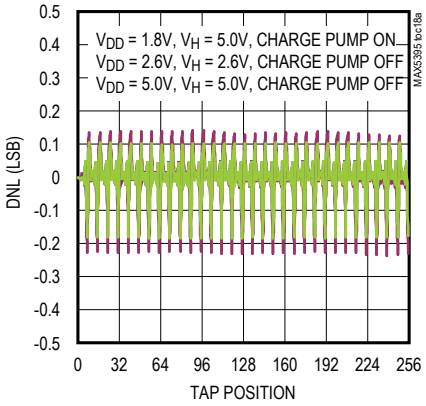
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



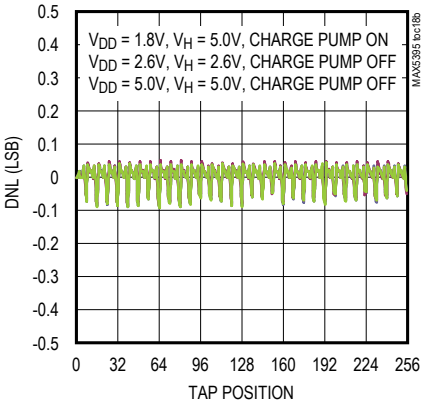
CHARGE-PUMP FEEDTHROUGH AT W



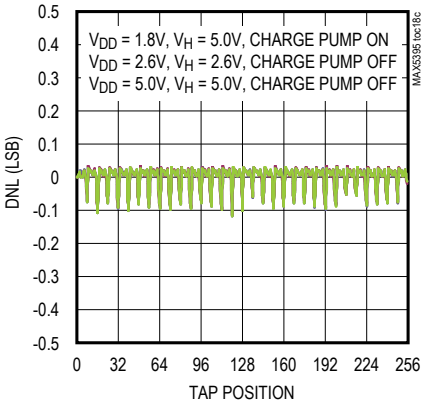
VARIABLE-RESISTOR DNL vs. TAP POSITION (10kΩ)



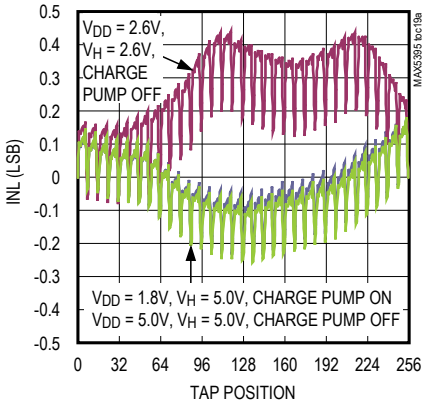
VARIABLE-RESISTOR DNL vs. TAP POSITION (50kΩ)



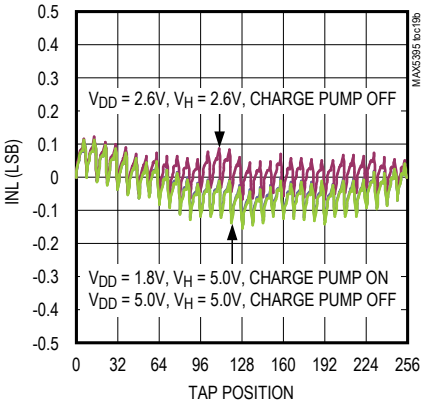
VARIABLE-RESISTOR DNL vs. TAP POSITION (100kΩ)



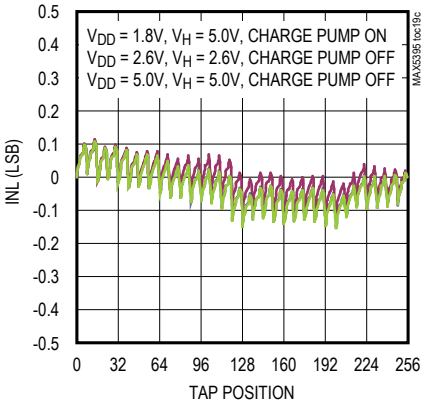
VARIABLE-RESISTOR INL vs. TAP POSITION (10kΩ)



VARIABLE-RESISTOR INL vs. TAP POSITION (50kΩ)



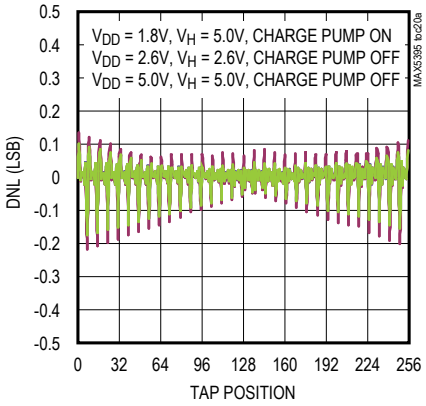
VARIABLE-RESISTOR INL vs. TAP POSITION (100kΩ)



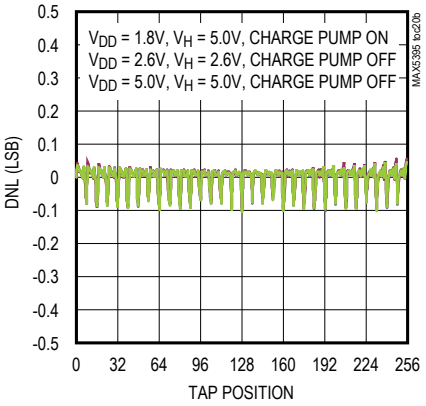
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, T_A = +25°C, unless otherwise noted.)

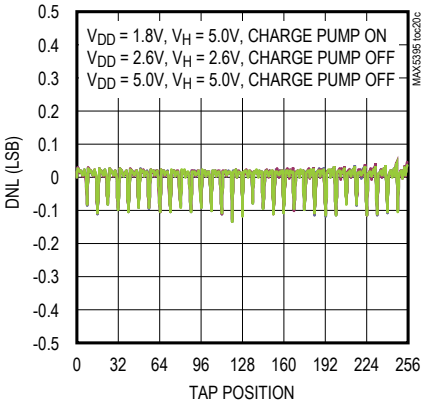
VOLTAGE-DIVIDER DNL vs. TAP POSITION (10kΩ)



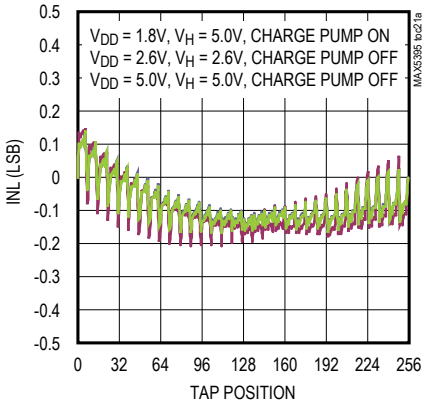
VOLTAGE-DIVIDER DNL vs. TAP POSITION (50kΩ)



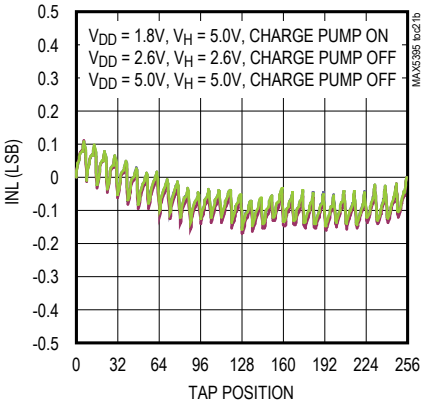
VOLTAGE-DIVIDER DNL vs. TAP POSITION (100kΩ)



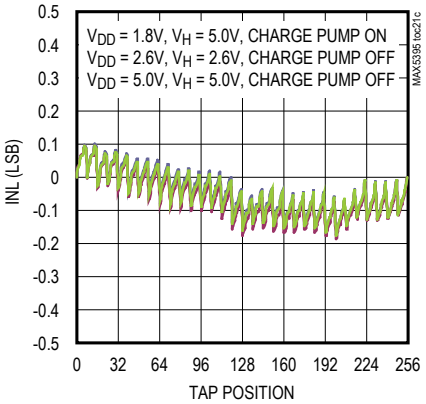
VOLTAGE-DIVIDER INL vs. TAP POSITION (10kΩ)



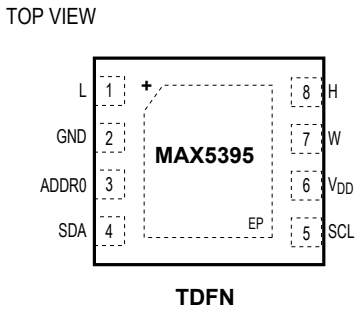
VOLTAGE-DIVIDER INL vs. TAP POSITION (50kΩ)



VOLTAGE-DIVIDER INL vs. TAP POSITION (100kΩ)



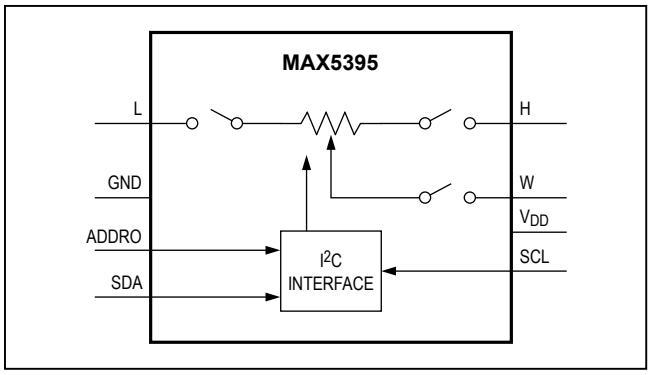
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	L	Low Terminal. The voltage at L can be greater than or less than the voltage at H. Current can flow into or out of L.
2	GND	Ground
3	ADDR0	Address Input 0. Connected to V_{DD}, GND, or open.
4	SDA	I2C Serial Data Input
5	SCL	I2C Clock Input
6	V_{DD}	Power Supply
7	W	Wiper Terminal
8	H	High Terminal. The voltage at H can be greater than or less than the voltage at L. Current can flow into or out of H.
—	EP	Exposed Pad. Internally connected to GND. Connect to ground.

Functional Diagram



Detailed Description

The MAX5395 single, 256-tap volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. Potentiometer terminals are independent of supply for voltages up to +5.25V with single-supply operation from 1.7V to 5.5V (charge pump enabled). User-controlled shutdown modes allow the H, W, or L terminals to be opened with the wiper position set to zero-code, midcode, full-code, or the value contained in the wiper register. Ultra-low-quiescent supply current (< 1µA) can be achieved for supply voltages between 2.6V and 5.5V by disabling the internal charge pump and not allowing potentiometer terminals to exceed the supply voltage by more than 0.3V. The MAX5395 provides a low 50ppm/°C end-to-end temperature coefficient and features a I²C serial interface.

The small package size, low supply operating voltage, low supply current, and automotive temperature range of the MAX5395 make the device uniquely suited for the portable consumer market and battery-backup industrial applications.

Charge Pump

The MAX5395 contains an internal charge pump that guarantees the maximum wiper resistance, R_{WL}, to be less than 50Ω (25Ω typ) for supply voltages down to 1.7V and allows pins H, W, and L to be driven between GND and 5.25V independent of V_{DD}. Minimal charge-pump feedthrough is present at the terminal outputs and is illustrated by the Charge-Pump Feedthrough at W vs. Frequency graph in the *Typical Operating Characteristics*. The charge pump is on by default but can be disabled with QP_OFF and enabled with the QP_ON commands (Table 1). The MAX5395 minimum supply voltage with charge pump disabled is limited to 2.6V and terminal voltage cannot exceed -0.3V to (V_{DD} + 0.3V).

I²C Interface

The MAX5395 feature an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL enable communication between the MAX5395 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX5395 by transmitting the proper slave address followed by the command byte and then the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX5395 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX5395 must transmit the proper slave address followed by a series of nine SCL pulses for each byte of data requested. The MAX5395 transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or Repeated START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output.

Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX5395 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals. The MAX5395 can accommodate bus voltages higher than V_{DD} up to a limit of +5.5V. Bus voltages lower than V_{DD} are not recommended and may result in significantly increased interface currents and data corruption.

The MAX5395 with I²C interface contains a shift register that decodes the command and address bytes, routing the data to the register. Data written to a memory register immediately updates the wiper position. The wiper powers up in mid position, D[7:0] = 0x80 with charge pump enabled.

I2C START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX5395. The master terminates transmission and frees the bus, by issuing a STOP condition. The bus remains active if a Repeated START condition is generated instead of a STOP condition.

I2C Early STOP and Repeated START Conditions

The MAX5395 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition. Transmissions ending in an early STOP condition will not impact the internal device settings. If the STOP occurs during a readback byte, the transmission is terminated and a later read mode request will begin transfer of the requested register data from the beginning. See Figure 3.

It is possible to interrupt a transmission to a MAX5395 with a new START (Repeated START) condition (perhaps addressing another device), which leaves the input registers with data that has not been transferred to the internal registers. The unused data will not be stored under these conditions. The aborted MAX5395 I2C sequence will have no effect on the part.

I2C Acknowledge

In write mode, the acknowledge bit (ACK) is a clocked 9th bit that the MAX5395 uses to handshake receipt of each byte of data as shown in Figure 4. The MAX5395 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication.

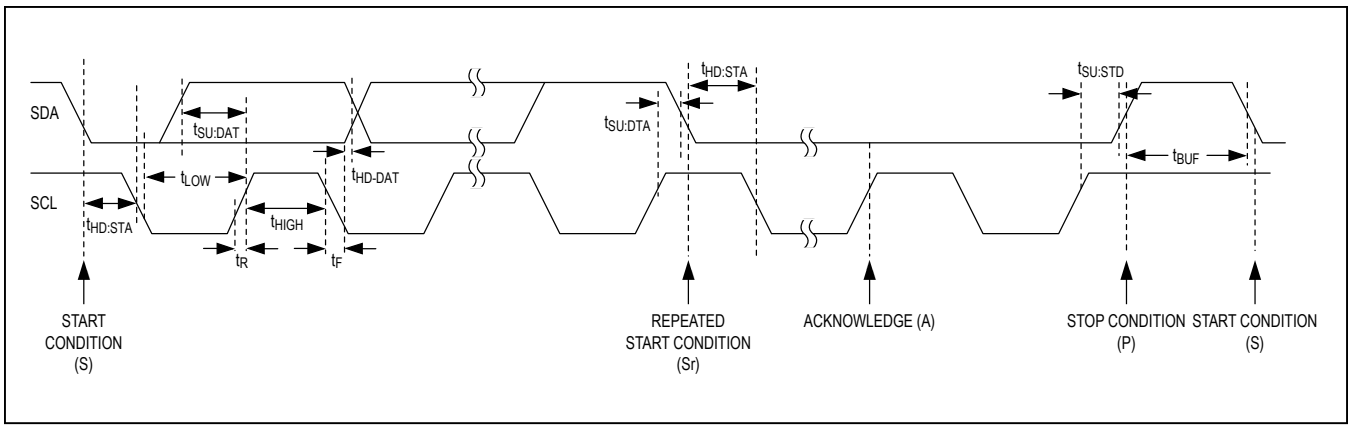


Figure 2. I2C Timing Diagram

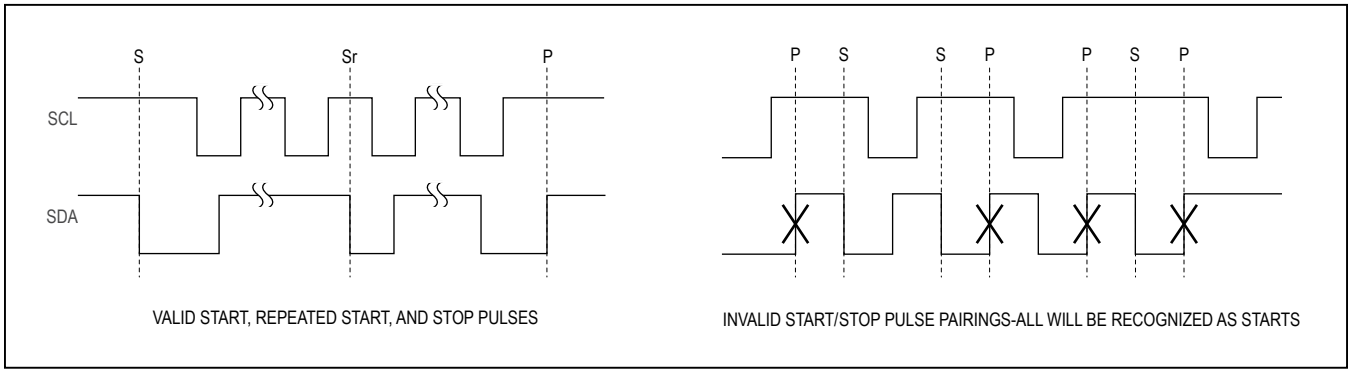


Figure 3. I2C START(s), Repeated START(S), and STOP(S) Conditions

In read mode, the master pulls down SDA during the 9th clock cycle to acknowledge receipt of data from the MAX5395. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX5395, followed by a STOP condition.

I2C Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the R/$\overline{W}$ bit. See Figure 5 and Figure 6. The five most significant bits are 01010 with the 3 LSBs determined ADDR0 as shown in Table 1. Setting the R/$\overline{W}$ bit to 1 configures the MAX5395 for read mode. Setting the R/$\overline{W}$ bit to 0 configures the MAX5395 for write mode. The slave address is the first byte of information sent to the MAX5395 after the START condition.

The MAX5395 has the ability to detect an unconnected (N.C.) state on the ADDR0 input for additional address flexibility; if disconnecting the ADDR0 input, be certain to minimize all loading on the ADDR0 input (i.e. provide a landing for ADDR0, but do not allow any board traces).

I2C Message Format for Writing

A master device communicates with the MAX5395 by transmitting the proper slave address followed by command and data word. Each transmit sequence is framed by a START or Repeated START condition and a STOP condition as described above. Each word is 8 bits long and is always followed by an acknowledge clock (ACK) pulse as shown in Figure 5. The first byte contains the address of the MAX5395 with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the command to be executed and the third byte contains the data to be written.

Table 1. I2C Slave Address LSBs

ADDR0	A1	A0	SLAVE ADDRESS
GND	0	0	0101000
N.C.	0	1	0101001
V_{DD}	1	1	0101011

I2C Message Format for Readback Operations

Each readback sequence is framed by a START or Repeated START condition and a STOP condition. Each word is 8 bits long and is followed by an acknowledge clock pulse as shown in Figure 6. The first byte contains the address of the MAX5395 with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the register that is to be read back. There is a Repeated START condition, followed by the device address with R/$\overline{W}$ = 1 to indicate a

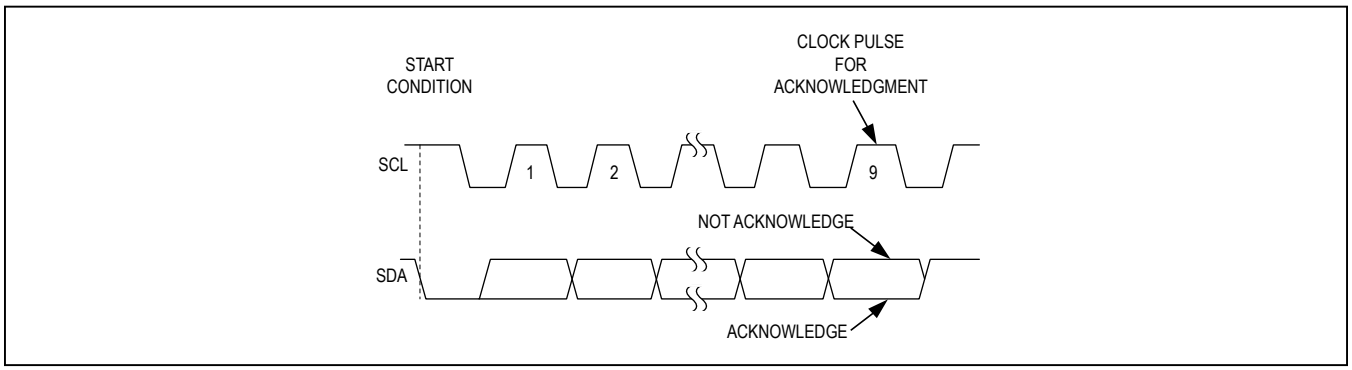


Figure 4. I2C Acknowledge

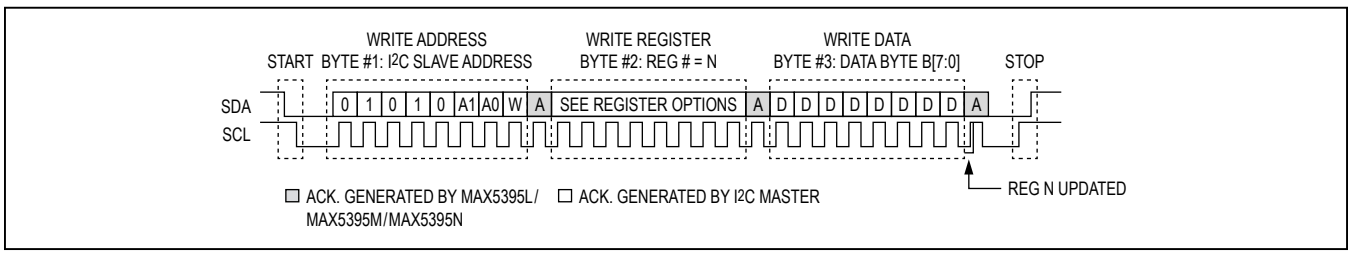


Figure 5. I2C Complete Write Serial Transmission

read and an acknowledge clock. The master has control of the SCL line but the MAX5395 takes over the SDA line. The final byte in the frame contains the register data readback followed by a STOP condition. If additional bytes beyond those required to read back the requested data are provided, the MAX5395 will continue to read back ones.

The wiper register and the configuration register are the only two registers that support readback (Table 2). Readback of all other registers is not supported and results in the readback of ones.

D[7:0]: Wiper position

QP: Charge pump status, 1 is enabled, 0 is disabled.

HSW: H terminal switch status, 0 is closed, 1 is open

WSW: W terminal switch status, 0 is closed, 1 is open

LSW: L terminal switch status, 0 is closed, 1 is open

TSEL[1:0]: Tap select, 00- wiper is at contents of wiper register, 01 – wiper is at 0x00, 10 – wiper is at 0x80, 11 – wiper is at 0xFF.

General Call Support

The MAX5395 supports software reset through general call address 0x00 followed by R/$\overline{W}$ = 0, followed by 0x06 data. A software reset of the MAX5395 will return the part to the power-on default conditions. The MAX5395 will ACK the general call address and any command byte following, but will not support any general call features other than software reset.

Table 2. I2C READ Command Byte Summary

REGISTER	COMMAND BYTE								DATA BYTE							
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
WIPER	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
CONFIG	1	0	0	0	0	0	0	0	QP	0	0	HSW	LSW	WSW	TSEL[1:0]	

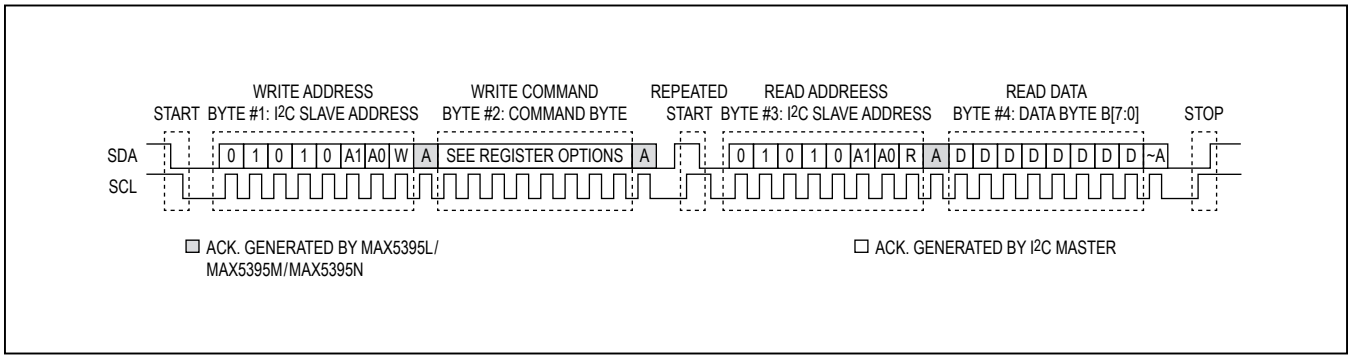


Figure 6. Standard I2C Register Read Sequence

Table 3. I2C Write Command Byte Summary

COMMAND		ADDRESS BYTE									COMMAND BYTE									DATA BYTE									
		A6	A5	A4	A3	A2	A1	A0	R/W		C7	C6	C5	C4	C3	C2	C1	C0		D7	D6	D5	D4	D3	D2	D1	D0		
WIPER									0		0	0	0	0	0	0	0	0		D7	D6	D5	D4	D3	D2	D1	D0		
SD_CLR									0		1	0	0	0	0	0	0	0											
SD_H_WREG									0		1	0	0	1	0	0	0	0											
SD_H_ZERO									0		1	0	0	1	0	0	0	1											
SD_H_MID									0		1	0	0	1	0	0	1	0											
SD_H_FULL									0		1	0	0	1	0	0	1	1											
SD_L_WREG	S								0	A	1	0	0	0	1	0	0	0	A									A	P
SD_L_ZERO									0		1	0	0	0	1	0	0	1											
SD_L_MID									0		1	0	0	0	1	0	1	0											
SD_L_FULL									0		1	0	0	0	1	0	1	1											
SD_W									0		1	0	0	0	0	1	X	X											
QP_OFF									0		1	0	1	0	0	0	0	0											
QP_ON									0		1	0	1	0	0	0	0	1											
RST									0		1	1	0	0	0	0	0	0											

See Table 1

Don't Care

WIPER Command

The data byte writes to the wiper register and the potentiometer moves to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 0x00 moves the wiper to the position closest to L. D[7:0] = 0xFF moves the wiper closest to H. D[7:0] = 0x80 following power-on.

SD_CLR Command

Removes any existing shutdown condition. Connects all potentiometer terminals and returns the wiper to the value stored in the wiper register. The command does not affect the current status of the charge pump.

SD_H_WREG Command

Opens the H terminal and maintains the wiper at the wiper register location. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will close the H terminal and allow the wiper register to be written. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_H_ZERO Command

Moves wiper to zero-scale position (0x00) and opens the H terminal. The wiper register remains unaltered. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close the H terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_H_MID Command

Moves wiper to midscale position (0x80) and opens the H terminal. The wiper register remains unaltered. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close the H terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_H_FULL Command

Moves wiper to full-scale position (0xFF) and opens the H terminal. The wiper register remains unaltered. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close the H terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_L_WREG Command

Opens the L terminal and maintains the wiper at the wiper register location. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will close the L terminal and allow wiper register to be written. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_L_ZERO Command

Moves wiper to zero-scale position (0x00) and opens the L terminal. The wiper register remains unaltered. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close the L terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_L_MID Command

Moves wiper to midscale position (0x80) and opens the L terminal. The wiper register remains unaltered. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close the L terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_L_FULL Command

Moves wiper to full-scale position (0xFF) and opens the L terminal. The wiper register remains unaltered. Writes cannot be made to the wiper register while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close the L terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

SD_W Command

Opens the W terminal keeping the internal tap position the same as the wiper register. Writes cannot be made to the wiper registers while shutdown mode is engaged. Clearing shutdown mode will return the wiper to the position contained in the wiper register and close W terminal. A RST will also deassert shutdown mode and return the wiper to midscale (0x80). This command does not affect the charge-pump status.

QP_OFF Command

Disables the onboard charge pump and places device in low power mode. Low supply voltage is limited to 2.6V.

QP_ON Command

Enables the onboard charge pump to allow low-supply voltage operation. This is the power-on default condition. Low supply voltage is 1.7V.

RST Command

Returns the device to power-on default conditions. Resets the wiper register to midscale (0x80), enables charge pump, and deasserts any shutdown modes.

Ordering Information

PART	PIN-PACKAGE	INTERFACE	TAPS	END-TO-END RESISTANCE (kΩ)
MAX5395LATA+T	8 TDFN-EP*	I2C	256	10
MAX5395MATA+T	8 TDFN-EP*	I2C	256	50
MAX5395NATA+T	8 TDFN-EP*	I2C	256	100

Note: *All devices operate over the -40°C to +125°C temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T822+2	21-0168	90-0065

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	9/12	Revised the *Absolute Maximum Ratings*	2
2	11/14	Removed automotive references from data sheet	1, 10
3	2/16	Add charge pump current at various disabled conditions	3

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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