+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
$\overline{CS}$, SCLK, DIN, $\overline{CLR}$ to GND .....-0.3V to +6V
REF to GND .....-0.3V to (V_{DD} + 0.3V)
OUT, INV to GND .....-0.3V to V_{DD}
RFB to INV .....-6V to +6V
RFB to GND .....-6V to +6V
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Ranges
MAX514_ EUA .....-40°C to +85°C
MAX514_ EUB .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Die Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V (MAX5143/MAX5144) or +5V (MAX5141/MAX5142), V_{REF} = +2.5V, T_A = T_{MIN} to T_{MAX}, C_L = 10pF, GND = 0, R_L = ∞, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		14			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic		±0.5	±1	LSB
Integral Nonlinearity	INL	MAX514_		±0.5	±1	LSB
Zero-Code Offset Error	ZSE				±2	LSB
Zero-Code Tempco	ZS_{TC}			±0.05		ppm/°C
Gain Error (Note 1)					±10	LSB
Gain-Error Tempco				±0.1		ppm/°C
DAC Output Resistance	R_{OUT}	(Note 2)		6.2		kΩ
Bipolar Resistor Matching		R_{FB}/R_{INV}		1		%
		Ratio error			±0.03	
Bipolar Zero Offset Error					±20	LSB
Bipolar Zero Tempco	BZS_{TC}			±0.5		ppm/°C
Power-Supply Rejection	PSR	+2.7V ≤ V_{DD} ≤ +3.3V (MAX5143/MAX5144)			±1	LSB
		+4.5V ≤ V_{DD} ≤ +5.5V (MAX5141/MAX5142)			±1	
Reference Input Range	V_{REF}	(Note 3)	2.0		V_{DD}	V
Reference Input Resistance (Note 4)	R_{REF}	Unipolar mode	10			kΩ
		Bipolar mode	6			
DYNAMIC PERFORMANCE—ANALOG SECTION						
Voltage-Output Slew Rate	SR	(Note 5)		15		V/µs
Output Settling Time		To ±½LSB of FS		1		µs
DAC Glitch Impulse		Major-carry transition		7		nV-s
Digital Feedthrough		Code = 0000 hex; $\overline{CS}$ = V_{DD}; SCLK, DIN = 0V to V_{DD} levels		0.2		nV-s

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V (MAX5143/MAX5144) or +5V (MAX5141/MAX5142), V_{REF} = +2.5V, T_A = T_{MIN} to T_{MAX}, C_L = 10pF, GND = 0, RL = ∞, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE—REFERENCE SECTION							
Reference -3dB Bandwidth	BW	Code = 3FFF hex			1		MHz
Reference Feedthrough		Code = 0000 hex, V_{REF} = $1V_{P-P}$ at 100kHz			1		mV_{P-P}
Signal-to-Noise Ratio	SNR				92		dB
Reference Input Capacitance	C_{INREF}	Code = 0000 hex			70		pF
		Code = 3FFF hex			170		
STATIC PERFORMANCE—DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Current	I_{IN}					±1	µA
Input Capacitance	C_{IN}	(Note 6)			3	10	pF
Hysteresis Voltage	V_H				0.15		V
POWER SUPPLY							
Positive Supply Range (Note 7)	V_{DD}	MAX5143/MAX5144		2.7		3.6	V
		MAX5141/MAX5142		4.5		5.5	
Positive Supply Current	I_{DD}	All digital inputs at V_{DD} or GND			0.12	0.20	mA
Power Dissipation	PD	All digital inputs at V_{DD} or GND	MAX5143/MAX5144		0.36		mW
			MAX5141/MAX5142		0.60		

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.3V (MAX5143/MAX5144), V_{DD} = +4.5V to +5.5V (MAX5141/MAX5142), V_{REF} = +2.5V, GND = 0, CMOS inputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{CLK}				25	MHz
SCLK Pulse Width High	t_{CH}		20			ns
SCLK Pulse Width Low	t_{CL}		20			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		15			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		15			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	(Note 6)	35			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		20			ns
DIN to SCLK High Setup	t_{DS}		15			ns
DIN to SCLK High Hold	t_{DH}		0			ns
$\overline{CLR}$ Pulse Width Low	t_{CLW}		20			ns
V_{DD} High to $\overline{CS}$ Low (Power-Up Delay)				20		µs

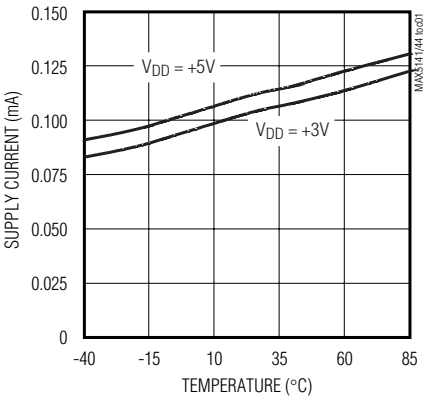
Note 1: Gain error tested at V_{REF} = +2.0V, +2.5V, and +3.0V (MAX5143/MAX5144) or V_{REF} = +2.0V, +2.5V, +3.0V, and +5.0V (MAX5141/MAX5142).
Note 2: R_{OUT} tolerance is typically ±20%.
Note 3: Min/max range guaranteed by gain-error test. Operation outside min/max limits will result in degraded performance.
Note 4: Reference input resistance is code dependent, minimum at 2155 hex in unipolar mode, 1155 hex in bipolar mode.
Note 5: Slew-rate value is measured from 10% to 90%.
Note 6: Guaranteed by design. Not production tested.
Note 7: Guaranteed by power-supply rejection test and *Timing Characteristics*.

+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs

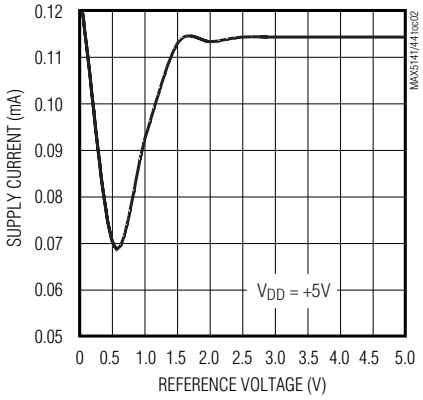
Typical Operating Characteristics

(V_{DD} = +3V (MAX5143/MAX5144) or +5V (MAX5141/MAX5142), V_{REF} = +2.5V, T_A = T_{MIN} to T_{MAX}, GND = 0, R_L = ∞, unless otherwise noted. Typical values are at T_A = +25°C.)

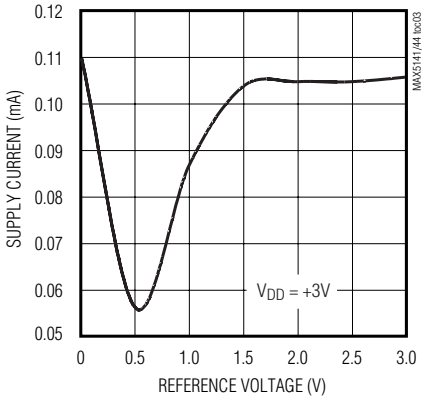
SUPPLY CURRENT vs. TEMPERATURE



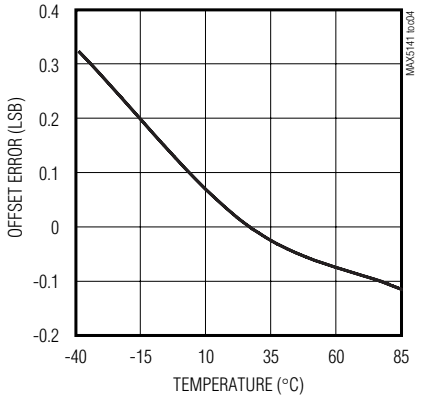
SUPPLY CURRENT vs. REFERENCE VOLTAGE



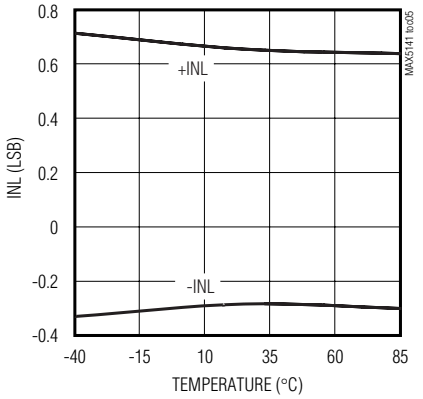
SUPPLY CURRENT vs. REFERENCE VOLTAGE



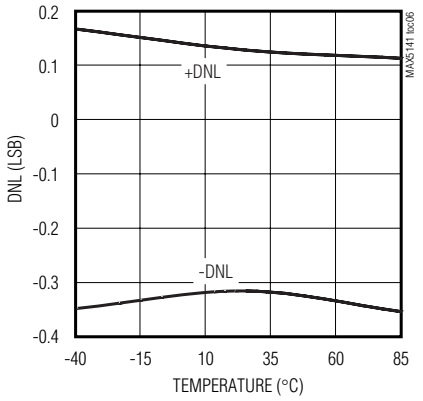
ZERO-CODE OFFSET ERROR vs. TEMPERATURE



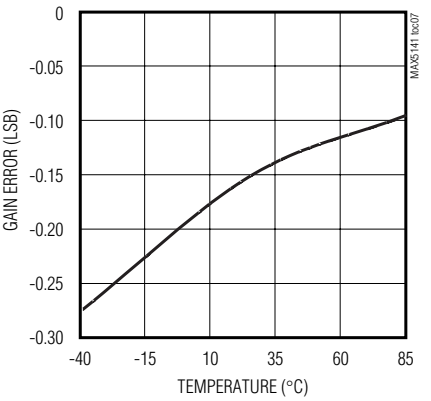
INTEGRAL NONLINEARITY vs. TEMPERATURE



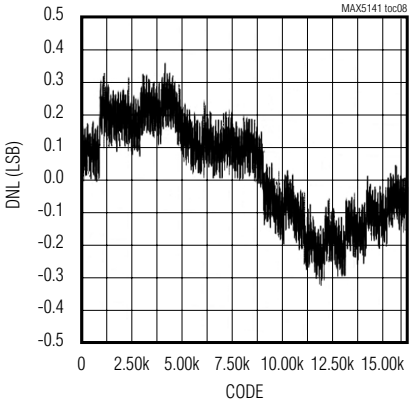
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



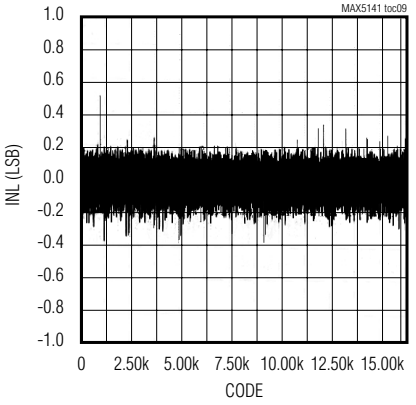
GAIN ERROR vs. TEMPERATURE



DIFFERENTIAL NONLINEARITY vs. CODE



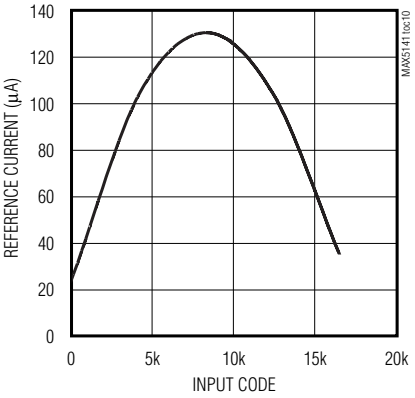
INTEGRAL NONLINEARITY vs. CODE



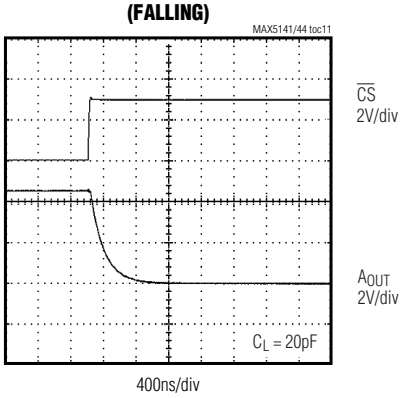
Typical Operating Characteristics (continued)

(V_{DD} = +3V (MAX5143/MAX5144) or +5V (MAX5141/MAX5142), V_{REF} = +2.5V, T_A = T_{MIN} to T_{MAX}, GND = 0, R_L = ∞, unless otherwise noted. Typical values are at T_A = +25°C.)

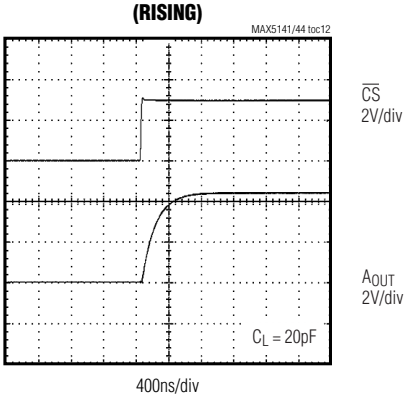
REFERENCE CURRENT vs. DIGITAL INPUT CODE



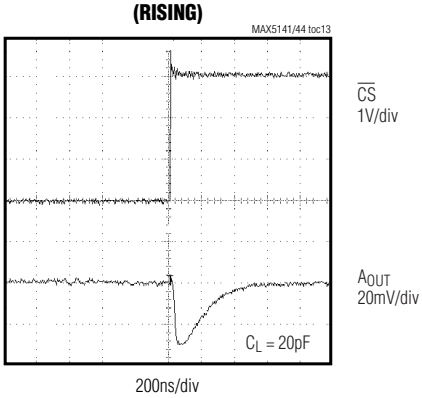
FULL-SCALE STEP RESPONSE (FALLING)



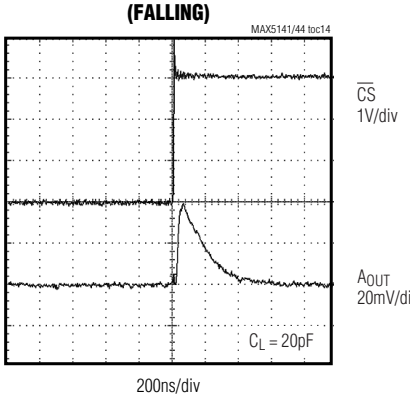
FULL-SCALE STEP RESPONSE (RISING)



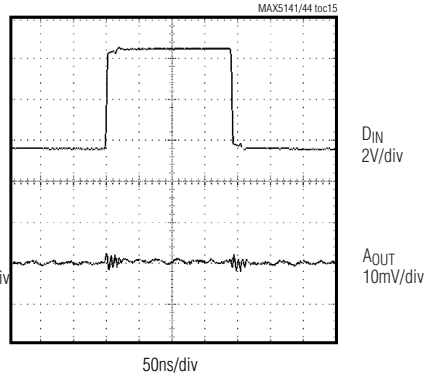
MAJOR-CARRY GLITCH (RISING)



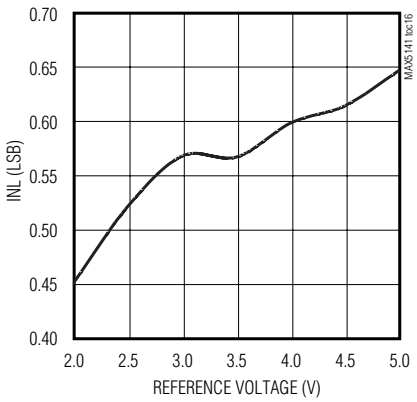
MAJOR-CARRY GLITCH (FALLING)



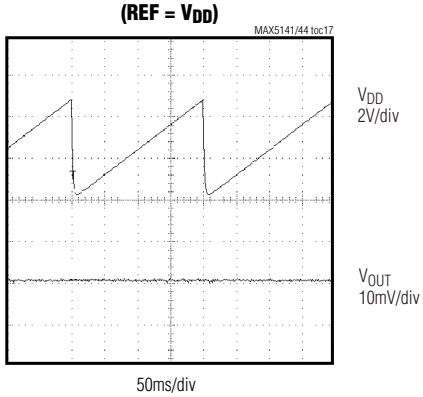
DIGITAL FEEDTHROUGH



INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



UNIPOLAR POWER-ON GLITCH (REF = V_{DD})



+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Pin Descriptions

PIN		NAME	FUNCTION
MAX5141 MAX5143	MAX5142 MAX5144		
1	1	REF	Voltage Reference Input
2	2	$\overline{CS}$	Chip-Select Input
3	3	SCLK	Serial Clock Input. Duty cycle must be between 40% and 60%.
4	4	DIN	Serial Data Input
5	5	$\overline{CLR}$	Clear Input. Logic low asynchronously clears the DAC to code 0 (MAX5141/MAX5143) or code 8192 (MAX5142/MAX5144).
6	6	OUT	DAC Output Voltage
—	7	INV	Junction of Internal Scaling Resistors. Connect to external op amp's inverting input in bipolar mode.
—	8	RFB	Feedback Resistor. Connect to external op amp's output in bipolar mode.
7	9	V_{DD}	Supply Voltage. Use +3V for MAX5143/MAX5144 and +5V for MAX5141/MAX5142.
8	10	GND	Ground

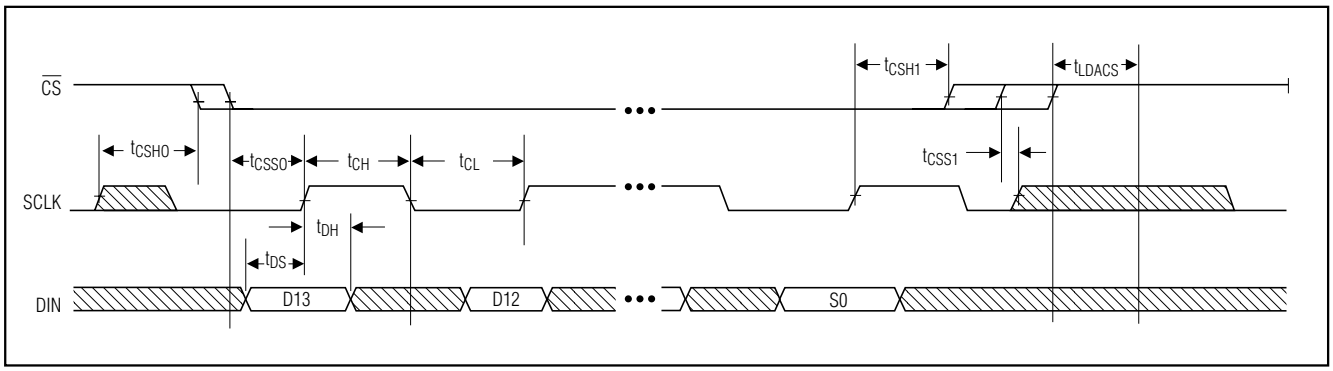


Figure 1. Timing Diagram

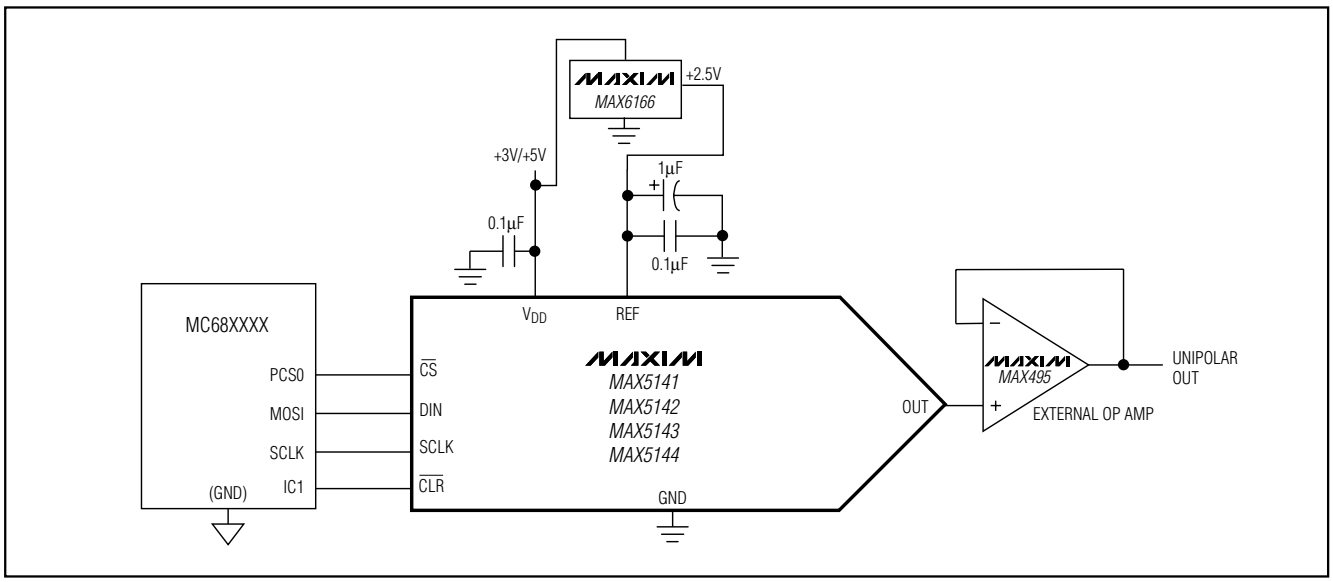


Figure 2a. Typical Operating Circuit—Unipolar Output

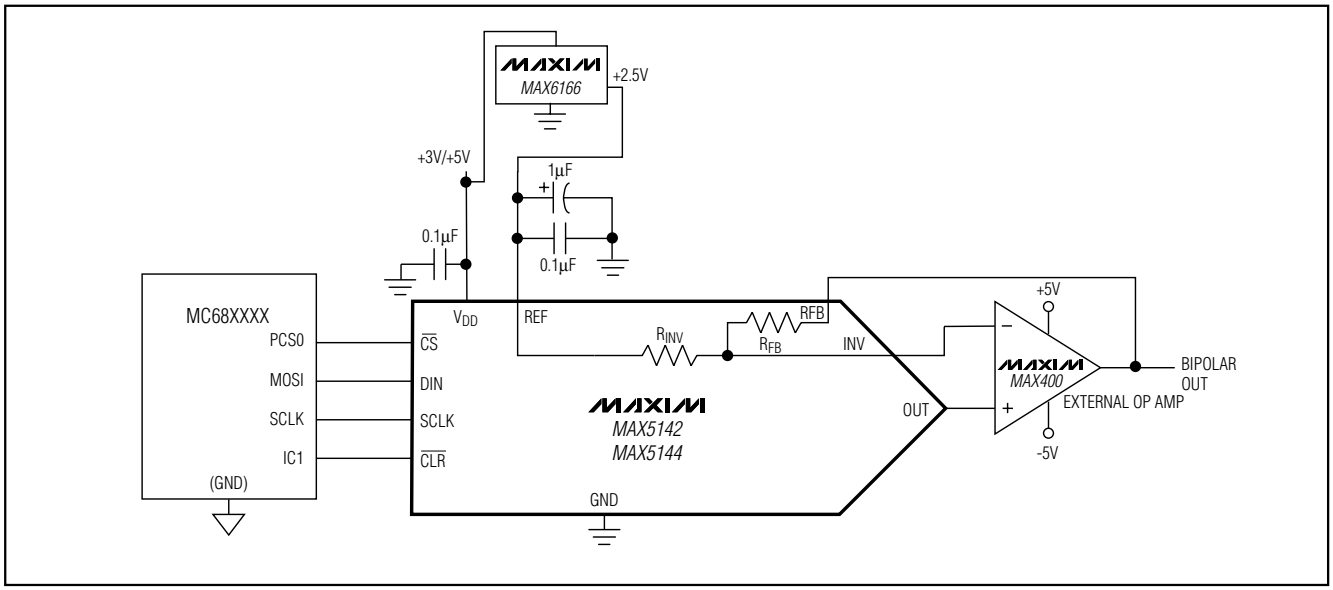


Figure 2b. Typical Operating Circuit—Bipolar Output

Detailed Description

The MAX5141–MAX5144 voltage-output, 14-bit digital-to-analog converters (DACs) offer full 14-bit performance with less than 1LSB integral linearity error and less than 1LSB differential linearity error, thus ensuring monotonic performance. Serial data transfer minimizes the number of package pins required.

The MAX5141–MAX5144 are composed of two matched DAC sections, with a 10-bit inverted R-2R DAC forming the ten LSBs and the four MSBs derived from 15 identically matched resistors. This architecture allows the lowest glitch energy to be transferred to the DAC output on major-carry transitions. It also lowers the DAC output impedance by a factor of eight compared

+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs

to a standard R-2R ladder, allowing unbuffered operation in medium-load applications.

The MAX5142/MAX5144 provide matched bipolar offset resistors, which connect to an external op amp for bipolar output swings (Figure 2b).

Digital Interface

The MAX5141–MAX5144 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data-input pin (DIN). Immediately following $\overline{CS}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 bits (14 data bits, plus two subbits set to zero) have been loaded into the serial input register, it transfers its contents to the DAC latch on $\overline{CS}$'s low-to-high transition (Figure 3). Note that if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

Clearing the DAC

A 20ns (min) logic low pulse on $\overline{CLR}$ asynchronously clears the DAC buffer to code 0 in the MAX5141/MAX5143 and to code 8192 in the MAX5142/MAX5144.

External Reference

The MAX5141–MAX5144 operate with external voltage references from +2V to V_{DD}. The reference voltage determines the DAC's full-scale output voltage.

Power-On Reset

The power-on reset circuit sets the output of the MAX5141/MAX5143 to code 0 and the output of the MAX5142/MAX5144 to code 8192 when V_{DD} is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after a loss of power.

Applications Information

Reference and Ground Inputs

The MAX5141–MAX5144 operate with external voltage references from +2V to V_{DD}, and maintain 14-bit performance if certain guidelines are followed when selecting and applying the reference. Ideally, the reference's temperature coefficient should be less than 0.5ppm/°C to maintain 14-bit accuracy to within 1LSB over the -40°C to +85°C extended temperature range. Since this converter is designed as an inverted R-2R voltage-mode DAC, the input resistance seen by the voltage reference is code dependent. In unipolar mode, the worst-case input-resistance variation is from 11.5kΩ (at code 2155 hex) to 200kΩ (at code 0000 hex). The maximum change in load current for a +2.5V reference is +2.5V / 11.5kΩ = 217µA; therefore, the required load regulation is 28ppm/mA for a maximum error of 0.1LSB. This implies a reference output impedance of less than 72mΩ. In addition, the signal-path impedance from the voltage reference to the reference input must be kept low because it contributes directly to the load-regulation error.

The requirement for a low-impedance voltage reference is met with capacitor bypassing at the reference inputs and ground. A 0.1µF ceramic capacitor with short leads between REF and GND provides high-frequency bypassing. A surface-mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional 1µF between REF and GND provides low-frequency bypassing. A low-ESR tantalum, film, or organic semiconductor capacitor works well. Leaded capacitors are acceptable because impedance is not as criti-

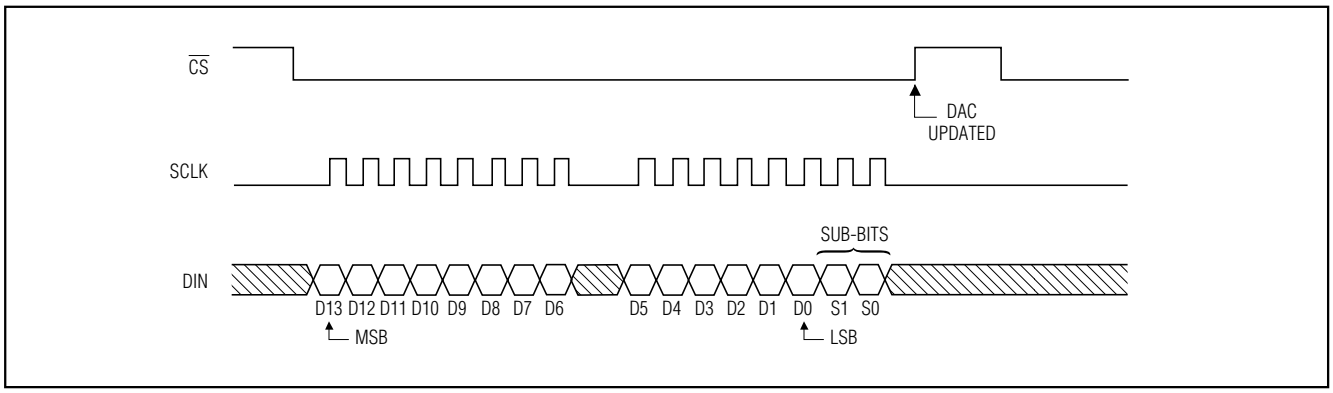


Figure 3. MAX5141–MAX5144 3-Wire Interface Timing Diagram

cal at lower frequencies. The circuit can benefit from even larger bypassing capacitors, depending on the stability of the external reference with capacitive loading.

Unbuffered Operation

Unbuffered operation reduces power consumption as well as offset error contributed by the external output buffer. The R-2R DAC output is available directly at OUT, allowing 14-bit performance from $+V_{REF}$ to GND without degradation at zero scale. The DAC's output impedance is also low enough to drive medium loads (R_L > 60kΩ) without degradation of INL or DNL; only the gain error is increased by externally loading the DAC output.

External Output Buffer Amplifier

The requirements on the external output buffer amplifier change whether the DAC is used in unipolar or bipolar operational mode. In unipolar mode, the output amplifier is used in a voltage-follower connection. In bipolar mode (MAX5142/MAX5144 only), the amplifier operates with the internal scaling resistors (Figure 2b). In each mode, the DAC's output resistance is constant and is independent of input code; however, the output amplifier's input impedance should still be as high as possible to minimize gain errors. The DAC's output capacitance is also independent of input code, thus simplifying stability requirements on the external amplifier.

In bipolar mode, a precision amplifier operating with dual power supplies (such as the MAX400) provides the $\pm V_{REF}$ output range. In single-supply applications, precision amplifiers with input common-mode ranges including GND are available; however, their output swings do not normally include the negative rail (GND) without significant degradation of performance. A single-supply op amp, such as the MAX495, is suitable if the application does not use codes near zero.

Since the LSBs for a 14-bit DAC are extremely small (152.6µV for V_{REF} = +2.5V), pay close attention to the external amplifier's input specification. The input offset voltage can degrade the zero-scale error and might require an output offset trim to maintain full accuracy if the offset voltage is greater than 1/2LSB. Similarly, the input bias current multiplied by the DAC output resistance (typically 6.25kΩ) contributes to zero-scale error. Temperature effects also must be taken into consideration. Over the -40°C to +85°C extended temperature range, the offset voltage temperature coefficient (referenced to +25°C) must be less than 0.95µV/°C to add less than 1/2LSB of zero-scale error. The external amplifier's input resistance forms a resistive divider with the DAC output resistance, which results in a gain error. To contribute less than 1/2LSB of gain error, the input resistance typically must be greater than:

$$6.25k\Omega \times 2^{15} = 205M\Omega$$

The settling time is affected by the buffer input capacitance, the DAC's output capacitance, and PC board capacitance. The typical DAC output voltage settling time is 1µs for a full-scale step. Settling time can be significantly less for smaller step changes. Assuming a single time-constant exponential settling response, a full-scale step takes 10.4 time constants to settle to within 1/2LSB of the final output voltage. The time constant is equal to the DAC output resistance multiplied by the total output capacitance. The DAC output capacitance is typically 10pF. Any additional output capacitance increases the settling time.

The external buffer amplifier's gain-bandwidth product is important because it increases the settling time by adding another time constant to the output response. The effective time constant of two cascaded systems, each with a single time-constant response, is approximately the root square sum of the two time constants. The DAC output's time constant is 1µs / 10.4 = 96ns, ignoring the effect of additional capacitance. If the time constant of an external amplifier with 1MHz bandwidth is 1 / 2π (1MHz) = 159ns, then the effective time constant of the combined system is:

$$\sqrt{\left[(96ns)^2 + (159ns)^2\right]} = 186ns$$

This suggests that the settling time to within 1/2LSB of the final output voltage, including the external buffer amplifier, will be approximately 10.4 × 186ns = 1.93µs.

Digital Inputs and Interface Logic

The digital interface for the 14-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and MICROWIRE interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input data serially into the DAC.

A 20ns (min) logic low pulse to $\overline{CLR}$ clears the data in the DAC buffer.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5141–MAX5144 without additional external logic. The digital inputs are compatible with TTL/CMOS-logic levels.

+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Unipolar Configuration

Figure 2a shows the MAX5141–MAX5144 configured for unipolar operation with an external op amp. The op amp is set for unity gain, and Table 1 lists the codes for this circuit. Bipolar MAX5142/MAX5144 can also be used in unipolar configuration by connecting RFB and INV to REF. This allows the DAC to power up to midscale.

Bipolar Configuration

Figure 2b shows the MAX5141–MAX5144 configured for bipolar operation with an external op amp. The op amp is set for unity gain with an offset of -1/2V_{REF}. Table 2 shows the offset binary codes for this circuit (less than 0.25 inches).

Power-Supply Bypassing and Ground Management

Bypass V_{DD} with a 0.1µF ceramic capacitor connected between V_{DD} and GND. Mount the capacitor with short leads close to the device (less than 0.25 inches).

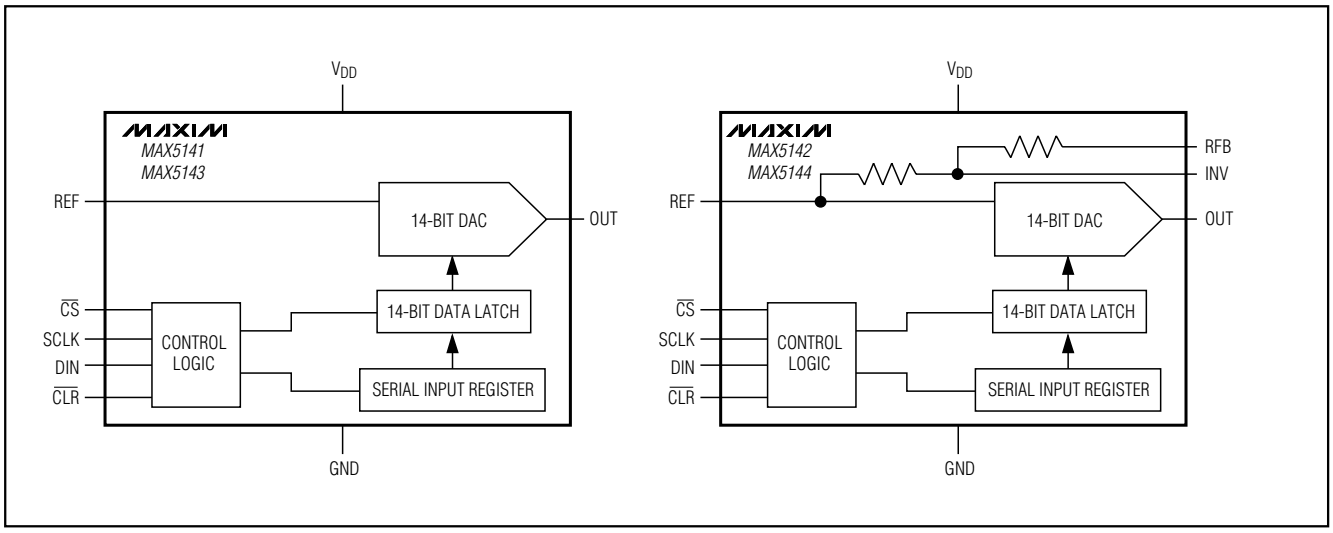
Table 1. Unipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 11	$V_{REF} \times (16{,}383 / 16{,}384)$
1000 0000 0000 00	$V_{REF} \times (8192 / 16{,}384) = {}^{1}/_{2}V_{REF}$
0000 0000 0000 01	$V_{REF} \times (1 / 16{,}384)$

Table 2. Bipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 11	$+V_{REF} \times (8191 / 8192)$
1000 0000 0000 01	$+V_{REF} \times (1 / 8192)$
1000 0000 0000 00	0V
0111 1111 1111 11	$-V_{REF} \times (1 / 8192)$
0000 0000 0000 00	$-V_{REF} \times (8192 / 8192) = -V_{REF}$

Functional Diagrams

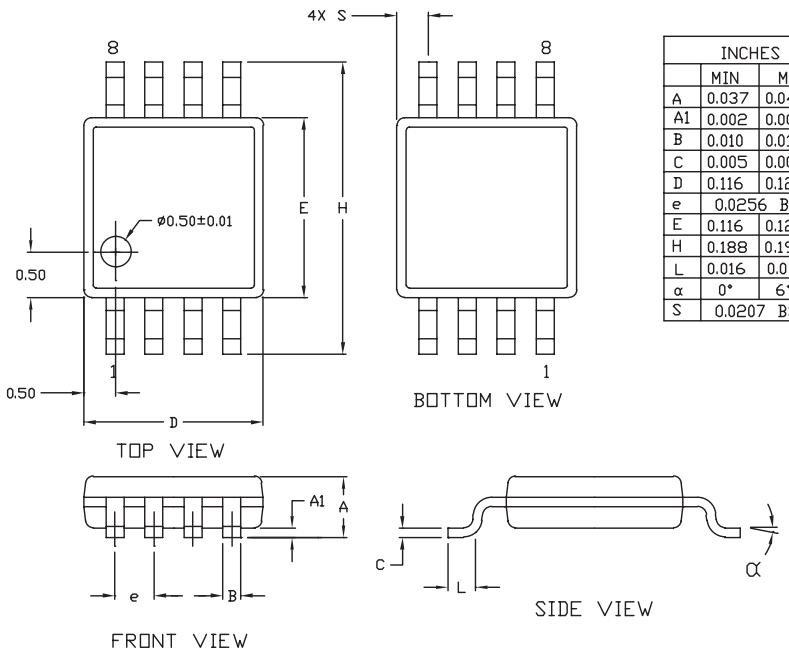


Chip Information

TRANSISTOR COUNT: 2800

PROCESS: BiCMOS

Package Information



	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC					

8LUMAXD.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.

MAXIM
PROPRIETARY INFORMATION

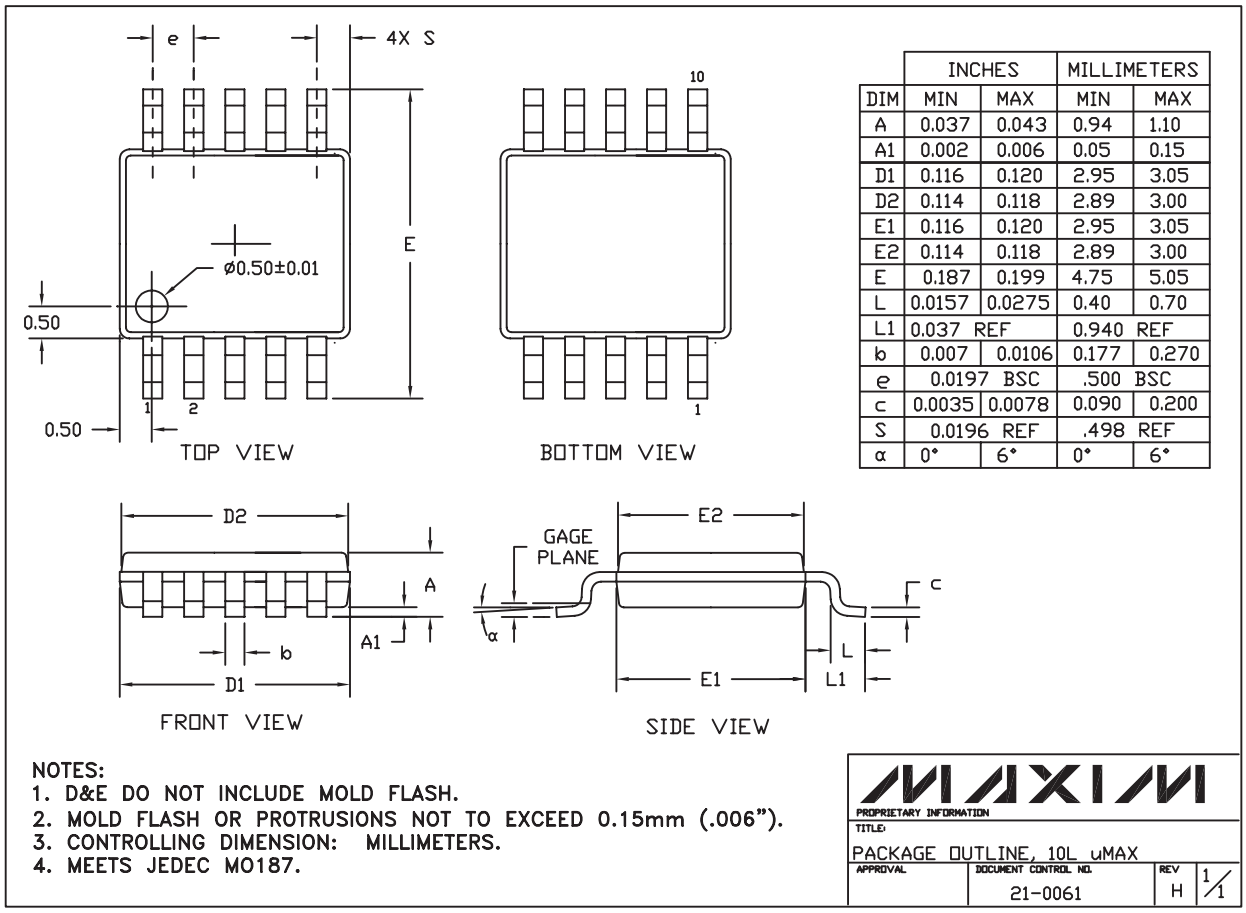
TITLE: PACKAGE OUTLINE, 8L uMAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	I	1/1

MAX5141–MAX5144

+3V/+5V, Serial-Input, Voltage-Output, 14-Bit DACs

Package Information (continued)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10
A1	0.002	0.006	0.05	0.15
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
E	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO187.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0061 | REV H | 1/1