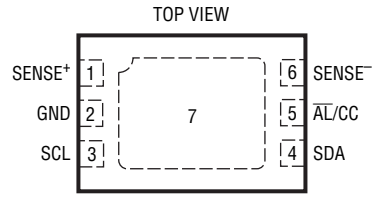
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (SENSE+) ..... –0.3V to 6V
SCL, SDA, $\overline{AL}$/CC ..... –0.3V to 6V
Sense Current (into SENSE–) ..... ±2A
Operating Ambient Temperature Range
LTC2941-1C ..... 0°C to 70°C
LTC2941-1I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 160°C/W (NOTE 8)
EXPOSED PAD (PIN 7): DO NOT CONNECT

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2941CDCB-1#TRMPBF	LTC2941CDCB-1#TRPBF	LFKP	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC2941IDCB-1#TRMPBF	LTC2941IDCB-1#TRPBF	LFKP	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
V_{SENSE+}	Supply Voltage			2.7		5.5	V
I_{SUPPLY}	Supply Current (Note 3)	Device On	 ●		70	100 120	µA µA
		Shutdown	●			2.5	µA
		Shutdown, $V_{SENSE+} \le 4.2V$				1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{SENSE+} Falling	●	2.5	2.6	2.7	V
Coulomb Counter							
I_{SENSE-}	Sense Current		●			±1	A
R_{SENSE}	Internal Sense Resistance				50		mΩ
R_{PP}	Pin-to-Pin Resistance from SENSE+ to SENSE–	(Note 7)		50	74	100	mΩ
q_{LSB}	Charge LSB (Note 4)	Prescaler M = 128 (Default)			0.085		mAh
TCE	Total Charge Error (Note 5)	$0.2A \le \lvert I_{SENSE} \rvert \le 1A$ DC				±1	%
		$0.2A \le \lvert I_{SENSE} \rvert \le 1A$ DC, 0°C to 70°C				±1.8	%
		$0.02A \le \lvert I_{SENSE} \rvert \le 1A$ DC (Note 7)	●			±2.8	%
V_{bat} Alert	V_{bat} Alert Threshold	V_{SENSE-} Falling, B[7:6] = 01, I_{SENSE-} = 0A	●	2.75	2.8	2.85	V
		V_{SENSE-} Falling, B[7:6] = 10, I_{SENSE-} = 0A	●	2.85	2.9	2.95	V
		V_{SENSE-} Falling, B[7:6] = 11, I_{SENSE-} = 0A	●	2.95	3	3.05	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs and Digital Outputs							
V_{ITH}	Logic Input Threshold, $\overline{AL}$/CC, SCL, SDA		●	0.3 • V_{SENSE+}		0.7 • V_{SENSE+}	V
V_{OL}	Low Level Output Voltage, $\overline{AL}$/CC, SDA	I = 3mA	●			0.4	V
I_{IN}	Input Leakage, $\overline{AL}$/CC, SCL, SDA	V_{IN} = V_{SENSE+}/2	●			1	µA
C_{IN}	Input Capacitance, $\overline{AL}$/CC, SCL, SDA	(Note 7)	●			10	pF
t_{PCC}	Minimum Charge Complete (CC) Pulse Width					1	µs
I²C Timing Characteristics							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400	900		kHz
$t_{BUF(MIN)}$	Bus Free Time Between Stop/Start		●			1.3	µs
$t_{SU,STA(MIN)}$	Minimum Repeated Start Setup Time		●			600	ns
$t_{HD,STA(MIN)}$	Minimum Hold Time (Repeated) Start Condition		●			600	ns
$t_{SU,STO(MIN)}$	Minimum Setup Time for Stop Condition		●			600	ns
$t_{SU,DAT(MIN)}$	Minimum Data Setup Time Input		●			100	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input		●			0	µs
$t_{HD,DATO}$	Data Hold Time Output		●	0.3		0.9	µs
t_{of}	Data Output Fall Time	(Notes 6, 7)	●	20 + 0.1 • C_B		300	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified

Note 3: I_{SUPPLY} = I_{SENSE+} + $I_{SENSE–}$

Note 4: The equivalent charge of an LSB in the accumulated charge registers (C,D) depends on the setting of the internal pre-scaling factor M. It is calculated by:

$$q_{LSB} = 0.085mAh \bullet \frac{M}{128}$$

See Choosing Coulomb Counter Prescaler M section for more information.

1mAh = 3.6A • s = 3.6C (Coulomb), 0.085mAh = 306mC.

Note 5: Deviation of q_{LSB} from its nominal value. Data is for a new device and does not include long-term sense resistor aging. See the Internal Sense Resistor section for more information.

Note 6: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 7: Guaranteed by design, not subject to test.

Note 8: Value decreases if exposed pad is soldered to large copper area. See Power Dissipation section for more information.

TIMING DIAGRAM

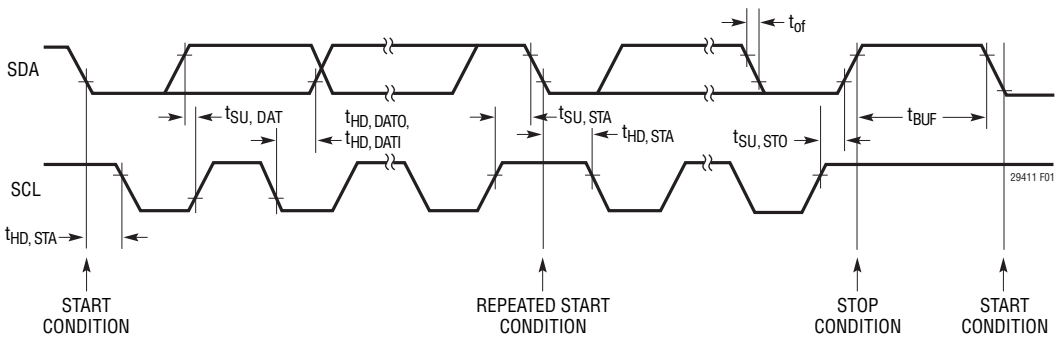
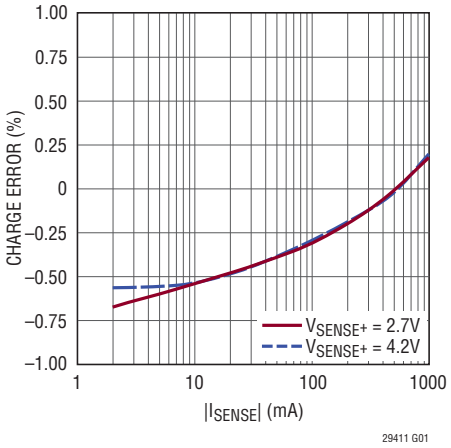


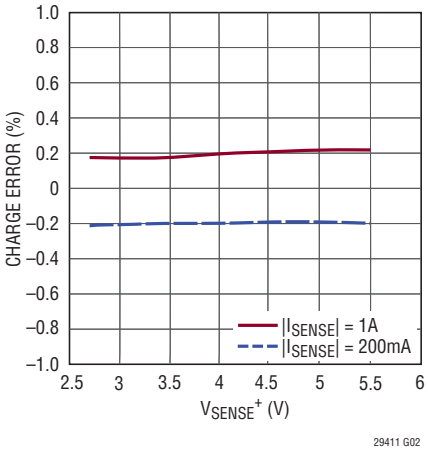
Figure 1. Definition of Timing on I²C Bus

TYPICAL PERFORMANCE CHARACTERISTICS

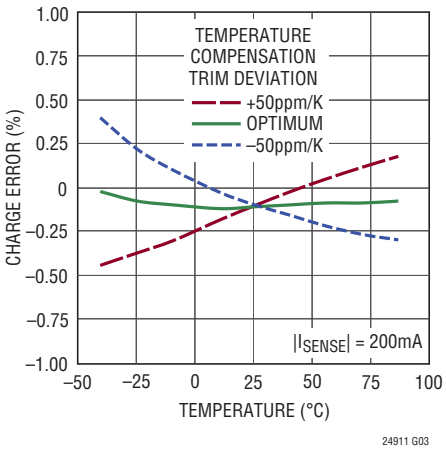
Total Charge Error vs Sense Current



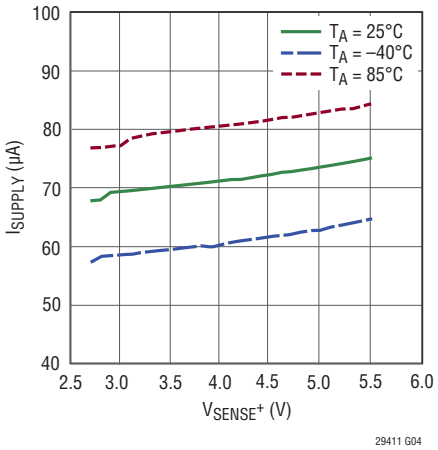
Total Charge Error vs Supply Voltage



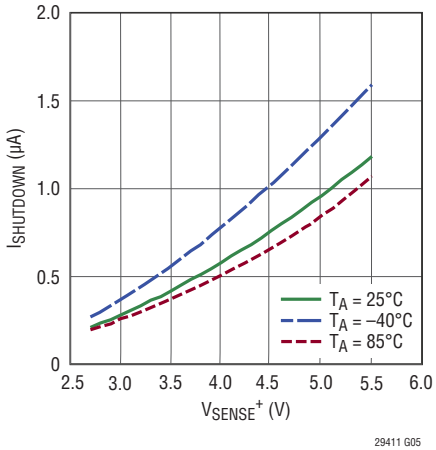
Total Charge Error vs Temperature



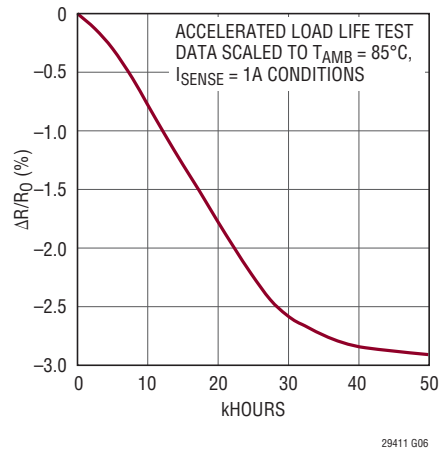
Supply Current vs Supply Voltage



Shutdown Supply Current vs Supply Voltage



Sense Resistor Stability



PIN FUNCTIONS

SENSE+ (Pin 1): Positive Current Sense Input and Power Supply. Connect to the load and battery charger output. V_{SENSE+} operating range is 2.7V to 5.5V.

GND (Pin 2): Device Ground. Connect directly to the negative battery terminal.

SCL (Pin 3): Serial Bus Clock Input.

SDA (Pin 4): Serial Bus Data Input and Output.

$\overline{AL}$/CC (Pin 5): Alert Output or Charge Complete Input. Configured either as an SMBus alert output or charge complete input by control register bits B[2:1]. At power-up, the pin defaults to alert mode conforming to the SMBus alert response protocol. It behaves as an open-drain logic output that pulls to GND when a value in the threshold registers is exceeded.

When configured as a charge complete input, a high level at CC sets the value of the accumulated charge (registers C, D) to FFFFh. Coulomb counting starts when the input returns to low level.

SENSE– (Pin 6): Negative Current Sense Input. Connect SENSE– to the positive battery terminal. Current from/into this pin must not exceed 1A in normal operation.

Exposed Pad (Pin 7): Do Not Connect. Soldering the exposed pad to adequate electrically isolated copper area is recommended for best thermal performance.

BLOCK DIAGRAM

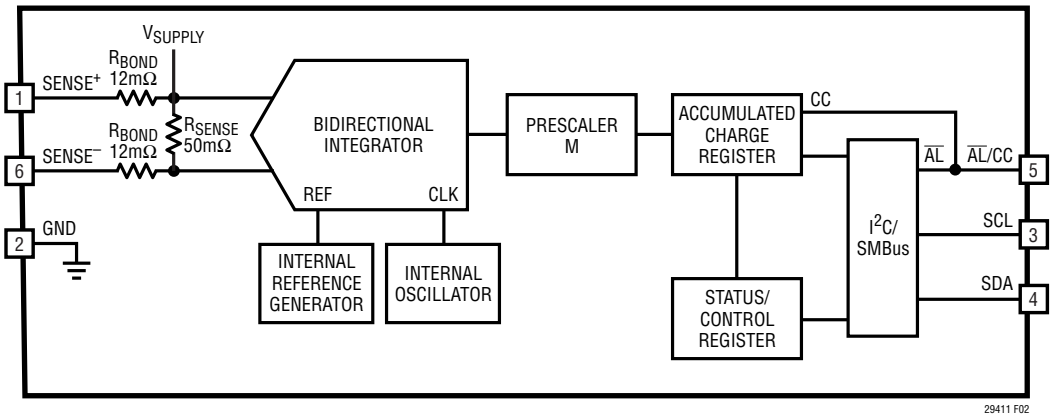


Figure 2. Block Diagram of the LTC2941-1

OPERATION

Overview

The LTC2941-1 is a battery gas gauge device designed for use with single Li-Ion cells and other battery types with terminal voltages from 2.7V to 5.5V. A precision coulomb counter integrates current through an internal sense resistor between the battery's positive terminal and the load or charger. The integrated, temperature-compensated sense resistor offers board space savings and superior charge measurement accuracy in applications with currents up to 1A.

Coulomb Counter

Charge is the time integral of current. The LTC2941-1 measures battery current by monitoring the voltage developed across its internal sense resistor and then integrates this information to infer charge. The internal sense resistor is tied between the $SENSE^+$ and $SENSE^-$ pins and is connected to an auto-zeroed differential analog integrator which converts the measured current to charge.

When the integrator output reaches the REFHI or REFLO thresholds, switches S1, S2, S3 and S4 toggle to reverse the ramp direction. By observing the condition of the switches and the ramp direction, polarity is determined. A programmable prescaler effectively increases integration time by a factor M programmable from 1 to 128. At each underflow or overflow of the prescaler, the accumulated charge register (ACR) value is incremented or decremented one count. The value of accumulated charge is read via the I^2C interface.

Power-Up Sequence

When V_{SENSE+} rises above a threshold of approximately 2.5V, the LTC2941-1 generates an internal power-on reset (POR) signal and sets all registers to their default state. In the default state, the coulomb counter is active. The accumulated charge is set to mid-scale (7FFFh), the low threshold registers are set to 0000h and all the high threshold registers are set to FFFFh. The alert mode is enabled and the coulomb counter pre-scaling factor M is set to 128.

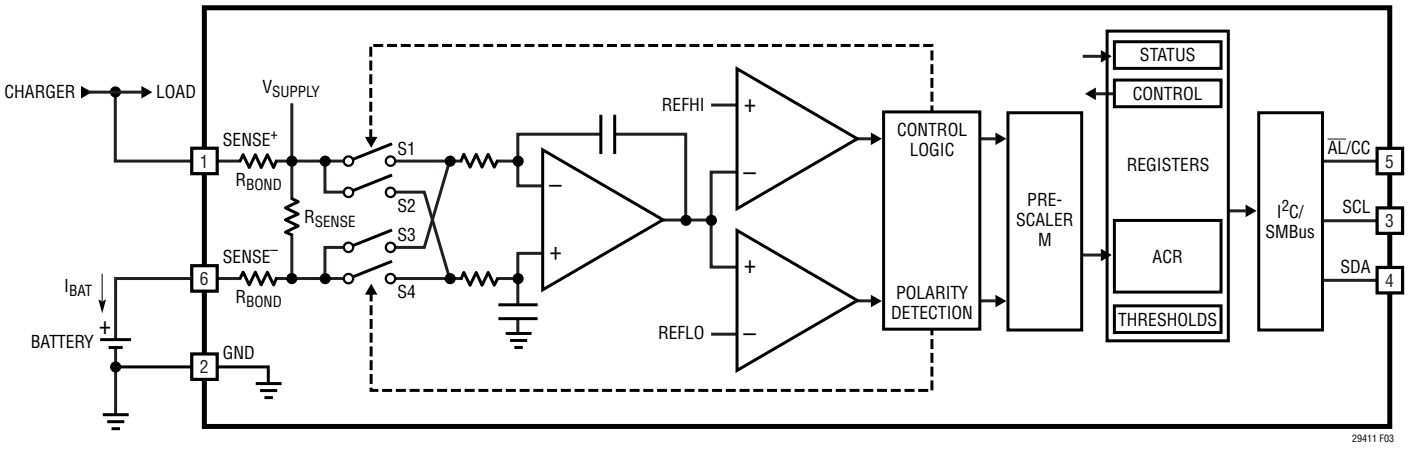


Figure 3. Coulomb Counter Section of the LTC2941-1

APPLICATIONS INFORMATION

I²C/SMBus Interface

The LTC2941-1 communicates with a bus master using a 2-wire interface compatible with I²C and SMBus. The 7-bit hard-coded **I²C address of LTC2941-1 is 1100100**.

The LTC2941-1 is a slave-only device. Therefore, the serial clock line (SCL) is input only while the data line (SDA) is bidirectional. The device supports I²C standard and fast mode. For more details refer to the I²C Protocol section.

Internal Registers

The LTC2941-1 integrates current through a sense resistor and stores a 16-bit result, accumulated charge, as two bytes in registers C and D. Two byte high and low limits programmed in registers E, F, G and H are continuously compared against the accumulated charge. If either limit is exceeded, a corresponding flag is set in the status register bits A[2] or A[3]. If the alert mode is enabled, the $\overline{AL}$/CC pin pulls low.

The internal eight registers are organized as shown in Table 1:

Table 1. Register Map

ADDRESS	NAME	REGISTER DESCRIPTION	R/W	DEFAULT
00h	A	Status	R	See Below
01h	B	Control	R/W	3Ch
02h	C	Accumulated Charge MSB	R/W	7Fh
03h	D	Accumulated Charge LSB	R/W	FFh
04h	E	Charge Threshold High MSB	R/W	FFh
05h	F	Charge Threshold High LSB	R/W	FFh
06h	G	Charge Threshold Low MSB	R/W	00h
07h	H	Charge Threshold Low LSB	R/W	00h

R = Read, W = Write

Status Register (A)

Table 2 shows the details of the status register (address 00h):

Table 2. Status Register A (Read Only)

BIT	NAME	OPERATION	DEFAULT
A[7]	Chip Identification	1: LTC2941-1 0: LTC2942-1	1
A[6]	Reserved	Not Used.	0
A[5]	Accumulated Charge Overflow/Underflow	Indicates that the value of the accumulated charge hit either top or bottom.	0
A[4]	Reserved	Not used.	0
A[3]	Charge Alert High	Indicates that the accumulated charge value exceeded the charge threshold high limit.	0
A[2]	Charge Alert Low	Indicates that the accumulated charge value dropped below the charge threshold low limit.	0
A[1]	V_{BAT} Alert	Indicates that the battery voltage (at $SENSE^-$) dropped below selected V_{BAT} threshold.	0
A[0]	Undervoltage Lockout Alert	Indicates recovery from undervoltage. If equal to 1, a UVLO has occurred and the content of registers is uncertain.	X

The $\overline{AL}$/CC pin can be configured to pull low whenever any status register bit is set (except for bit A[7] and A[0]), using control register bits B[2] and B[1]. All status register bits except A[7] are cleared after being read by the host if the conditions which set these bits have been removed.

As soon as one of the measured quantities exceeds the programmed limits, the corresponding bit A[3], A[2] or A[1] in the status register is set.

APPLICATIONS INFORMATION

Bit A[5] is set if the LTC2941-1's accumulated charge overflows or underflows the combined total in registers C and D. Note that the counting process does not roll over, but simply stops at FFFFh or 0000h until the direction is reversed.

The LTC2941-1 includes a battery undervoltage monitor, which sets bit A1 if the limit is exceeded. Limits are selected in the control register.

The undervoltage lockout (UVLO) bit A[0] is set if, during operation, the voltage on SENSE+ drops below 2.7V without reaching the POR level. The analog parts of the coulomb counter are switched off while the digital register values are retained. After recovery of the supply voltage the coulomb counter resumes integrating with the stored value in the accumulated charge registers (C, D) but it has missed any charge flowing while $V_{SENSE+} < 2.7V$.

The hard coded bit A[7] of the status register enables the host to distinguish the LTC2941-1 from the pin compatible LTC2942-1, allowing the same software to be used with both devices.

Control Register (B)

The operation of the LTC2941-1 can be controlled by programming the control register at address 01h. Table 3 shows the organization of the 8-bit control register B[7:0]

Table 3. Control Register B

BIT	NAME	OPERATION	DEFAULT
B[7:6]	V_{BAT} Alert	[11] Threshold Value = 3.0V. [10] Threshold Value = 2.9V. [01] Threshold Value = 2.8V. [00] V_{BAT} Alert Off.	[00]
B[5:3]	Prescaler M	Sets coulomb counter prescaling factor M between 1 and 128. Default is 128. $M = 2^{(4 \bullet B[5] + 2 \bullet B[4] + B[3])}$.	[111]
B[2:1]	$\overline{AL}$/CC Configure	Configures the $\overline{AL}$/CC pin. [10] Alert Mode. Alert functionality enabled. Pin becomes logic output. [01] Charge Complete Mode. Pin becomes logic input and accepts "charge complete" signal (e.g., from a charger) to set accumulated charge Register to FFFFh. [00] $\overline{AL}$/CC pin disabled. [11] Not allowed.	[10]
B[0]	Shutdown	Shut down analog section to reduce I_{SUPPLY}.	[0]

Power Down B[0]

Programming the last bit B[0] of the control register to 1 sets the analog parts of the LTC2941-1 in power down and the current consumption drops typically below 1µA. All analog circuits are disabled while the values in the registers are retained. Note that any charge flowing while B[0] is 1 is not measured and the charge information below 1LSB of the accumulated charge register is lost.

Alert/Charge Complete Configuration B[2:1]

The $\overline{AL}$/CC pin is a dual function pin configured by the control register. By setting bits B[2:1] to [10] (default) the $\overline{AL}$/CC pin is configured as an alert pin following the SMBus protocol. In this alert mode the $\overline{AL}$/CC pin is a digital output and is pulled low if one of the measured quantities exceeds its high or low threshold or if the an overflow/underflow occurs in the accumulated charge registers C and D. An alert response procedure started by the master resets the alert at the $\overline{AL}$/CC pin. For further information see the Alert Response Protocol section.

Setting the control bits B[2:1] to [01] configures the $\overline{AL}$/CC pin as a digital input. In this mode, a high input on the $\overline{AL}$/CC pin communicates to the LTC2941-1 that the battery is full and the accumulated charge is set to its maximum value FFFFh. Coulomb counting starts when the $\overline{AL}$/CC pin returns to low level.

If neither the alert nor the charge complete functionality is desired, bits B[2:1] should be set to [00]. The $\overline{AL}$/CC pin is then disabled and should be tied to GND. Avoid setting B[2:1] to [11] as it enables the alert and the charge complete modes simultaneously.

Choosing Coulomb Counter Prescaler 'M' B[5:3]

To use as much of the range of the accumulated charge register as possible the prescaler factor M is chosen based on battery capacity Q_{BAT}:

$$M \geq 128 \bullet \frac{Q_{BAT}}{2^{16} \bullet 0.085mAh} = \frac{23}{Ah} \bullet Q_{BAT}$$

M can be set to 1, 2 ,4, 8,... 128 by programming B[5:3] of the control register as $M = 2^{(4 \bullet B[5] + 2 \bullet B[4] + B[3])}$.

APPLICATIONS INFORMATION

The default value after power up is M = 128 = 2^7 (B[5:3] = 111). The maximum battery capacity supported within the prescaler range is 5.5Ah with M = 128. See the section Extending Coulomb Counter Range if battery capacity is higher.

Depending on the choice of prescaler factor M, the charge LSB of the accumulated charge register becomes:

$$q_{LSB} = 0.085mAh \bullet \frac{M}{128}$$

Note that the internal digital resolution of the coulomb counter is higher than indicated by q_{LSB}. The internal charge resolution is typically 299µAs.

V_{BAT} Alert B[7:6]

The V_{BAT} alert function allows the LTC2941-1 to monitor the voltage at SENSE$^-$. If enabled, a drop of the voltage at the SENSE$^-$ pin below a preset threshold is detected and bit A[1] in the status register is set. If the alert mode is enabled by setting B[2] to one, an alert is generated at the $\overline{AL}$/CC pin. The threshold for the V_{BAT} alert function is selectable according to Table 3.

Battery voltage is measured at the internal bond pads connected to SENSE$^-$, hence, the current flowing through the combined pin and bond wire slightly shifts the battery alert threshold levels. For the full-scale current of ±1A at room temperature, this shift is typically ±9mV, which can be ignored for most applications. The V_{BAT} alert thresholds are specified with zero current through the sense resistor.

Accumulated Charge Register (C,D)

The coulomb counter of the LTC2941-1 integrates current through its internal sense resistor over time. The result of this charge integration is stored in the 16-bit accumulated charge register (registers C, D). The amount of charge for a given register contents (C[7:0]D[7:0]) and prescaler setting M can be calculated by:

$$Q = 0.085mAh \bullet \frac{M}{128} \bullet (C \bullet 256 + D)$$

The ACR should be read in a single I^{2}C Read transaction (see Figure 8). If C and D are read in individual single-byte transactions, each with a STOP condition, the register may change between the first and the second transaction due to coulomb count events, causing erroneous charge readings.

As the LTC2941-1 does not know the actual battery status at power-up, the accumulated charge register (ACR) is set to mid-scale (7FFFh). If the host knows the status of the battery, the accumulated charge (C[7:0]D[7:0]) can be either programmed to the correct value via I^{2}C or it can be set after charging to FFFFh (full) by pulling the $\overline{AL}$/CC pin high if charge complete mode is enabled via bits B[2:1]. In this case, FFFFh represents a fully charged battery. If the actual battery capacity is smaller, the host can subtract the excess charge whenever doing the charge calculation, and set the low charge threshold (registers G, H) to the value representing an empty battery. This procedure essentially shifts the zero point of the scale upwards. Before writing the accumulated charge registers, the analog section should be shut down by setting B[0] to 1.

Threshold Registers (E, F), (G, H)

For battery charge, the LTC2941-1 features a high and a low threshold register. At power-up the high threshold is set to FFFFh while the low threshold is set to 0000h. Both thresholds can be programmed to a desired value via I^{2}C. As soon as the accumulated charge exceeds the high threshold or falls below the low threshold, the LTC2941-1 sets the corresponding flag in the status register and pulls the $\overline{AL}$/CC pin low if alert mode is enabled.

I^{2}C Protocol

The LTC2941-1 uses an I^{2}C/SMBus compatible 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the bus wires low and they never drive the bus high. The bus wires should be externally connected to a positive supply voltage via a current source or pull-up resistor. When the bus is idle, both SDA and SCL are high. Data on the I^{2}C-bus can be transferred at rates of up to 100kbit/s in standard mode and up to 400kbit/s in fast mode.

Each device on the I^{2}C/SMbus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the

APPLICATIONS INFORMATION

device. In addition to transmitters and receivers, devices can also be classified as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave. The LTC2941-1 always acts as a slave. Figure 4 shows an overview of the data transmission on the I^2C bus.

Start and Stop Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Data Transmission

After a START condition, the I^2C bus is considered busy and data transfer begins between a master and a slave. As data is transferred over I^2C in groups of nine bits (eight data bits followed by an acknowledge bit), each group takes nine SCL cycles. The transmitter releases the SDA line during the acknowledge clock pulse and the receiver issues an acknowledge (ACK) by pulling SDA low or leaves SDA high to indicate a not-acknowledge (NAK) condition. Change of data state can only happen while SCL is low.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave **address 1100100** and the R/$\overline{W}$ bit set to zero, as shown in Figure 5. The LTC2941-1 acknowledges this by pulling SDA low and then the master sends a command byte which indicates which internal register the master is to write. The LTC2941-1 acknowledges and then latches the command byte into its internal register address pointer. The master delivers the data byte, the LTC2941-1 acknowledges once more and latches the data into the desired register. The transmission is ended when the master sends a STOP condition. If the master continues by sending a second data byte instead of a stop, the LTC2941-1 acknowledges again, increments its address pointer and latches the second data byte in the following register, as shown in Figure 6.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave **address 1100100** and the R/$\overline{W}$ bit set to zero, as shown in Figure 7. The LTC2941-1 acknowledges and then the master sends a command byte which indicates which internal register the master is to read. The LTC2941-1 acknowledges and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/$\overline{W}$ bit now set to one. The LTC2941-1 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, the LTC2941-1 increments its address pointer and sends the contents of the following register as shown in Figure 8.

Alert Response Protocol

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt (Figure 9).

The master initiates the ARA procedure with a START condition and the special **7-bit ARA bus address (0001100)** followed by the read bit (R) = 1. If the LTC2941-1 is asserting the $\overline{AL}$/CC pin in alert mode, it acknowledges and responds by sending its **7-bit bus address (1100100)** and a 1. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LTC2941-1 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LTC2941-1 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LTC2941-1 will stop pulling down the $\overline{AL}$/CC pin and will not respond to further ARA requests until a new alert event occurs.

APPLICATIONS INFORMATION

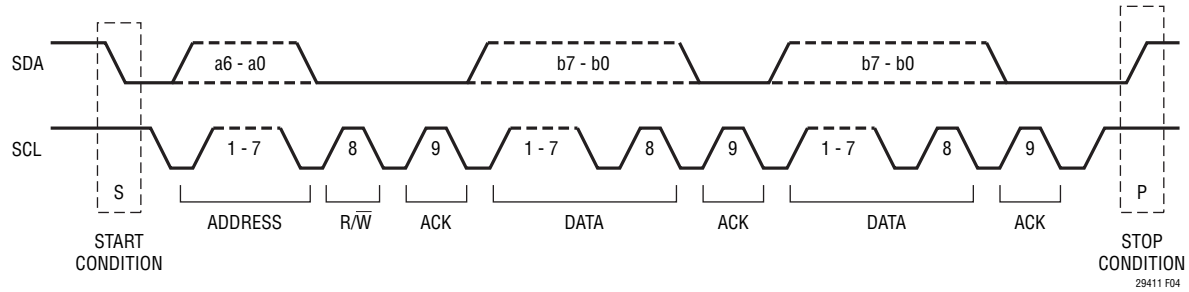


Figure 4. Data Transfer Over I²C or SMBus

S	ADDRESS	W	A	REGISTER	A	DATA	A	P
	1100100	0	0	01h	0	FCh	0	

29411 F05

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
Ā: NOT-ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
W: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 5. Writing FCh to LTC2941-1 Control Register (B)

S	ADDRESS	W	A	REGISTER	A	DATA	A	DATA	A	P
	1100100	0	0	02h	0	F0h	0	01h	0	

29411 F06

Figure 6. Writing F001h to the LTC2941-1 Accumulated Charge Registers (C, D)

S	ADDRESS	W	A	REGISTER	A	S	ADDRESS	R	A	DATA	Ā	P
	1100100	0	0	00h	0		1100100	1	0	81h	1	

29411 F07

Figure 7. Reading the LTC2941-1 Status Register (A)

S	ADDRESS	W	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	Ā	P
	1100100	0	0	02h	0		1100100	1	0	80h	0	01h	1	

29411 F08

Figure 8. Reading the LTC2941-1 Accumulated Charge Registers (C, D)

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	Ā	P
	0001100	1	0	11001001	1	

29411 F09

Figure 9. LTC2941-1 Serial Bus SDA Alert Response Protocol

APPLICATIONS INFORMATION

Internal Sense Resistor

The internal sense resistor uses proprietary* temperature compensation techniques to reduce the effective temperature coefficient to less than ±50ppm/K typically. The effective sense resistance as seen by the coulomb counter is factory trimmed to 50mΩ. Both measures, and the lack of thermocouple effects in the sense resistor connections, contribute to the LTC2941-1's superior charge measurement accuracy compared to competing solutions employing a common 1% tolerance, 50ppm/K tempco discrete current sense resistor.

Like all sense resistors, the integrated sense resistor in the LTC2941-1 will exhibit minor long-term resistance shift. The resistance typically drops less than –0.1% per 1000h at 1A current and 85°C ambient temperature; this outperforms most types of discrete sense resistors except those of the *very high* and *ultrahigh* stability variety. See the Typical Performance Characteristics for expected resistor drift performance under worst-case conditions. Drift will be much slower at lower temperatures. Contact LTC applications for more information.

For most coulomb counter applications this aging behavior of the integrated sense resistor is insignificant compared to the change of battery capacity due to battery aging. The LTC2941-1 is factory trimmed to optimum accuracy when new; for applications which require the best possible coulomb count accuracy over the full product lifetime, the coulomb counter gain can be adjusted in software. For instance, if the error contribution of sense resistor drift must be limited to ±1%, coulomb counts may be biased high by 1% (use factor 1.01), and maximum operational temperature and current then must be derated such that sense resistor drift over product lifetime or calibration intervals is less than –2%.

Applications employing the standard external resistor LTC2941 with an external 50mΩ sense resistor may be upgraded to the pin compatible LTC2941-1 by removing the external sense resistor.

Voltage Drop Between SENSE+ and SENSE–

The LTC2941-1 is trimmed for an effective internal resistance of 50mΩ , but the total pin-to-pin resistance (R_{PP}), consisting of the sense resistor in series with pin and bond wire resistances, is somewhat higher. Assuming a sense resistor temperature coefficient of about 3900ppm/K, the total resistance between SENSE+ and SENSE– at a temperature, T, is typically:

$$R_{PP}(T) = R_{PP}(T_{NOM})\ [1 + 0.0039(T - T_{NOM})]$$

where T_{NOM} = 27°C (or 300K) and $R_{PP}(T_{NOM})$ is from the Electrical Characteristics table. This means that the resistance between SENSE+ and SENSE– may drop by 26% if die temperature changes from 27°C to –40°C or increase by 23% for a 27°C to 85°C die temperature change. Ensure that total voltage drop between SENSE+ and SENSE–, caused by maximum peak current flowing in/out of SENSE– :

$$V_{DROP} = I_{PEAK} \bullet R_{PP}(T_{DIE(MAX)})$$

does not exceed the application's requirements .

Limiting Inrush Current

Inrush currents during events like battery insertion or closure of a mechanical power switch may be substantially higher than peak currents during normal operation. Extremely large inrush currents may require additional circuitry to keep currents through the LTC2941-1 sense resistor below the absolute maximum ratings.

Note that external Schottky clamp diodes between SENSE+ and SENSE– can leak significantly, especially at high temperature, which can cause significant coulomb counter errors. Preferred solutions to limit inrush current include active Hot Swap™ current limiting or connector designs that include current limiting resistance and staggered pins to ensure a low impedance connection when the connector is fully mated.

Power Dissipation

Power dissipation in the R_{PP} resistance when operated at high currents can increase the die temperature several degrees over ambient. Soldering the exposed pad of the DFN package to a large copper region on the PCB is recommended for applications operating close to the specified maximum current and ambient temperature. Die temperature at a given I_{SENSE} can be estimated by:

$$T_{DIE} = T_{AMB} + 1.22 \bullet \theta_{JA} \bullet R_{PP(MAX)} \bullet I_{SENSE}^2$$

*Patent pending.

APPLICATIONS INFORMATION

where the factor 1.22 approximates the effect of sense resistor self-heating, $R_{PP(MAX)}$ is the maximum pad-to-pad resistance at nominal temperature (27°C) and θ_{JA} is the thermal resistance from junction to ambient. The θ_{JA} data given for the DFN package is valid for typical PCB layouts; more precise θ_{JA} data for a particular PCB layout may be obtained by measuring the voltage V_{P-P} between $SENSE^+$ and $SENSE^-$, the ambient temperature T_{AMB}, and the die temperature T_{DIE}, and calculating:

$$\theta_{JA} = \frac{T_{DIE} - T_{AMB}}{V_{P-P} \bullet I_{SENSE}}$$

For evaluation of printed circuit board layouts during development, both T_{AMB} and T_{DIE} temperature may be measured using a pin compatible LTC2942-1 internal temperature sensor. I_{SENSE} should be set to zero to measure T_{AMB}, and high enough during T_{DIE} measurement to achieve a significant temperature increase over T_{AMB}.

Measuring Current

In some applications, it may be desirable to measure the current I_{SENSE} flowing through the internal sense resistor. Since charge measured by the coulomb counter is the time integral over I_{SENSE}, differentiation of the contents of the accumulated charge register (ACR) over time may be used to measure average current.

Accuracy of such an indirect current measurement is limited by the basic accuracy of the coulomb counter, the accuracy of the timebase within the host system, quantization caused by the prescaler setting, and time delays caused by I^2C transactions. Still, especially at higher currents, useful results may be obtained by reading the accumulated charge register twice, with a defined time interval in between, and dividing the charge difference by the time interval. The time interval may be increased at low currents to limit time quantization errors to the desired accuracy. For quicker current measurement at low currents, prescale factor M may be temporarily decreased, sacrificing some coulomb count accuracy for higher current resolution.

Extending Coulomb Counter Range

To increase the range of the coulomb counter for battery capacities higher than 5.5Ah, the host controller can either regularly poll the accumulated charge register (ACR) or use the threshold registers to determine when the accumulated charge register approaches the minimum or maximum limits. At this point it can add or subtract a fixed charge quantity and rewrite the result into the ACR. The added or subtracted charge quantities can then be tracked in software, increasing the effective ACR range.

PC Board Layout Recommendations

Keep all traces as short as possible to minimize noise and inaccuracy. Use wider traces from the resistor to the battery, load and/or charger (see Figure 10). Put the bypass capacitor close to $SENSE^+$ and GND. Provide adequate copper area on exposed pad for heat sinking.

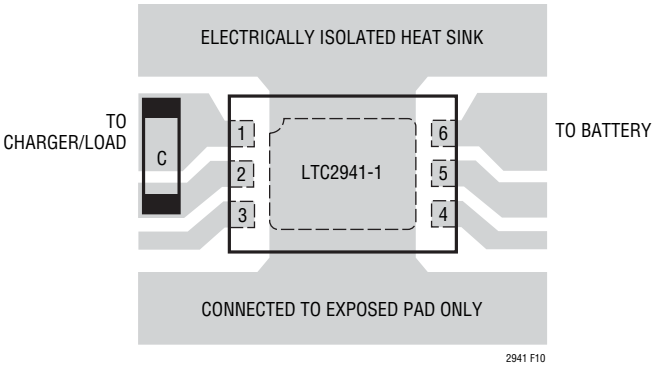
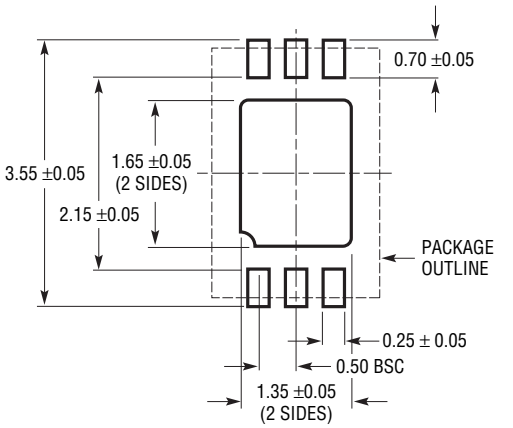


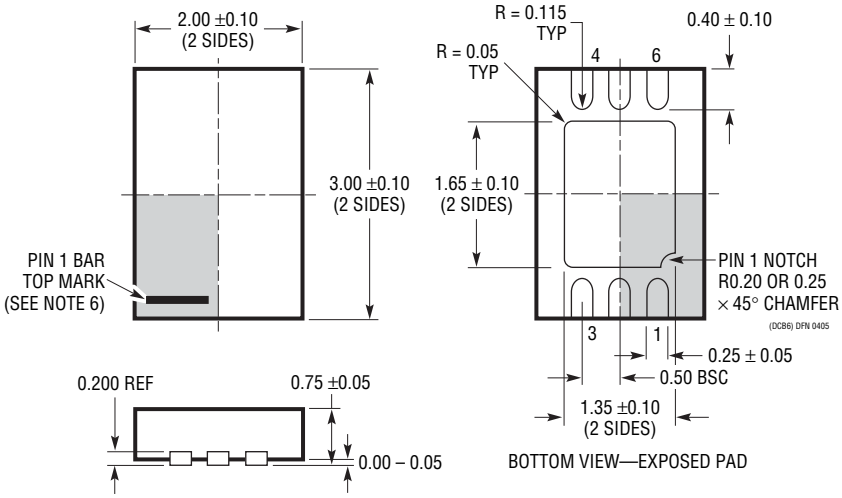
Figure 10. Recommended Layout

PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

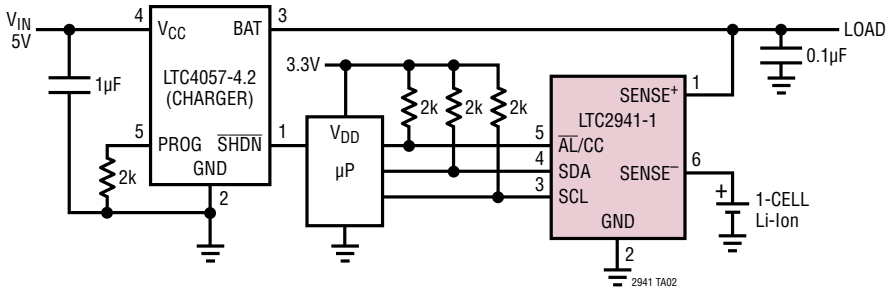


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Single Cell Lithium-Ion Coulomb Counter with Battery Charger for Discharge Currents of up to 1A



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Battery Gas Gauges		
LTC2941	Battery Gas Gauge with I²C Interface	Pin Compatible with LTC2942
LTC2942	Battery Gas Gauge with I²C Interface, Voltage and Temperature Measurement	14-Bit ΔΣ ADC, Pin Compatible with LTC2941
LTC2942-1	Battery Gas Gauge with I²C Interface and Voltage and Temperature ADC; Integrated 50mΩ Sense Resistor	14-Bit ΔΣ ADC, Pin Compatible with LTC2941-1
LTC4150	Coulomb Counter/Battery Gas Gauge	2.7V to 8.5V Operation, 10-Pin MSOP Package
Battery Chargers		
LTC1734	Lithium-Ion Battery Charger in ThinSOT™	Simple ThinSOT Charger, No Blocking Diode, No Sense Resistor Needed
LTC4002	Switch Mode Lithium-Ion Battery Charger	Standalone, 4.7V ≤ V_{IN} ≤ 24V, 500kHz Frequency
LTC4052	Monolithic Lithium-Ion Battery Pulse Charger	No Blocking Diode or External Power FET Required, ≤1.5A Charge Current
LTC4053	USB Compatible Monolithic Li-Ion Battery Charger	Standalone Charger with Programmable Timer, Up to 1.25A Charge Current
LTC4057	Lithium-Ion Linear Battery Charger	Up to 800mA Charge Current, Thermal Regulation, ThinSOT Package
LTC4058	Standalone 950mA Lithium-Ion Charger in DFN	C/10 Charge Termination, Battery Kelvin Sensing, ±7% Charge Accuracy
LTC4059	900mA Linear Lithium-Ion Battery Charger	2mm × 2mm DFN Package, Thermal Regulation, Charge Current Monitor Output
LTC4061	Standalone Linear Li-Ion Battery Charger with Thermistor Input	4.2V, ±0.35% Float Voltage, Up to 1A Charge Current, 3mm × 3mm DFN Package
LTC4063	Li-Ion Charger with Linear Regulator	Up to 1A Charge Current, 100mA, 125mV LDO, 3mm × 3mm DFN Package
LTC4080	500mA Standalone Li-Ion Charger with Integrated 300mA Synchronous Buck	3mm × 3mm DFN Package, Low External Component Count, Especially Suitable for Portable Applications
LTC4088	High Efficiency Battery Charger/USB Power Manager	Maximizes Available Power from USB Port, Bat-Track™, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, 4mm × 3mm DFN-14 Package

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