Features (continued)

- Configurable through MII serial management port or via external control pins
- Programmable LED outputs for link, activity, full/half duplex, collision and speed
- On-chip built-in analog front end filtering for both 100BASE-TX and 10BASE-T
- Supports back-to-back, 100BASE-FX to 100BASE-TX for media converter applications
- Single 3.3V power supply with built-in 1.8V regulator ('L' parts)
- 48 Pin LQFP, 48 Pin SSOP

Ordering Information

Part Number	Integrated LDO	Temperature Range	Package	Lead Finish
KS8001L	Yes	0°-70°C	48-LQFP	Standard
KS8001S	No	0°–70°C	48-SSOP	Standard
KSZ8001L	Yes	0°–70°C	48-LQFP	Lead-free
KSZ8001LI	Yes	-40°–85°C	48-LQFP	Lead-free
KSZ8001S	No	0°–70°C	48-SSOP	Lead-free
KSZ8001SI	No	-40°–85°C	48-SSOP	Lead-free

Revision History

Revision	Date	Summary of Changes
PRELIMINARY	25 Mar 2004	• Preliminary data
0.8	9 Aug 2004	• Updated pin 38 (VDDRCV) definition to 3.3V • Corrected pin configuration diagrams to reflect NC on pins 42 and 43 • Updated crystal tolerance to +/- 50 ppm
0.81	17 Sep 2004	• Updated series resistance for crystal specification to 40 Ω
0.82	25 Jan 2005	• LinkMD distance coefficient changed to 0.39 • Interrupt register status bits set to RO/SC • Recommended reset circuit added • RMII timing added
1.00	31 Mar 2005	• Added lead-free part numbers
1.01	16 May 2005	• Changed REXT value to 6.65 KΩ • Removed preliminary status • Added KSZ8001S to ordering information
1.02	30 Jan 2006	• Updated part ordering information • Corrected recommended reset circuits to match corresponding description • Added Micrel disclaimer to last page • Corrected crystal/oscillator PPM in Reference Clock Connection Diagrams • Added current consumption for KSZ8001L • Correct RXC clock pulse width timing in 100BASE-TX MII Receive Timing Diagram • Added description for Auto MDI/MDI-X mode in register 1f.15 • Updated description for MDI/MDI-X select in register 1f.14 • Corrected Auto-Negotiation Complete bit, register 1f.7, to read only • Added “Circuit Design Reference for Power Supply” section • Updated Pin Description for the following pins: MDIO, VDDIO, VDDC, RX+, RX-, TX+, TX-, XI, XO
1.03	7 March 2006	• Removed 48 Pin QFN (targeted) package option • Renamed KS8001 to KSZ8001 throughout datasheet • Added mechanical info for SSOP package • Updated package thermal resistance
1.04	25 June 2009	• Update ordering information.

Table of Contents

Pin Description

Pin Number	Pin Name	Type (Note 1)	Pin Function
1	MDIO	I/O	MII Management (MIIM) Interface: Data I/O This pin requires an external 4.7K pull-up resistor.
2	MDC	I	MII Management (MIIM) Interface: Clock Input This pin is synchronous to the MDIO data line.
3	RXD3/ PHYAD1	Ipd/O	MII Mode: Receive Data Output[3][2] / Configuration Mode: The pull-up/pull-down value is latched as PHYADDR[1] during reset. See “Strapping Options” section for details.
4	RXD2/ PHYAD2	Ipd/O	MII Mode: MII Receive Data Output[2][2] / Configuration Mode: The pull-up/pull-down value is latched as PHYADDR[2] during reset. See “Strapping Options” section for details.
5	RXD1/ RXD[1]/ PHYAD3	Ipd/O	MII Mode: Receive Data Output[1][2] / RMII Mode: Receive Data Output[1][3] / Configuration Mode: The pull-up/pull-down value is latched as PHYADDR[3] during reset. See “Strapping Options” section for details.
6	RXD0/ RXD[0]/ RX PHYAD4	Ipd/O	MII Mode: Receive Data Output[0][2] / RMII Mode: Receive Data Output[0][3] / SMII Mode: Receive Data and Control[4] / Configuration Mode: The pull-up/pull-down value is latched as PHYADDR[4] during reset. See “Strapping Options” section for details.
7	VDDIO	Pwr	3.3V digital VDD
8	GND	Gnd	Ground
9	RXDV/ CRSDV/ PCS_LPBK	Ipd/O	MII Mode: Receive Data Valid Output / RMII Mode: Carrier Sense/Receive Data Valid / Configuration Mode: The pull-up/pull-down value is latched as pcs_lpbk during reset. See “Strapping Options” section for details.
10	RXC/ SMII_SELECT	Ipd/O	MII Receive Clock Output Operating at: 25 MHz = 100 Mbps 2.5 MHz = 10 Mbps Configuration Mode: The pull-up/pull-down value is latched as SMII during reset. See “Strapping Options” section for details.
11	RXER/ RX_ER/ ISO	Ipd/O	MII Mode: Receive Error Output / RMII Mode: Receive Error / Configuration Mode: The pull-up/pull-down value is latched as ISOLATE during reset. See “Strapping Options” section for details.
12	GND	Gnd	Ground
13	VDDC	Pwr	1.8V digital core VDD VDD output : KSZ8001L / KSZ8001SL VDD input : KSZ8001S (See “Circuit Design Reference for Power Supply” section for details)
14	TXER	Ipd	MII Transmit Error Input
15	TXC/ REFCLK/ CLOCK	I/O	MII Mode: MII Transmit Clock Output / RMII Mode: 50 MHz Reference Clock Input / SMII Mode: 125 MHz Synchronization Clock Input
16	TXEN	Ipd	MII Transmit Enable Input

Pin Number	Pin Name	Type (Note 1)	Pin Function
17	TXD0/ TXD[0]/ TX	Ipd	MII Mode: Transmit Data Input[0] / RMII Mode: Transmit Data Input[0] / SMII Mode: Transmit Data and Control
18	TXD1/ TXD[1]/ SYNC	Ipd	MII Mode: Transmit Data Input[1] / RMII Mode: Transmit Data Input[1] / SMII Mode: SYNC
19	TXD2	Ipd	MII Transmit Data Input[2]
20	TXD3	Ipd	MII Transmit Data Input[3]
21	COL / RMII_SELECT	Ipd/O	MII Collision Detect Output Configuration Mode: The pull-up/pull-down value is latched as RMII select during reset. See “Strapping Options” section for details.
22	CRS/ RMII_BTB	Ipd/O	MII Carrier Sense Output Configuration Mode: The pull-up/pull-down value is latched as RMII Loop-back during reset when RMII mode is selected. See “Strapping Options section” for details.
23	GND	Gnd	Ground
24	VDDIO	Pwr	3.3V digital VDD
25	INT#/ PHYAD0	Ipu/O	Management Interface (MII) Interrupt Out. Configuration Mode: Latched as PHYAD[0] during power up / reset. See “Strapping Options” section for details.
26	LED0/ TEST	Ipu/O	Programmable LED Output 0 Configuration Mode: The external pull down enable test mode and only used for tfactory test. Active Low. The LED0 pin is also programmable via register 1eh.
			LED mode = 00
			Link/Act / Pin State / LED Definition
			No Link / H / Off
			Link / L / On
			Activity / - / Toggle
			LED mode = 01
			Link / Pin State / LED Definition
			No Link / H / Off
			Link / L / On
			LED mode = 10
			10Mbps Link / Pin State / LED Definition
			No Link / H / Off
			Link / L / On
27	LED1 / SPD100/ noFEF	Ipu/O	Programmable LED Output 1 Configuration Mode: Latched as SPEED (Register 0, bit 13) during power up / reset. See “Strapping Options” Section for details. Active Low. The LED1 pin is also programmable via register 1eh.
			LED mode = 00
			Speed / Pin State / LED Definition
			10BT / H / Off
			100BT / L / On

Pin Number	Pin Name	Type (Note 1)	Pin Function		
			LED mode = 01		
			Speed	Pin State	LED Definition
			10BT	H	Off
			100BT	L	On
			LED mode = 10		
			100Mbps Link	Pin State	LED Definition
			No Link	H	Off
			Link	L	On
28	LED2/ DUPLEX	Ipu/O	Programmable LED Output 2 Configuration Mode: Latched as DUPLEX (register 0h, bit 8) during power up / reset. See "Strapping Options" Section for details. Active Low. The LED2 pin is also programmable via register 1eh.		
			LED mode = 00		
			Duplex	Pin State	LED Definition
			Half	H	Off
			Full	L	On
			LED mode = 01		
			Full Duplex/Col	Pin State	LED Definition
			Half	H	Off
			Full	L	On
			Collision	-	Toggle
			LED mode = 10		
			Duplex	Pin State	LED Definition
			Half	H	Off
			Full	L	On
29	LED3/ NWAYEN	Ipu/O	Programmable LED Output 3 Configuration Mode: Latched as ANEG_EN (register 0h, bit 12) during power up / reset. See "Strapping Options" Section for details. Active Low. The LED3 pin is also programmable via register 1eh.		
			LED mode = 00		
			Collision	Pin State	LED Definition
			No Collision	H	Off
			Collision	L	On
			LED mode = 01		
			Activity	Pin State	LED Definition
			Activity	-	Toggle
			LED mode = 10		
			Activity	Pin State	LED Definition
			Activity	-	Toggle
30	PD#	Ipu	Chip power down input (active low) 1 (high) = Normal operation 0 (low) = Power down		

Pin Number	Pin Name	Type (Note 1)	Pin Function
31	VDDRX	Pwr	1.8V analog VDD (See “Circuit Design Reference for Power Supply” section for details)
32	RX-	I/O	Physical receive or transmit ‘-’ differential signal
33	RX+	I/O	Physical receive or transmit ‘+’ differential signal
34	FXSD/ FXEN	Ipd/O	Fiber Mode Enable / Signal Detect in Fiber Mode If FXEN=0, FX mode is disable. The default is “0”. (See “100BASE-FX Mode” section for details)
35	GND	Gnd	Ground
36	GND	Gnd	Ground
37	REXT	I	Connect a 6.65KΩ external resistor from this pin to ground
38	VDDRCV	Pwr	3.3V analog VDD (See “Circuit Design Reference for Power Supply” section for details)
39	GND	Gnd	Ground
40	TX-	I/O	Physical transmit or receive ‘-’ differential signal
41	TX+	I/O	Physical transmit or receive ‘+’ differential signal
42	NC		No Connect
43	NC		No Connect
44	GND	Gnd	Ground
45	XO	O	25MHz crystal/oscillator clock connections
46	XI	I	Pins (XI, XO) connect to a crystal. If an oscillator is used, XI connects to a 3.3V tolerant oscillator and XO is a no connect. Clock is +/- 50ppm for both crystal and oscillator.
47	VDDPLL	Pwr	1.8V analog PLL VDD (See “Circuit Design Reference for Power Supply” section for details)
48	RST#	Ipu	Chip Reset Active low, minimum of 50 us pulse is required

Note 1:

Pwr = power supply;
Gnd = ground;
I = input;
O = output;
I/O = bi-directional
Ipu = input w/ internal pull up;
Ipd = input w/ internal pull down;
Ipu/O = input w/ internal pull up during reset, output pin otherwise;
Ipd/O = input w/ internal pull down during reset, output pin otherwise;
PD = strap pull down;
PU = strap pull up;

Note 2:

MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD [3..0] presents valid data to MAC through the MII. RXD [3..0] is invalid when RXDV is de-asserted.

Note 3:

RMII Rx Mode: The RXD[1..0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.

Note 4:

SMII Rx Mode: Receive data and control information are sent in 10 bit segments. In 100MBit mode, each segment represents a new byte of data. In 10MBit mode, each segment is repeated ten times; therefore, every ten segments represents a new byte of data. The MAC can sample any one of every 10 segments in 10MBit mode.

Note 5:
MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD [3..0] presents valid data from the MAC through the MII. TXD [3..0] has no effect when TXEN is de-asserted.

Note 6:
RMII Tx Mode: The TXD[1..0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of recovered data are recovered by the PHY.

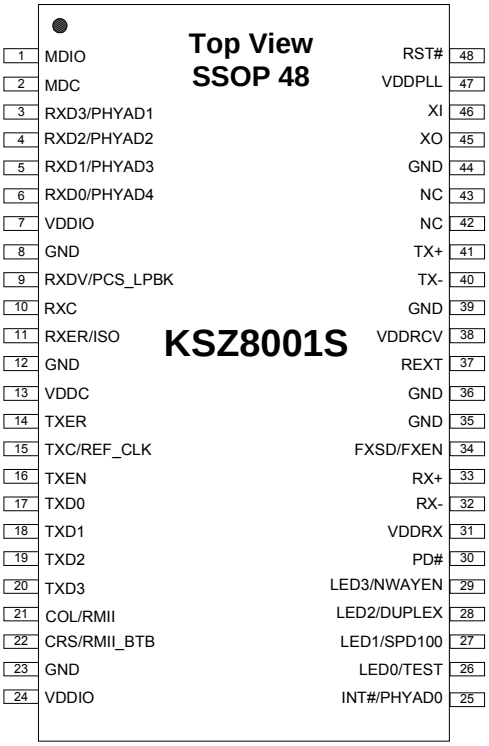
Note 7:
SMII Tx Mode: Transmit data and control information are received in 10 bit segments. In 100MBit mode, each segment represents a new byte of data. In 10MBit mode, each segment is repeated ten times; therefore, every ten segments represents a new byte of data. The PHY can sample any one of every 10 segments in 10MBit mode.

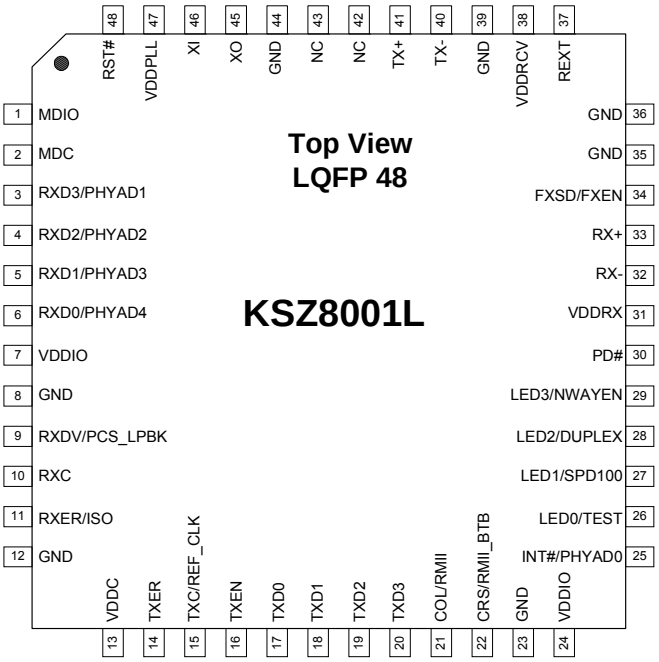
Strapping Options

Pin Number	Pin Name	Type (Note 2)	Description
6, 5, 4, 3	PHYAD[4:1] / RXD[0:3]	Ipd/O	PHY Address latched at power-up / reset. The default PHY address is 00001.
25	PHYAD0 / INT#	Ipu/O	
9	PCS_LPBK / RXDV	Ipd/O	Enables PCS_LPBK mode at power-up / reset. PD (default) = Disable, PU = Enable
10	SMII_SELECT / RXC	Ipd/O	Enables SMII mode at power-up / reset. PD (default) = Disable, PU = Enable
11	ISO / RXER	Ipd/O	Enables ISOLATE mode at power-up /reset. PD (default) = Disable, PU = Enable
21	RMII_SELECT / COL	Ipd/O	Enables RMII mode at power-up / reset. PD (default) = Disable, PU = Enable
22	RMII_BTB/ CRS	Ipd/O	Enable RMII_BTB mode at power-up / reset. PD (default) = Disable, PU = Enable
27	SPD100 / No FEF / LED1	Ipu/O	Latched into Register 0h bit 13 during power-up / reset. PD = 10Mb/s, PU (default) = 100Mb/s. If SPD100 is asserted during power-up / reset, this pin also latched as the Speed Support in register 4h. (If FXEN is pulled up, the latched value 0 means no Far _End _Fault.)
28	DUPLEX/ LED2	Ipu/O	Latched into Register 0h bit 8 during power-up / reset. PD = Half Duplex, PU (default) = Full duplex. If Duplex is pulled up during reset, this pin also latched as the Duplex support in register 4h.
29	NWAYEN/ LED3	Ipu/O	Nway (auto-=Negotiation) Enable Latched into Register 0h bit 12 during power-up / reset. PD = Disable Auto-Negotiation, PU (default) = Enable Auto-Negotiation
30	PD#	Ipu	Power Down Enable PU (default) = Normal operation, PD = Power down mode

Note: Strap-in is latched during power up or reset. In some systems, the MAC RXD pins may drive high at all times causing the PHY strap-in to be latched high during power up or system reset. In this case, it is recommended to use a strong pull down to GND via 1kohm resistor on RXDV, RXC, and RXER pins. Otherwise, the PHY may stay in Isolate or loop back modes.

Pin Configuration





Functional Description

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, NRZ to NRZI conversion, MLT-3 encoding and transmission. The circuitry starts with a parallel-to-serial conversion, which converts the 25 MHz, 4-bit nibbles into a 125 MHz serial bit stream. The incoming data is clocked in at the positive edge of the TXC signal. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 6.65 KΩ resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

100BASE-TX Receive

The 100BASE-TX receive function performs adaptive equalization, DC restoration, MLT-3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion are a function of the length of the cable, the equalizer has to adjust its characteristic to optimize performance. In this design, the variable equalizer will make an initial estimation based upon comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effects of base line wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. Finally, the NRZ serial data is converted to 4-bit parallel 4B nibbles. A synchronized 25 MHz RXC is generated so that the 4B nibbles is clocked out at the negative edge of RCK25 and is valid for the receiver at the positive edge. When no valid data is present, the clock recovery circuit is locked to the 25 MHz reference clock and both TXC and RXC clocks continue to run.

PLL Clock Synthesizer

The KSZ8001 generates 125 MHz, 25 MHz and 20 MHz clocks for system timing. An internal crystal oscillator circuit provides the reference clock for the synthesizer.

Scrambler/De-scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

10BASE-T Transmit

When TXEN (transmit enable) goes high, data encoding and transmission will begin. The KSZ8001 will continue to encode and transmit data as long as TXEN remains high. The data transmission will end when TXEN goes low. The last transition occurs at the boundary of the bit cell if the last bit is zero, or at the center of the bit cell if the last bit is one. The output driver is incorporated into the 100BASE- driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.5 V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the RX+ or RX- input from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8001 decodes a data frame. This activates the carrier sense (CRS) ad RXDV signals and makes the receive data (RXD) available. The receive clock is maintained active during idle periods in between data reception.

SQE and Jabber Function (10BASE-T only)

In 10BASE-T operation, a short pulse will be put out on the COL pin after each packet is transmitted. This is required as a test of the 10BASE-T transmit/receive path and is called SQE test. The 10BASE-T transmitter will be disabled and COL will go high if TXEN is High for more than 20 ms (Jabbering). If TXEN then goes low for more than 250 ms, the 10BASE-T transmitter will be re-enabled and COL will go Low.

Auto-Negotiation

The KSZ8001 performs auto-negotiation by hardware strapping option (pin 29) or software (Register 0.12). It will automatically choose its mode of operation by advertising its abilities and comparing them with those received from its link partner whenever auto-negotiation is enabled. It can also be configured to advertise 100BASE-TX or 10BASE-T in either full- or half-duplex mode. Auto-negotiation is disabled in FX mode.

During auto-negotiation, the contents of Register 4, coded in Fast Link Pulse (FLP), will be sent to its link partner under the conditions of power-on, link-loss or re-start. At the same time, the KSZ8001 will monitor incoming data to determine its mode of operation. Parallel detection circuit will be enabled as soon as either 10BASE-T NLP (Normal Link Pulse) or 100BASE-TX idle is detected. The operation mode is configured based on the following priority:

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

When the KSZ8001 receives a burst of FLP from its link partner with 3 identical link code words (ignoring acknowledge bit), it will store these code words in Register 5 and wait for the next 3 identical code words. Once the KSZ8001 detects the second code words, it then configures itself according to the above-mentioned priority. In addition, the KSZ8001 also checks for 100BASE-TX idle or 10BASE-T NLP symbols. If either is detected, the KSZ8001 automatically configures to match the detected operating speed.

MII Management Interface

The KSZ8001 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ8001. The MDIO interface consists of the following:

- A physical connection including a data line (MDIO), a clock line (MDC) and an optional interrupt line (INTRPT)
- A specific protocol that runs across the above-mentioned physical connection and it also allows one controller to communicate with multiple KSZ8001 devices. Each KSZ8001 is assigned an MII address between 0 and 31 by the PHYAD inputs.
- An internal addressable set of fourteen 16-bit MDIO registers. Register [0:6] are required and their functions are specified by the IEEE 802.3 specifications. Additional registers are provided for expanded functionality.

The INTPRT pin functions as a management data interrupt in the MII. An active Low or High in this pin indicates a status change on the KSZ8001 based upon 1fh.9 level control. Register bits at 1bh[15:8] are the interrupt enable bits. Register bits at 1bh[7:0] are the interrupt condition bits. This interrupt is cleared by reading Register 1bh.

MII Data Interface

The data interface consists of separate channels for transmitting data from a 10/100 802.3 compliant Media Access Controller (MAC) to the KSZ8001, and for receiving data from the line. Normal data transmission is implemented in 4B Nibble Mode (4-bit wide nibbles).

Transmit Clock (TXC): The transmit clock is normally generated by the KSZ8001 from an external 25MHz reference source at the X1 input. The transmit data and control signals must always be synchronized to the TXC by the MAC. The KSZ8001 normally samples these signals on the rising edge of the TXC.

Receive Clock (RXC): For 100BASE-TX links, the receive clock is continuously recovered from the line. If the link goes down, and auto-negotiation is disabled, the receive clock then operates off the master input clock (X1 or TXC). For 10BASE-T links, the receive clock is recovered from the line while carrier is active, and operates from the master input clock when the line is idle. The KSZ8001 synchronizes the receive data and control signals on the falling edge of RXC in order to stabilize the signals at the rising edge of the clock with 10ns setup and hold times.

Transmit Enable: The MAC must assert TXEN at the same time as the first nibble of the preamble, and de-assert TXEN after the last bit of the packet.

Receive Data Valid: The KSZ8001 asserts RXDV when it receives a valid packet. Line operating speed and MII mode will determine timing changes in the following way:

- For 100BASE-TX link with the MII in 4B mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. RXDV is asserted with the first nibble of the SFD " 5D" and remains asserted until the end of the packet.

Error Signals: Whenever the KSZ8001 receives an error symbol from the network, it asserts RXER and drives "1110" (4B) on the RXD pins. When the MAC asserts TXER, the KSZ8001 will drive "H" symbols (a Transmit Error define in the IEEE 802.3 4B/5B code group) out on the line to force signaling errors.

Carrier Sense (CRS): For 100TX links, a start-of-stream delimiter, or /J/K symbol pair causes assertion of Carrier Sense (CRS). An end-of-stream delimiter, or /T/R symbol pair causes de-assertion of CRS. The PMA layer will also de-assert CRS if IDLE symbols are received without /T/R, yet in this case RXER will be asserted for one clock cycle when CRS is de-asserted. For 10T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an end-of-frame (EOF) marker.

Collision: Whenever the line state is half-duplex and the transmitter and receiver are active at the same time, then the KSZ8001 asserts its collision signal, which is asynchronous to any clock.

RMII (Reduced MII) Data Interface

RMII interface specifies a low pin count (Reduced) Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch or Repeater ASICs. It is fully compliant with IEEE 802.3u [2].

This interface has the following characteristics:

- It is capable of supporting 10Mb/s and 100Mb/s data rates
- A single clock reference is sourced from the MAC to PHY (or from an external source)
- It provides independent 2 bit wide (di-bit) transmit and receive data paths
- It uses TTL signal levels, compatible with common digital CMOS ASIC processes

RMII Signal Definition

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN	Input	Output	Transit Enable
TXD[1:0]	Input	Output	Transit Data
RX_ER	Output	Input (Not Required)	Receive Error

Note: Unused MII signals, TXD[3:2], TXER need to be tied to GND when RMII is used

Reference Clock (REF_CLK)

REF_CLK is a continuous 50 MHz clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. REF_CLK is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device. Each PHY device shall have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected carrier is said to be detected.

Loss of carrier shall result in the de-assertion of CRS_DV synchronous to REF_CLK. So long as carrier criteria are being met, CRS_DV shall remain asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit and shall be negated prior to the first REF_CLK that follows the final di-bit.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be "00" until proper receive signal decoding takes place (see definition of RXD[1:0] behavior).

Receive Data [1:0] (RXD[1:0])

RXD[1:0] shall transition synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g. before data recovery or during error conditions) a pre-determined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] shall be "00" to indicate idle when CRS_DV is de-asserted. Values of RXD[1:0] other than "00" when CRS_DV is de-asserted are reserved for out-of-band signaling (to be defined). Values other than "00" on RXD[1:0] while CRS_DV is de-asserted shall be ignored by the MAC/repeater. Upon assertion of CRS_DV, the PHY shall ensure that RXD[1:0]=00 until proper receive decoding takes place.

Transmit Enable (TX_EN)

Transmit Enable TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] on the RMII for trans-mission. TX_EN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented to the RMII. TX_EN shall be negated prior to the first REF_CLK following the final di-bit of a frame. TX_EN shall transition synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

Transmit Data TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] shall be "00" to indicate idle when TX_EN is de-asserted. Values of TXD[1:0] other than "00" when TX_EN is de-asserted are reserved for out-of-band signaling (to be defined). Values other than "00" on TXD[1:0] while TX_EN is disserted shall be ignored by the PHY.

Collision Detection

Since the definition of CRS_DV and TX_EN both contain an accurate indication of the start of frame, the MAC can reliably regenerate the COL signal of the MII by Ending TX_EN and CRS_DV.

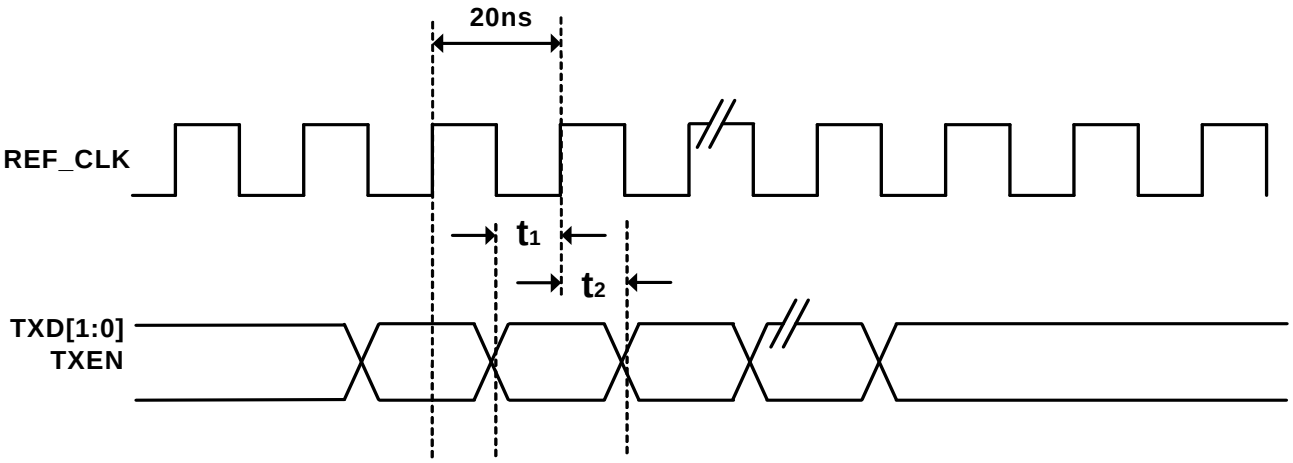
During the IPG time following the successful transmission of a frame, the COL signal is asserted by some transceivers as a self-test. The Signal Quality Error (SQE) function will not be supported by the reduced MII due to the lack of the COL signal. Historically, SQE was present to indicate that a transceiver located physically remote from the MAC was functioning. Since the reduced MII only supports chip-to-chip connections on a PCB, SQE functionality is not required.

RX_ER

The PHY shall provide RX_ER as an output according to the rules specified in IEEE 802.3u [2] (see Clause 24, Figure 24-11 - Receive State Diagram). RX_ER shall be asserted for one or more REF_CLK periods to indicate that an error (e.g. a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY. RX_ER shall transition synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER shall have no effect on the MAC.

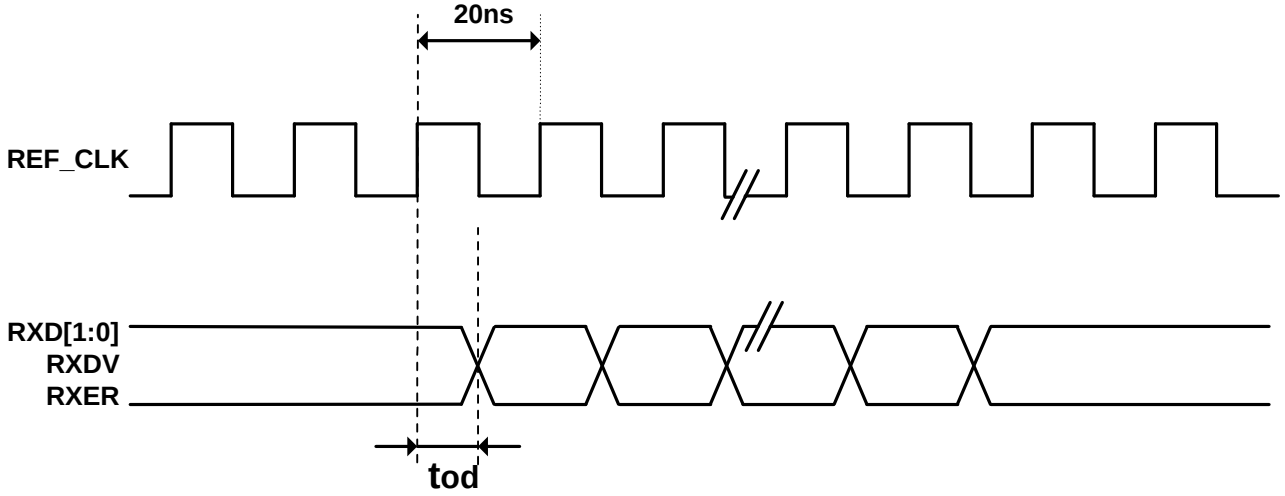
RMII AC Characteristics

RMII Transmit Timing



Parameter	Min	Typ	Max	Unit
REF_CLK Frequency		50		MHz
TXD[1:0], TX_EN, Data Setup to REF_CLK rising edge	4			ns
TXD[1:0], TX_EN, Data hold from REF_CLK rising edge	2			ns

RMII Receive Timing



Parameter	Min	Typ	Max	Unit
REF_CLK Frequency		50		MHz
RXD[1:0], CRS_DV, RX_ER Output delay from REF_CLK rising edge	2.8		10	ns

SMII Signal Definition

SMII is composed of two signals per port, a global synchronization signal, and a global 125MHz reference clock. All signals are synchronous to the clock. All SMII I/F uses a common 125MHz reference clock and SYNC signals that are synchronous to the reference clock. There are two signals in SMII from MAC-to-PHY for each port (TXD and TxSYNC), and one signal per port from PHY-to-MAC (RXD).

The Serial Media Independent Interface (SMII) is designed to satisfy the following requirements:

- Convey complete MII information between a 10/100 PHY and MAC with two pins per port.
- Allow a multi-port MAC/PHY communication with one system clock.
- Operate in both half and full duplex.
- Per packet switching between 10Mbit and 100Mbit data rates.
- Allow direct MAC-to-MAC communication.

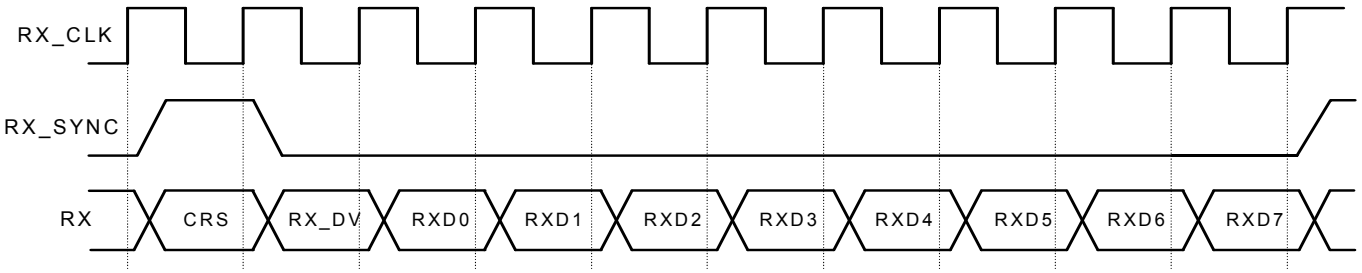
SMII Signals

Signal Name	From	To	Use
RX	PHY	MAC	Receive Data and Control
TX	MAC	PHY	Transmit Data and Control
SYNC	MAC	PHY	Synchronization
Clock	System	MAC&PHY	Synchronization

Receive Path

Receive data and control information are signaled in ten bit segments. In 100Mbit mode, each segment represents a new byte of data. In 10Mbit mode, each segment is repeated ten times; therefore, every ten segments represent a new byte of data. The MAC can simply any one of every 10 segment ion 10Mbit mode.
Segment boundaries are delimited by SYNC. The MAC continuously generates a pulse on SYNC every 10 clocks.

Receive Sequence Diagram



RX contains all of the information found on the receive path of the standard MII.

Bits	Purpose
CRS	Carrier Sense – identical to MII, except that it is not an asynchronous signal
RX_DV	Receive Data Valid – identical to MII
RXD7-0	Encoded Data, see the RXD0-7 Encoding table

RX – Bit Description

RXD7-0 are used to convey packet data, RX_ER, and PHY status. The MAC can infer the meaning of RXD on a segment-by-basis by encoding the two control bits.

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	0	RX_ER from previous frame	Speed 0=10Mbit 1=100Mbit	Duplex 0=Half 1=Full	Link 0=Down 1=Up	Jabber 0=OK 1=Error	Upper Nibble 0=invalid 1=valid	False Carrier Detected	1
X	1	One Data Byte (Two MII Data Nibble)							

TXD7 – 0 Encoding

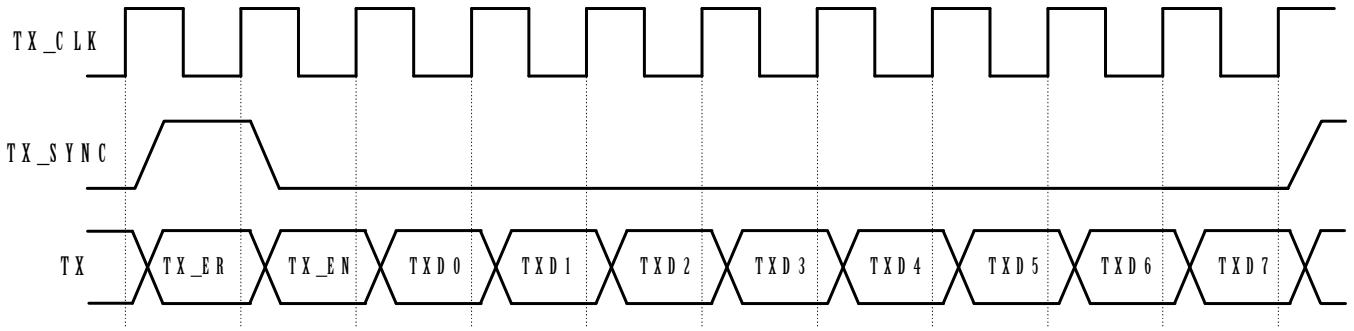
Inter-frame status bit RXD5 conveys the validity of the upper nibble of the byte of the previous frame. Inter-frame status bit RXD0 indicates whether or not the PHY detected an error somewhere on the previous frame. Both of these bits should be valid in the segment immediately following a frame, and should stay valid until the first data segment of the next frame begins.
When asserted, inter-frame status bit RXD6 indicates that the PHY has detected a false carrier event.
In order to send receive data to the MAC synchronous to the reference clock, the PHY must pass the data through an elasticity FIFO to handle any difference between the reference clock rate and the clock at the packet source. The Ethernet specification calls for packet data to be referenced to a clock with a frequency tolerance of 100ppm (0.01%); however, it is not uncommon to encounter Ethernet stations with clocks that have frequency errors up to 0.1%. Therefore, the elasticity FIFO should be at least 27 bits * long, filling to the halfway point before beginning valid data transfer via RX. RX_ER should be asserted if, during the reception of a frame, this FIFO overflows or underflows.

Only RXD and RX_DV should be passed through the elasticity FIFO. CRS should not be passed through the elasticity FIFO. Instead, CRS should be asserted for the time the ‘wire’ is busy receiving a frame.

Transmit Path

Transmit data and control information are signaled in ten bit segments, just like the receive path. In 100Mbit mode, each segment represents anew byte of data. In 10Mbit mode each segment is repeated ten times; therefore, every ten segments represents a new byte of data. The PHY can sample any one of every 10 segments in 10Mbit mode.
Segment boundaries are delimited by SYNC. The MAC continuously generates a pulse on SYNC every 10 clocks.

Transmit Sequence Diagram



Bits	Purpose
TX_EN	Transmit Enable – identical to MII
TX_ER	Transmit Error – identical to MII
TXD7-0	Encoded Data – see TXD7-0 Encoding Table

TX- Bit Description

As far as the PHY is concerned, TXD7-0 are used to convey only packet data. To allow for a direct MAC-to-MAC connection, the MAC uses TXD7-0 to signal 'status' in between frames.

TX_ER	TX_EN	TXD0	TXD1	TXD2	TXD3	TXD4	TXD7-5
x	0	Use to force an error in a direct MAC to MAC connection	1 100MBit	1 Full Duplex	1 Link Up	0 No Jabber	1
x	1	One Data Byte (Two MII Data Nibbles)					

TXD7 – 0 Encoding

Collision Detection

Collisions occur when CRS and TX_EN are simultaneously asserted. For this to work, the PHY must ensure that CRS is not affected by its transmit path.

DC Specification

Parameter	Symbol	Min	Max	Units
Input High Voltage	Vih	2.0		Volts
Input Low Voltage	Vil		0.8	Volts
Input High Current	Iih	-10	10	uA
Input Low Current	Iil	-10	10	uA

Timing Specification

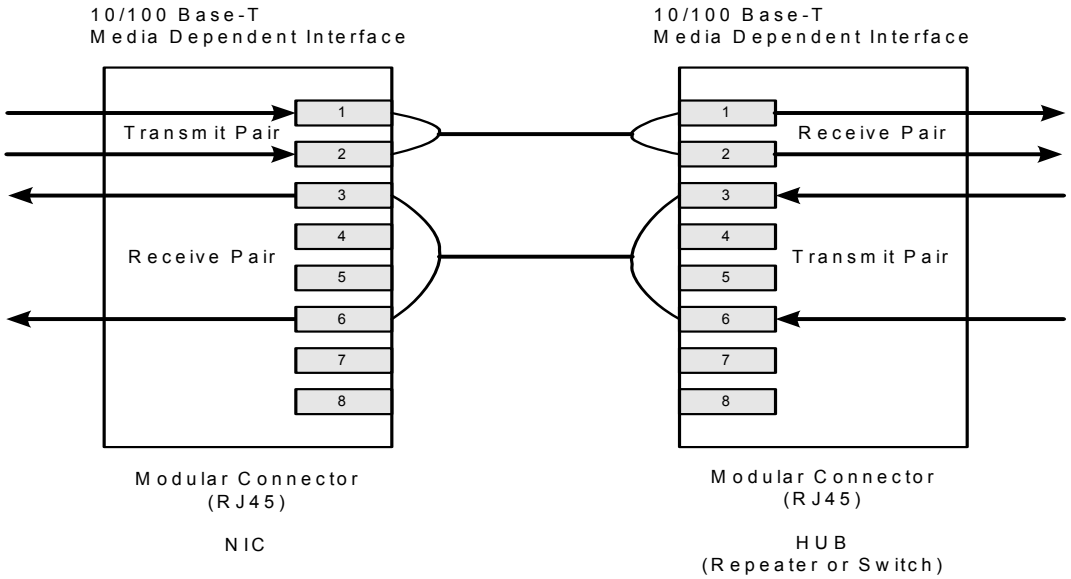
Parameter	Min	Max	Units
Input Setup	1.5		ns
Input Hold	1		ns
Output Delay	1.5	5	ns

HP Auto Crossover (Auto MDI/MDI-X)

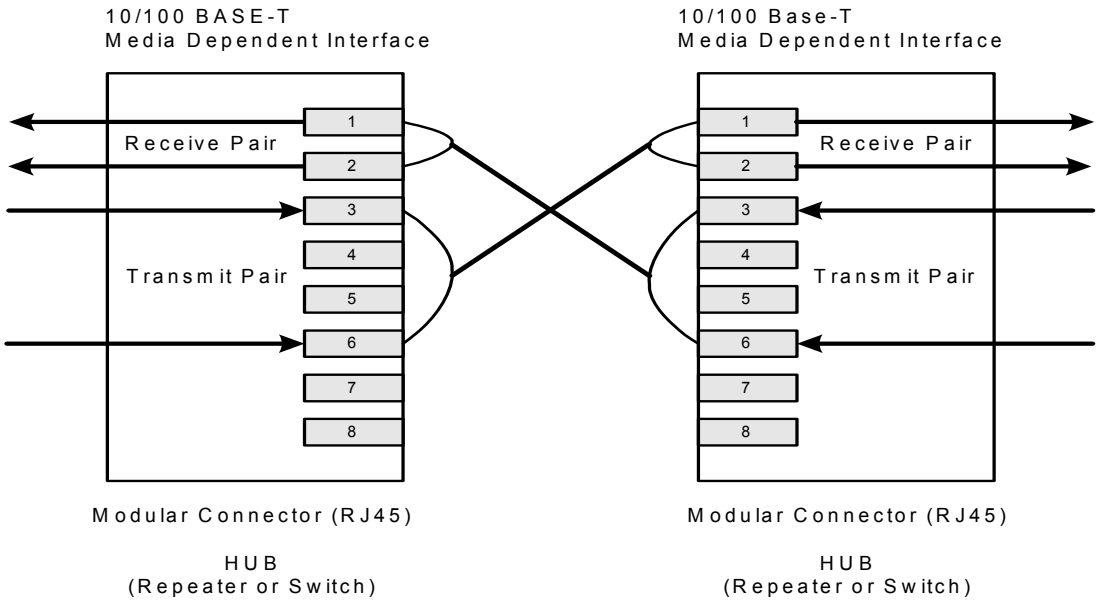
Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. The assignment of pin-outs for a 10/100 BASE-T crossover function cable is shown below.

This feature can eliminate the confusion in real applications by allowing both straight cable and crossover cables. This feature is controlled by register 1f:13, see “Register 1fh” section for details.

Straight Through Cable



Crossover Cable



Auto MDI/MDI-X Cross-Over Transformer Connection

KSZ8001 features HP Auto MDI/MDI-X crossover and requires symmetric transformers that support Auto MDI/MDI-X. See "Selection of Isolation Transformer" for a list of transformers that support Auto MDI/MDI-X.

Power Management

The KSZ8001 offers the following modes for power management:

- *Power Down Mode:* This mode can be achieved by writing to Register 0.11 or pulling pin 30 PD# Low. In the power down state, the KS8061 disables all internal functions and drives output pins to logic zero, except for the MII serial management interface.
- *Power Saving Mode:* writing to register 1fh.10 can disable this mode. The KSZ8001 will then turn off everything except for the Energy Detect and PLL circuits when the cable is not installed. In other words, the KSZ8001 will shutdown most of the internal circuits to save power if there is no link. Power Saving mode will be in this most effective state when Auto-Negotiation Mode is enabled.

100BASE-FX Mode

100BASE-FX mode is activated when FXSD/FXEN is higher than 0.6V (This pin has a default pull down). Under this mode, the auto-negotiation and auto-MDIX features are disabled.

In fiber operation FXSD pin should connect to the SD (signal detect) output of the fiber module. The internal threshold of FXSD is around ⅔ Vdd +/- 50 mV (2.2V +/- 0.05V at 3.3V). Above this level, it is considered Fiber signal detected, and the operation is summarized in the following table:

FXSD/FXEN	Condition
Less than 0.6V	100TX mode
Less than 2.15V, but greater than 0.6V	FX mode No signal detected FEF generated
Greater than 2.25V	FX mode Signal detected

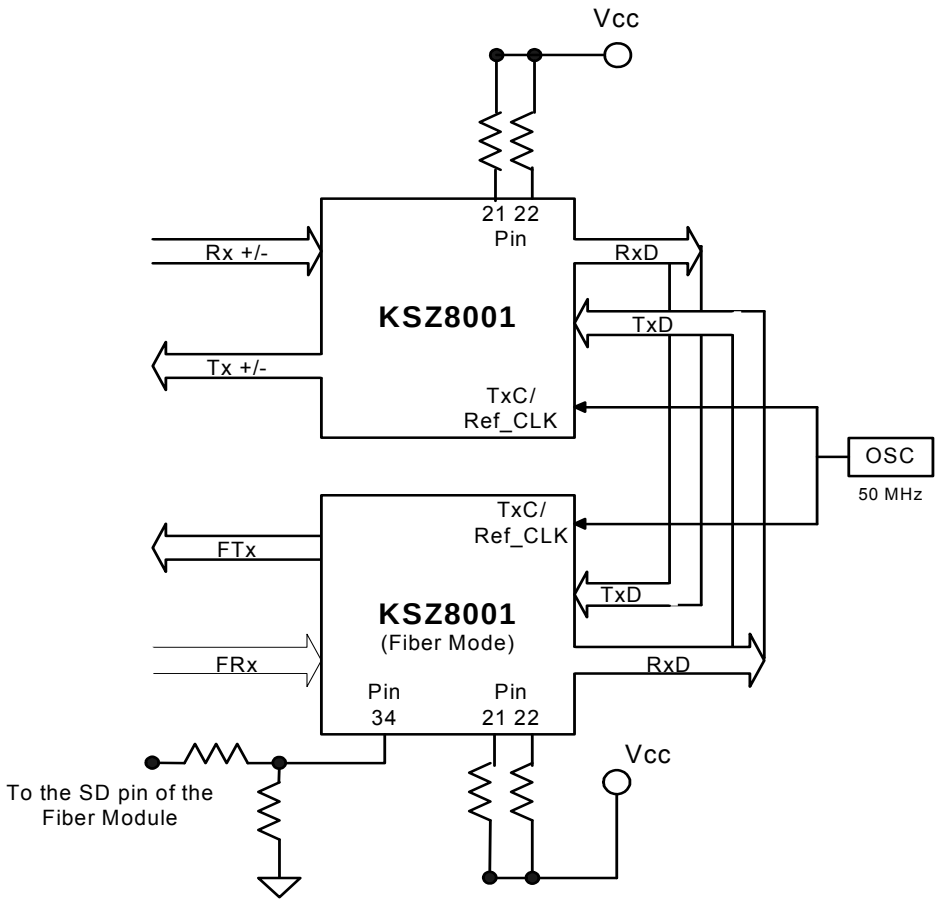
To ensure proper operation, the swing of fiber module SD should cover the threshold variation. A resistive voltage divider is recommended to adjust the SD voltage range.

FEF (Far End Fault), repetition of a special pattern, which consists of 84-ones and 1-zero, is generated under "FX mode with no signal detected". The purpose of FEF is to notify the sender of a faulty link. When receiving a FEF, the LINK will go down to indicate a fault, even with fiber signal detected. The transmitter is not affected by receiving a FEF and still sends out its normal transmit pattern from MAC. FEF can be disabled by strapping pin27 low, please refer to "Strapping Options" section.

Media Converter Operation

The KSZ8001 is capable of performing media conversion with 2 parts in a back-to-back RMII mode as indicated in the diagram. Both parts are in RMII mode and with RMII_BTB asserted (pin21 & 22 strapped high). One part is operating at TX mode and the other in FX mode. Both parts can share a common 50MHz oscillator.

Under this operation, auto-Negotiation on the TX side will prohibit 10BASE-T link up. Additional options can be implemented under this operation. Disable the transmitter and set it at tri-state by controlling the high TXD2 pin. In order to do this, RXD2 and TXD2 pins need to be connected via an inverter. When TXD2 pin is high in both the copper and fiber operation, it disables transmit. Meanwhile, the RXD2 pin on the copper side serves as the energy detect and can indicate if a line signal is detected. TXD3 should be tied low and RXD3 let float. Please contact your local Micrel FAE for a Media Converter reference design.



LinkMD Cable Diagnostics

The KSZ8001 utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits and impedance mismatches. LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDIX pairs and analyzing the shape of the reflected signal. Timing the duration gives an indication of the distance to the cabling fault with maximum distance of 200 m and accuracy of +/- 2 m. Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

LinkMD is used by accessing register 1dh, the LinkMD Control/Status register in conjunction with register 1fh, the 100BASE-TX PHY Controller register. To use LinkMD, HP Auto-MDIX is disabled by writing a '1' to 1f:13 to enable manual control over which pair is used to transmit the LinkMD pulse. The self-clearing Cable diagnostic test enable bit, 1d.15 is set to '1' to start the test on this pair. When 1d.15 returns to '0', the test is complete. The test result is returned in 1d.14:13 and the distance is returned in 1d.8:0. The cable diagnostic test results are as follows:

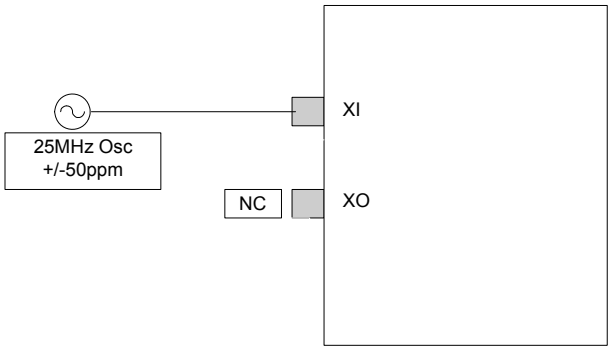
- 00 = Valid test, normal condition
- 01 = Valid test, open circuit in cable
- 10 = Valid test, short circuit in cable
- 11 = Invalid test, LinkMD failed

The '11' case, Invalid test, occurs when it is not possible for the KSZ8001 to shut down the link partner. In this case, the test is not run, since it would not be possible for the KSZ8001 to determine if the detected signal is a reflection of the signal generated or a signal from another source.

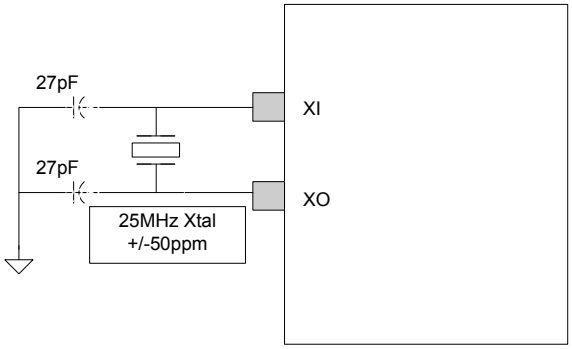
Cable length can be determined by multiplying the contents of 1d.8:0 by 0.39. This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

Reference Clock Connection Options

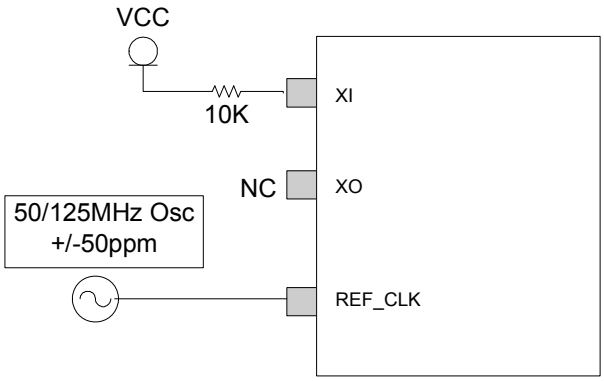
KSZ8001 is capable of performing three different kinds of clock speed options for connecting the external reference clock depends upon the different interface of using MII/RMII/SMII. The figures below illustrate the recommended connection for using the different interface options. Please see the selection of reference crystal table for specifications.



25MHz Oscillator Reference Clock Connection Diagram



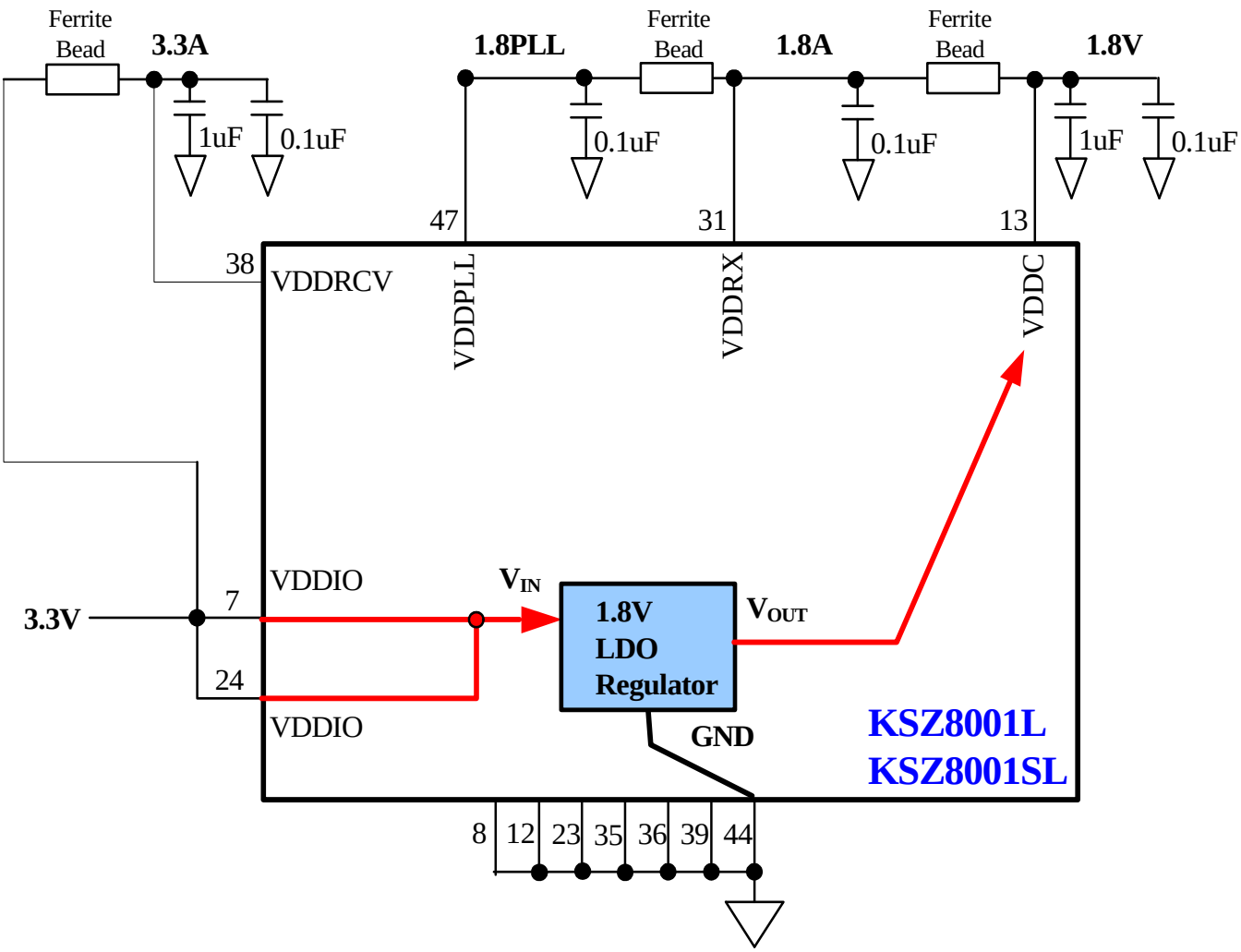
25MHz Crystal Reference Clock Connection Diagram



50/125 MHz Oscillator Reference Clock Connection for RMII/SMII Mode Diagram

Circuit Design Reference for Power Supply

The following diagram shows the power connections for the single 3.3V supply KSZ8001L and KSZ8001SL devices.



Register Map

Register No.	Description
0h	Basic Control Register
1h	Basic Status Register
2h	PHY Identifier I
3h	PHY Identifier II
4h	Auto-Negotiation Advertisement Register
5h	Auto-Negotiation Link Partner Ability Register
6h	Auto-Negotiation Expansion Register
7h	Auto-Negotiation Next Page Register
8h	Link Partner Next Page Ability
9h-14h	Reserved
15h	RXER Counter Register
16h – 1ah	Reserved
1bh	Interrupt Control/Status Register
1ch	Reserved
1dh	LinkMD Control/Status Register
1eh	PHY Control Register
1fh	100BASE-TX PHY Control Register

Address	Name	Description	Mode	Default
Register 0h – Basic Control				
0.15	Reset	1 = software reset. Bit is self-clearing	RW/ SC	0
0.14	Loop-back	1 = loop-back mode 0 = normal operation	RW	0
0.13	Speed Select (LSB)	1 = 100Mb/s 0 = 10Mb/s Ignored if Auto-Negotiation is enabled (0.12 = 1)	RW	Set by SPD100
0.12	Auto-Negotiation Enable	1 = enable auto-negotiation process (override 0.13 and 0.8) 0 = disable auto-negotiation process	RW	Set by NWAYEN
0.11	Power Down	1 = power down mode 0 = normal operation	RW	0
0.10	Isolate	1 = electrical isolation of PHY from MII and TX+/TX- 0 = normal operation	RW	Set by ISO
0.9	Restart Auto-Negotiation	1 = restart auto-negotiation process 0 = normal operation. Bit is self-clearing	RW/ SC	0
0.8	Duplex Mode	1 = full duplex 0 = half duplex	RW	Set by DUPLEX
0.7	Collision Test	1 = enable COL test 0 = disable COL test	RW	0
0.6:1	Reserved		RO	0
0.0	Disable Transmitter	0 = enable transmitter 1 = disable transmitter	RW	0

Address	Name	Description	Mode	Default
Register 1h – Basic Status				
1.15	100BASE-T4	1 = T4 capable 0 = not T4 capable	RO	0
1.14	100BASE-TX Full Duplex	1 = capable of 100BASE-X full duplex 0 = not capable of 100BASE-X full duplex	RO	1
1.13	100BASE-TX Half Duplex	1 = capable of 100BASE-X half duplex 0 = not capable of 100BASE-X half duplex	RO	1
1.12	10BASE-T Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex capability	RO	1
1.11	10BASE-T Half Duplex	1 = 10Mbps with half duplex 0 = no 10Mbps with half duplex capability	RO	1
1.10:7	Reserved		RO	0
1.6	No Preamble	1 = preamble suppression 0 = normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = remote fault 0 = no remote fault	RO/ LH	0
1.3	Auto-Negotiation Ability	1 = capable to perform auto-negotiation 0 = unable to perform auto-negotiation	RO	1
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL	0
1.1	Jabber Detect	1 = jabber detected 0 = jabber not detected. Default is Low	RO/ LH	0
1.0	Extended Capability	1 = supports extended capabilities registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	000101
3.9:4	Model Number	Six bit manufacturer's model number	RO	100001
3.3:0	Revision Number	Four bit manufacturer's model number	RO	1010
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = next page capable 0 = no next page capability.	RW	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = remote fault supported 0 = no remote fault	RW	0
4.12 : 11	Reserved		RO	0

Address	Name	Description	Mode	Default
4.10	Pause	1 = pause function supported 0 = no pause function	RW	0
4.9	100BASE-T4	1 = T4 capable 0 = no T4 capability	RO	0
4.8	100BASE-TX Full Duplex	1 = TX with full duplex 0 = no TX full duplex capability	RW	Set by SPD100 & DUPLEX
4.7	100BASE-TX	1 = TX capable 0 = no TX capability	RW	Set by SPD100
4.6	10BASE-T Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps full duplex capability	RW	Set by DUPLEX
4.5	10BASE-T	1 = 10Mbps capable 0 = no 10Mbps capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	00001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = next page capable 0 = no next page capability	RO	0
5.14	Acknowledge	1 = link code word received from partner 0 = link code word not yet received	RO	0
5.13	Remote Fault	1 = remote fault detected 0 = no remote fault	RO	0
5.12	Reserved		RO	0
5.11:10	Pause	5.10 5 .11 0 No PAUSE 1 Asymmetric PAUSE (link partner) 0 Symmetric PAUSE 1 Symmetric & Asymmetric PAUSE (local device)	RO	0
5.9	100 BASE-T4	1 = T4 capable 0 = no T4 capability	RO	0
5.8	100BASE-TX Full Duplex	1 = TX with full duplex 0 = no TX full duplex capability	RO	0
5.7	100BASE-TX	1 = TX capable 0 = no TX capability	RO	0
5.6	10BASE-T Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps full duplex capability	RO	0
5.5	10BASE-T	1 = 10Mbps capable 0 = no 10Mbps capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	00001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0

Address	Name	Description	Mode	Default
6.4	Parallel Detection Fault	1 = fault detected by parallel detection 0 = no fault detected by parallel detection.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = link partner has next page capability 0 = link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = local device has next page capability 0 = local device does not have next page capability	RO	1
6.1	Page Received	1 = new page received 0 = new page not yet received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = link partner has auto-negotiation capability 0 = link partner does not have auto-negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = additional next page(s) will follow 0 = last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = message page 0 = unformatted page	RW	1
7.12	Acknowledge2	1 = will comply with message 0 = cannot comply with message	RW	0
7.11	Toggle	1 = previous value of the transmitted link code word equaled logic One 0 = logic Zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = additional Next Page(s) will follow 0 = last page	RO	0
8.14	Acknowledge	1 = successful receipt of link word 0 = no successful receipt of link word	RO	0
8.13	Message Page	1 = Message Page 0 = Unformatted Page	RO	0
8.12	Acknowledge2	1 = able to act on the information 0 = not able to act on the information	RO	0
8.11	Toggle	1 = previous value of transmitted Link Code Word equal to logic zero 0 = previous value of transmitted Link Code Word equal to logic one	RO	0
8.10:0	Message Field		RO	0
Register 15h – RXER Counter				
15.15:0	RXER Counter	RX Error counter for the RX_ER in each package	RO	0000

Address	Name	Description	Mode	Default
Register 1bh – Interrupt Control/Status Register				
1b.15	Jabber Interrupt Enable	1=Enable Jabber Interrupt 0=Disable Jabber Interrupt	RW	0
1b.14	Receive Error Interrupt Enable	1=Enable Receive Error Interrupt 0=Disable Receive Error Interrupt	RW	0
1b.13	Page Received Interrupt Enable	1=Enable Page Received Interrupt 0=Disable Page Received Interrupt	RW	0
1b.12	Parallel Detect Fault Interrupt Enable	1= Enable Parallel Detect Fault Interrupt 0= Disable Parallel Detect Fault Interrupt	RW	0
1b.11	Link Partner Acknowledge Interrupt Enable	1= Enable Link Partner Acknowledge Interrupt 0= Disable Link Partner Acknowledge Interrupt	RW	0
1b.10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0= Disable Link Down Interrupt	RW	0
1b.9	Remote Fault Interrupt Enable	1= Enable Remote Fault Interrupt 0= Disable Remote Fault Interrupt	RW	0
1b.8	Link Up Interrupt Enable	1= Enable Link Up Interrupt 0= Disable Link Up Interrupt	RW	0
1b.7	Jabber Interrupt	1= Jabber Interrupt Occurred 0= Jabber Interrupt Does Not Occurred	RO/ SC	0
1b.6	Receive Error Interrupt	1= Receive Error Occurred 0= Receive Error Does Not Occurred	RO/ SC	0
1b.5	Page Receive Interrupt	1= Page Receive Occurred 0= Page Receive Does Not Occurred	RO/ SC	0
1b.4	Parallel Detect Fault Interrupt	1= Parallel Detect Fault Occurred 0= Parallel Detect Fault Does Not Occurred	RO/ SC	0
1b.3	Link Partner Acknowledge Interrupt	1= Link Partner Acknowledge Occurred 0= Link Partner Acknowledge Does Not Occurred	RO/ SC	0
1b.2	Link Down Interrupt	1= Link Down Occurred 0= Link Down Does Not Occurred	RO/ SC	0
1b.1	Remote Fault Interrupt	1= Remote Fault Occurred 0= Remote Fault Does Not Occurred	RO/ SC	0
1b.0	Link Up Interrupt	1= Link Up Interrupt Occurred 0= Link Up Interrupt Does Not Occurred	RO/ SC	0
Register 1dh – LinkMD Control/Status Register				
1d.15	Cable diagnostic test enable	0 = Indicates cable diagnostic test has completed and the status information is valid for read. 1 = the cable diagnostic test is activated. This bit is self-clearing.	RW/ SC	0

Address	Name	Description	Mode	Default
1d.14:13	Cable diagnostic test result	[00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test failed	RO	0
1d.12:9	Reserved			
1d.8:0	Cable fault counter	Distance to fault, approximately 0.39m*cabfaultcnt value	RO	0
Register 1eh – PHY Control				
1e:15:14	LED mode	[00] = LED3 <- collision LED2 <- full duplex LED1 <- speed LED0 <- link/activity [01] = LED3 <- activity LED2 <- full duplex/collision LED1 <- speed LED0 <- link [10] = LED3 <- activity LED2 <- full duplex LED1 <- 100Mbps link LED0 <- 10Mbps link [11] = reserved	RW	0
1e.13	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed	RO	
1e.12	Far end fault detect	0 = Far end fault detected 1 = Far end fault not detected	RO	
1e.11	MDIX/MDI state	0 = MDIX 1 = MDI	RO	
1e:10:8	Reserved			
1e:7	Remote loopback	0: normal mode 1: remote (analog) loop back is enable	RW	0
1e:6:0	Reserved			
Register 1fh – 100BASE-TX PHY Controller				
1f:15	HP_MDIX	0: Micrel Auto MDI/MDI-X mode 1: HP Auto MDI/MDI-X mode	RW	1

Address	Name	Description	Mode	Default
1f:14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 0 = Transmit on TX+/- (pins 41,40) Receive on RX+/- (pins 33,32) 1 = Transmit on RX+/- (pins 33,32) Receive on TX+/- (pins 41,40)	RW	0
1f:13	Pairswap disable	1 = disable MDI/MDIX 0 = enable MDI/MDIX	RW	0
1f.12	Energy detect	1 = presence of signal on RX+/- analog wire pair 0 = no signal detected on RX+/-	RO	0
1f.11	Force link	1 = force link pass 0 = normal link operation This bit bypasses the control logic and allow transmitter to send pattern even if there is no link.	RW	0
1f.10	Power Saving	1 = enable power saving 0 = disable	RW	1
1f.9	Interrupt Level	1 = interrupt pin active high 0 = active low	RW	0
1f.8	Enable Jabber	1 = enable jabber counter 0 = disable	RW	1
1f.7	Auto-Negotiation Complete	1 = auto-negotiation complete 0 = not complete This bit has the same definition as register 1.5.	RO	0
1f.6	Enable Pause (Flow-Control Result)	1 = flow control capable 0 = no flow control	RO	0
1f.5	PHY Isolate	1 = PHY in isolate mode 0 = not isolated	RO	0
1f.4:2	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10BASE-T half duplex [010] = 100BASE-TX half duplex [011] = default [101] = 10BASE-T full duplex [110] = 100BASE-TX full duplex [111] = PHY/MII isolate	RO	0
1f.1	Enable SQE test	1 = enable SQE test 0 = disable	RW	0
1f.0	Disable Data Scrambling	1 = disable scrambler 0 = enable	RW	0

Absolute Maximum Rating (Note 1)

Storage Temperature (T_S) …… -55°C to +150°C
Supply Referenced to GND…… ……-0.5V to +4.0
All pins ……....-0.5V to +4.0

Important: Please read the Notes at the end of the Electrical Characteristics.

Operating Range (Note 2)

Supply Voltage
(V_{DDPLL}, V_{DDRX}, V_{DDC})……1.8V ± 5%
($V_{DDRCV,}$ V_{DDIO})……3.3V ± 5%
Ambient Temperature Commercial (T_{AC})……0°C to +70°C
Ambient Temperature Industrial (T_{AI})…….-40°C to +85°C

Package Thermal Resistance (θ_{JA})[Note 3]

Thermal Resistance	θ_{JA}	θ_{JA}	θ_{JA}	θ_{JC}
Airflow Velocity (m/s)	0	1	2	0
KSZ8001L / KSZ8001LI	83.56	77.08	72.36	35.90
KSZ8001SL / KSZ8001SLI	75.19	68.20	66.43	42.65
KSZ8001S	42.43	36.19	34.24	6.75

Electrical Characteristics [Note4]

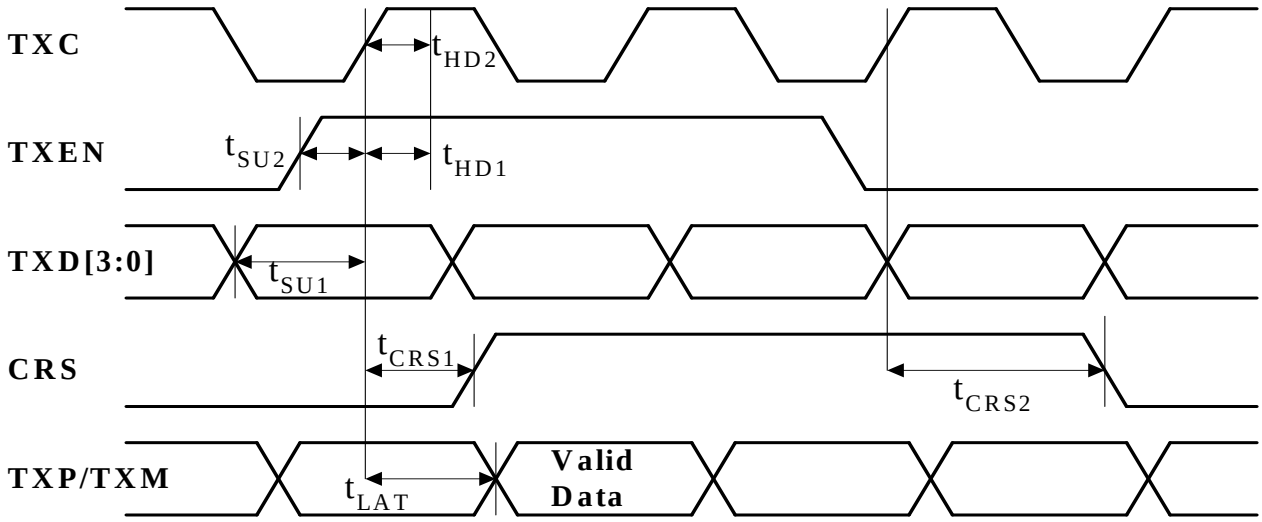
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Total Supply Current [Note 5]						
KSZ8001L	- Current consumption is for the single 3.3V supply KSZ8001L device only, and includes the 1.8V supply voltages (VDDRX, VDDPLL) that are provided by the KSZ8001L via power output pin 13 (VDDC). - Transformer consumes an additional 45mA @ 3.3V for 100BASE-TX and 70mA @ 3.3V for 10BASE-T.					
I_{DD1}	100BASE-TX	Chip only, no transformer		52		mA
I_{DD2}	10BASE-T	Chip only, no transformer		32		mA
I_{DD3}	Power Saving Mode	Ethernet cable disconnected		35		mA
I_{DD4}	SW Power Down Mode	Register (software) power down		5		mA
I_{DD5}	Power down pin (PD#)	Chip (hardware) power down		3		mA
TTL Inputs						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND – V_{DD}		-10	10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4			V
V_{OL}	Output Low Voltage				0.4	V
$I I_{OZ} I$	Output Tri-State Leakage				10	µA
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Ouput Voltage	50Ω from each output to V_{DD}	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	50Ω from each output to V_{DD}			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.25	ns
	Overshoot				5	%
V_{SET}	Refernce Voltage of ISET			0.75		V
	Propagation Delay			45	60	Ns
	Jitter			0.7	1.4	$ns_{(pk-pk)}$

10BASE-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Ouput Voltage	50Ω from each output to V_{DD}	2.2		2.8	V
V_{IMB}	Output Voltage Imbalance	50Ω from each output to V_{DD}			±3.5	ns
t_r, t_t	Rise/Fall Time			25		ns
Clock Outputs						
X1, X2	Crystal Oscillator			25		MHz
RXC_{100}	Receive Clock, 100TX			25		MHz
RXC_{10}	Receive Clock, 10T			2.5		MHz
	Receive Clock Jitter			3.0		$ns_{(pk-pk)}$
TXC_{100}	Transmit Clock, 100TX			25		MHz
TXC_{10}	Transmit Clock, 10T			2.5		MHz
	Transmit Clock Jitter			1.8		$ns_{(pk-pk)}$

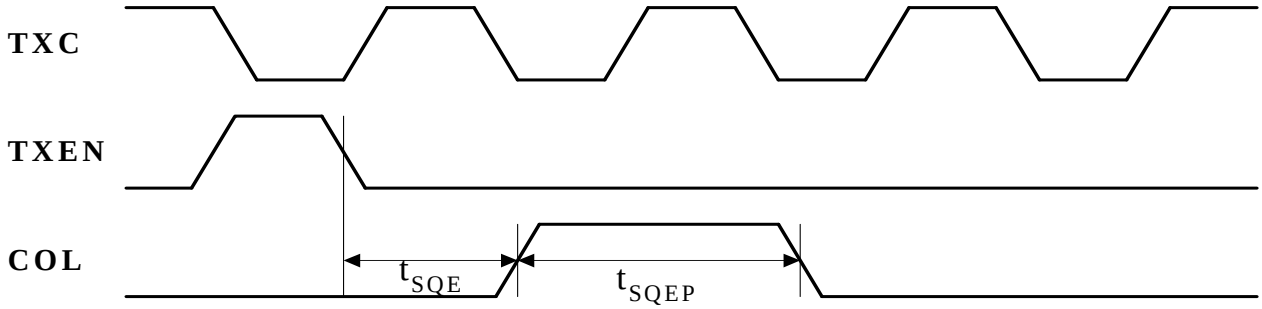
Note 1: Exceeding the absolute rating(s) may cause permanent damage to the device. Operating at maximum conditions for extended periods may affect device reliability.
Note 2: This device is not guaranteed to operate beyond its specified operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).
Note 3: No HS (heat spreader) in package.
Note 4: Specification for packaged product only.
Note 5: 100% data transmission in full-duplex mode and minimum IPG with 130-meter cable.

Timing Diagrams

10BaseT MII Transmit Timing

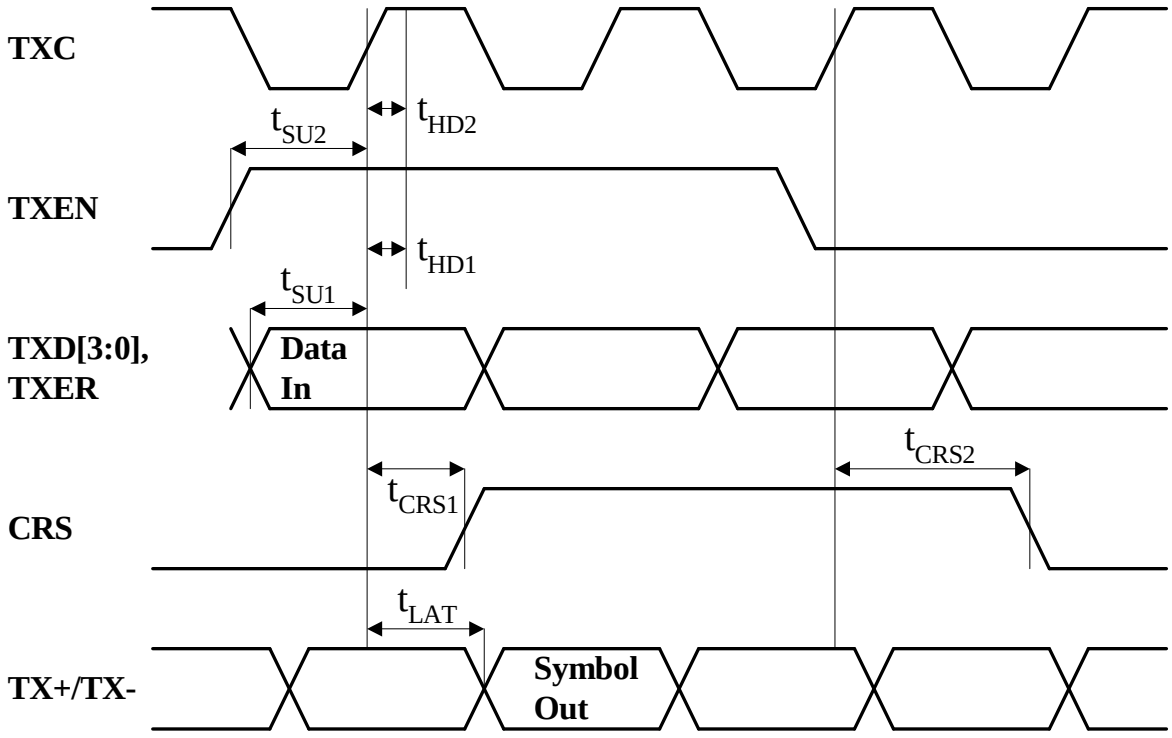


SQE Timing



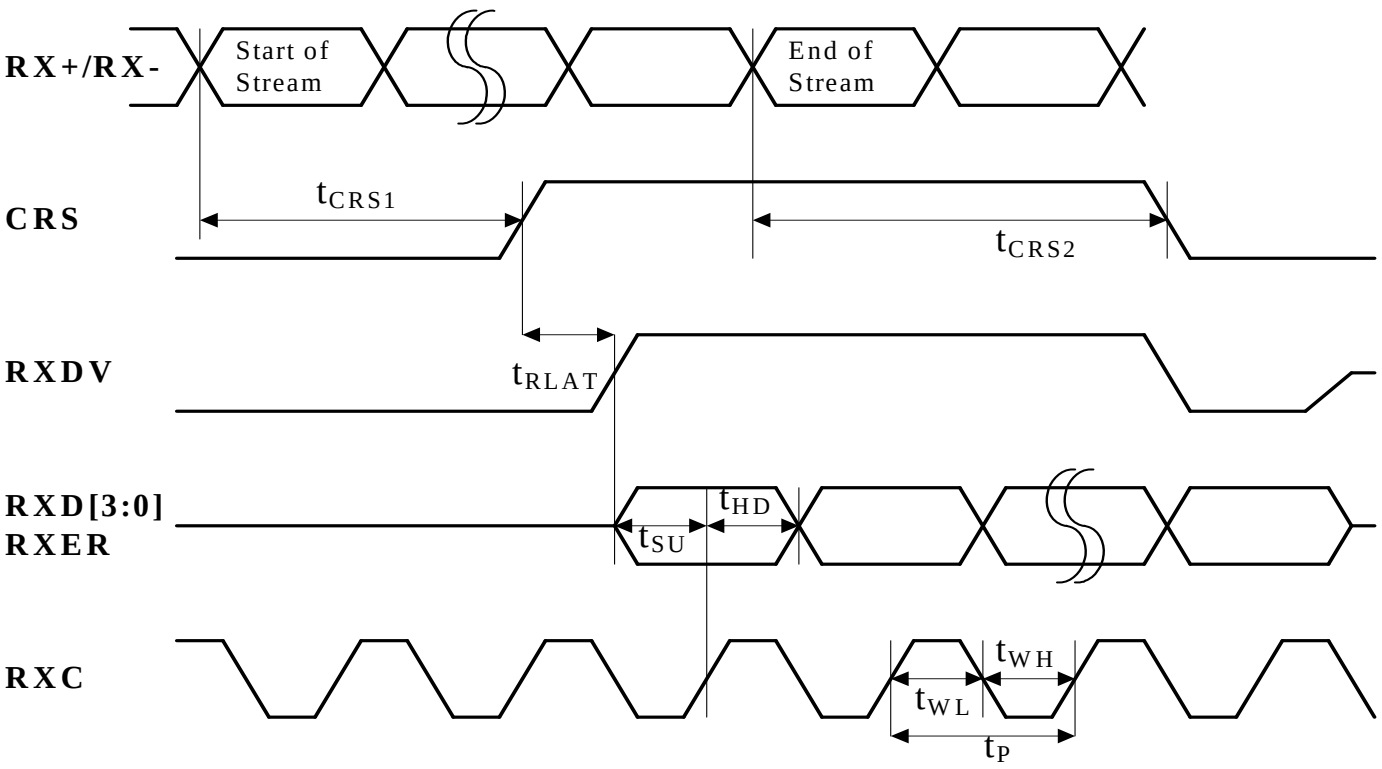
		min.	typ.	max.
t_{SU1}	TXD[3:0] Setup to TXC High	10ns		
t_{SU2}	TXEN Setup to TXC High	10ns		
t_{HD1}	TXD[3:0] Hold after TXC High	0ns		
t_{HD2}	TXEN Hold after TXC High	0ns		
t_{CRS1}	TXEN High to CRS asserted latency		4BT	
t_{CRS2}	TXEN Low to CRS de-asserted latency		8BT	
t_{LAT}	TXEN High to TXP/TXM output (TX latency)		4BT	
t_{SQE}	COL (SQE) Delay after TXEN de-asserted		2.5us	
t_{SQEP}	COL (SQE) Pulse Duration		1.0us	

100BaseTX MII Transmit Timing



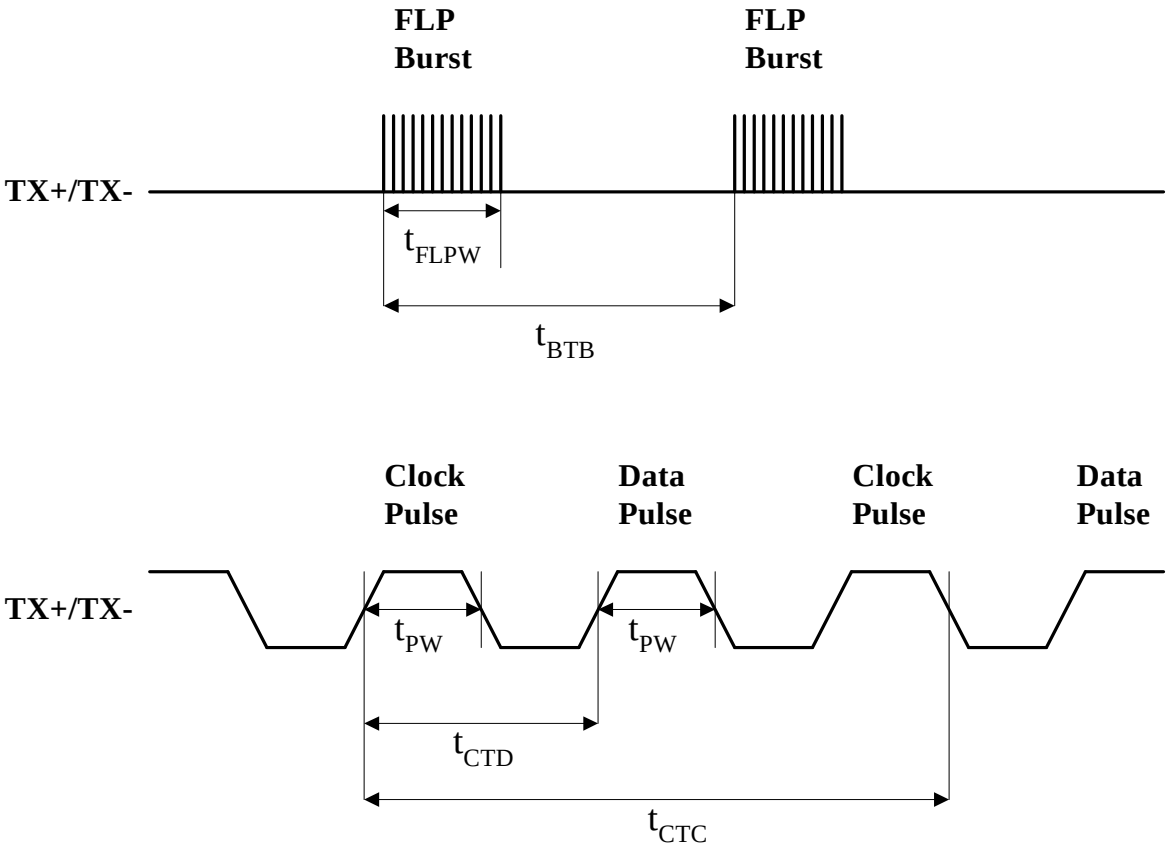
		min.	typ.	max.
t_{SU1}	TXD[3:0] Setup to TXC High	10ns		
t_{SU2}	TX_ER Setup to TXC High	10ns		
t_{HD1}	TXD[3:0] Hold after TXC High	0ns		
t_{HD2}	TXER Hold after TXC High	0ns		
t_{HD3}	TXEN Hold after TXC High	0ns		
t_{CRS1}	TXEN High to CRS asserted latency		4BT	
t_{CRS2}	TXEN Low to CRS de-asserted latency		4BT	
t_{LAT}	TXEN High to TX+/TX- output (TX latency)		7BT	

100BaseTX MII Receive Timing



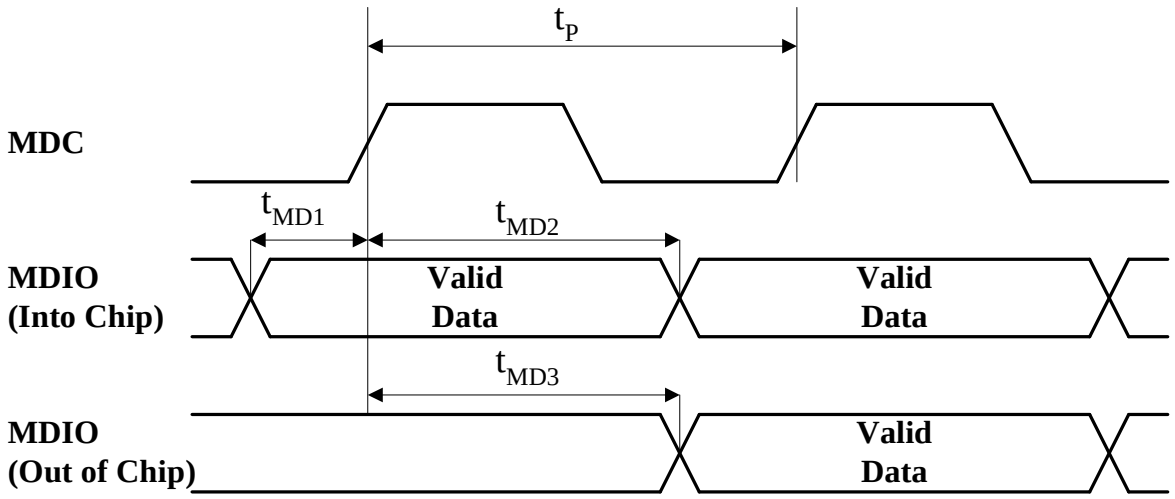
		min.	typ.	max.
t_P	RXC period		40ns	
t_{WL}	RXC pulse width		20ns	
t_{WH}	RXC pulse width		20ns	
t_{SU}	RXD[3:0], RXER, RXDV setup to rising edge of RXC		20ns	
t_{HD}	RXD[3:0], RXER, RXDV hold from rising edge of RXC		20ns	
t_{RLAT}	CRS to RXD latency, 4B or 5B aligned	1BT	2BT	3BT
t_{CRS1}	"Start of Stream" to CRS asserted		140ns	
t_{CRS2}	"End of Stream" to CRS de-asserted		170ns	

Auto Negotiation / Fast Link Pulse Timing



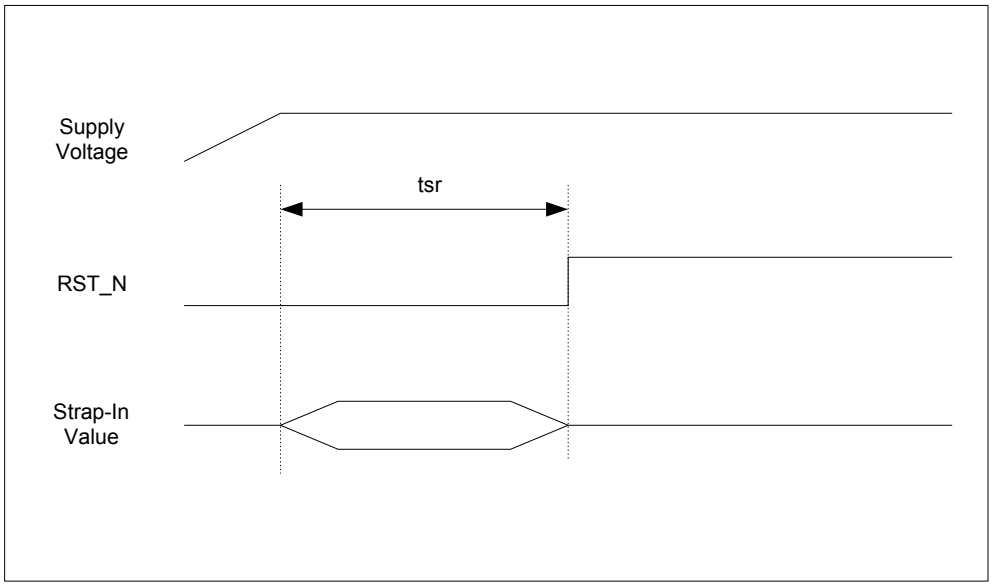
		min.	typ.	max.
t_{BTB}	FLP burst to FLP burst	8ms	16ms	24ms
t_{FLPW}	FLP burst width		2ms	
t_{PW}	Clock/Data pulse width		100ns	
t_{CTD}	Clock pulse to data pulse		69us	
t_{CTC}	Clock pulse to clock pulse		136us	
	Number of Clock/Data pulses per burst	17		33

Serial Management Interface Timing



		min.	typ.	max.
t_P	MDC period		400 ns	
t_{MD1}	MDIO Setup to MDC (MDIO as input)	10ns		
t_{MD2}	MDIO Hold after MDC (MDIO as input)	10ns		
t_{MD3}	MDC to MDIO Valid (MDIO as output)		222ns	

Reset Timing Diagram

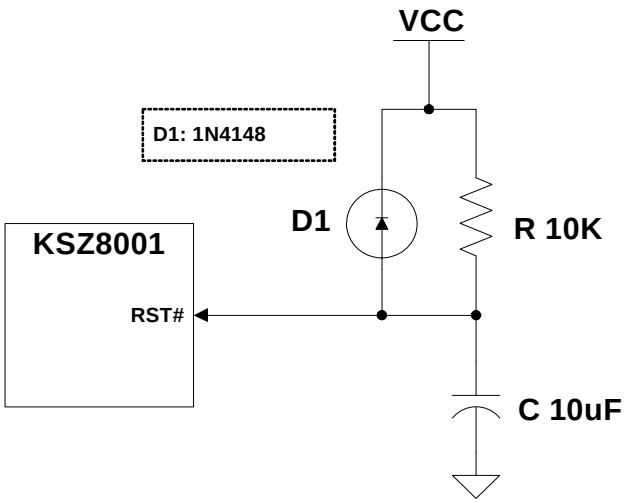


Reset Timing Parameters

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltages to reset high	50		us

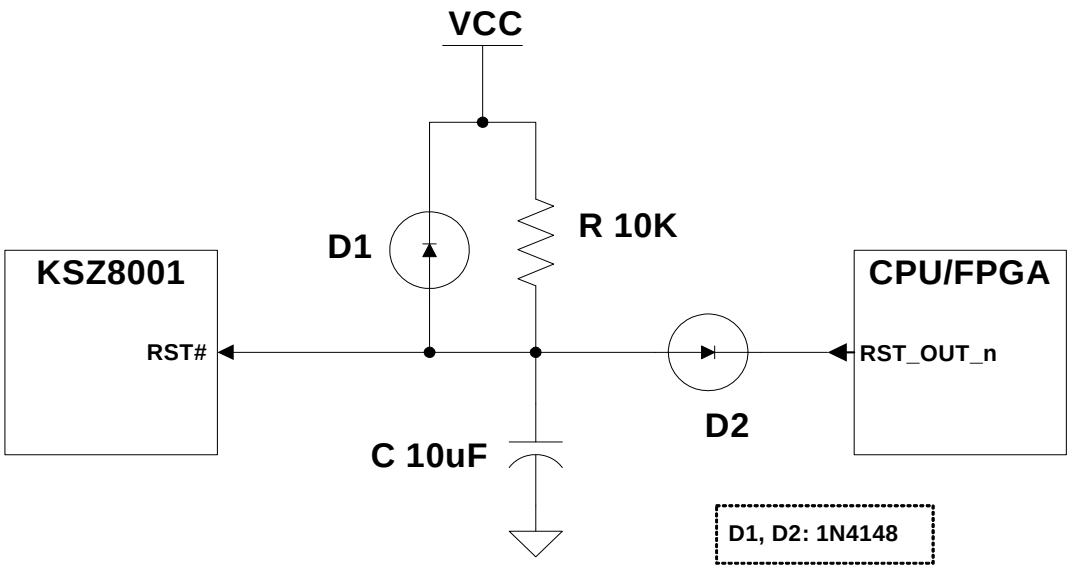
Reset Circuit Diagram

Micrel recommends the following discrete reset circuit when powering up the KSZ8001 device.



Recommended Reset Circuit

For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), the following reset circuit is recommended.

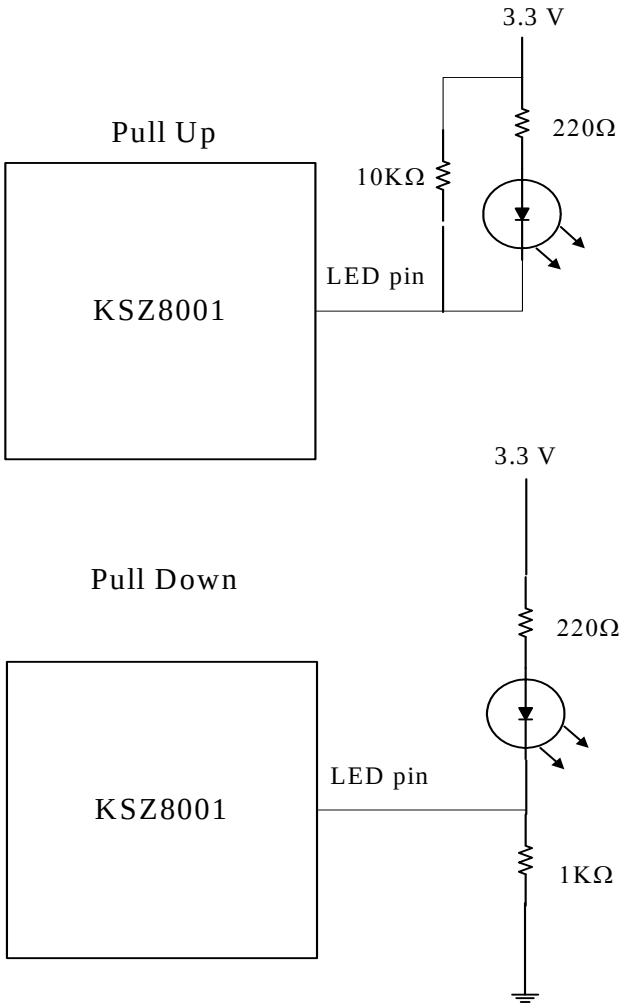


Recommended Circuit for Interfacing with CPU/FPGA Reset

At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the Micrel device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommend to power up VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.

Reference Circuit for Strapping Option Configuration

The following figure shows the reference circuits for external pull-up and pull-down on the LED strapping pins.



Reference circuits for unmanaged programming through LED ports

Selection of Isolation Transformer

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Transformer Selection Criteria

Parameter	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350 uH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 uH	1 MHz (min.)
Inter-Winding Capacitance (max.)	12 pF	
D.C. Resistance (max.)	0.9 Ohms	
Insertion Loss (max.)	1.0 dB	0-65 MHz
HIPOT (min.)	1500 Vrms	

Magnetic Vendor Selection Lists

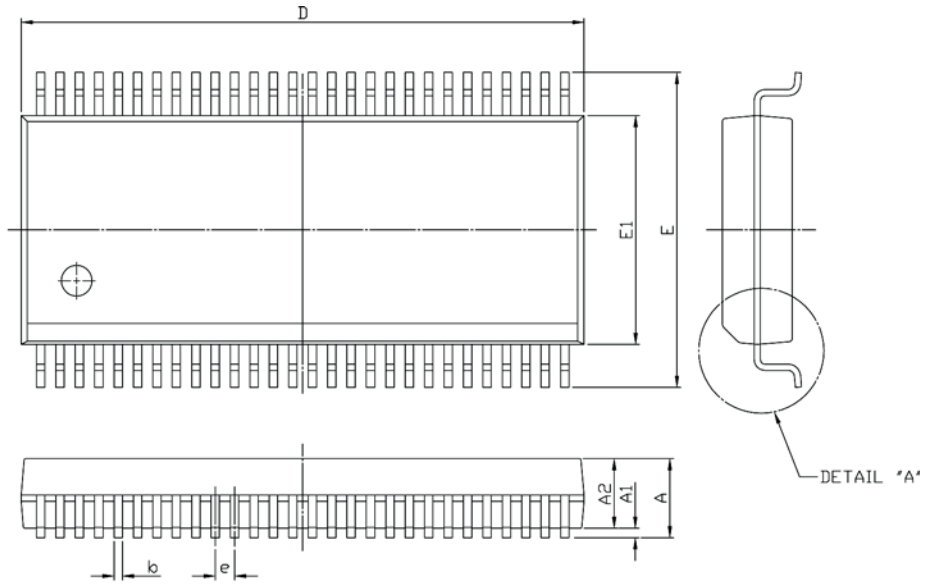
Single Port			
Magnetic manufacturer	Part number	AUTO MDIX	Number of port
Pulse	H1102	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
Bel Fuse	SI-46001	Yes	1
Bel Fuse	SI-50170	Yes	1
YCL	PT163020	Yes	1
Transpower	HB726	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1

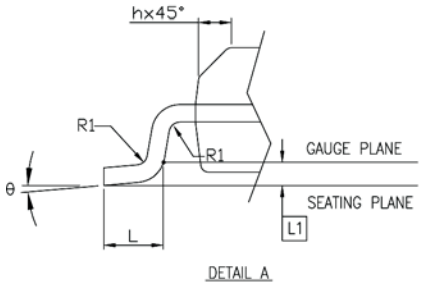
Selection of Reference Crystal

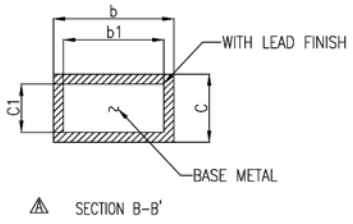
An oscillator or crystal with the following typical characteristics is recommended.

Charateristics	Value	Units
Frequency	25.00000	MHz
Frequency Tolerance(max)	± 50	ppm
Load Capacitance (max)	20	pF
Series Resistance	40	Ω

Package Information



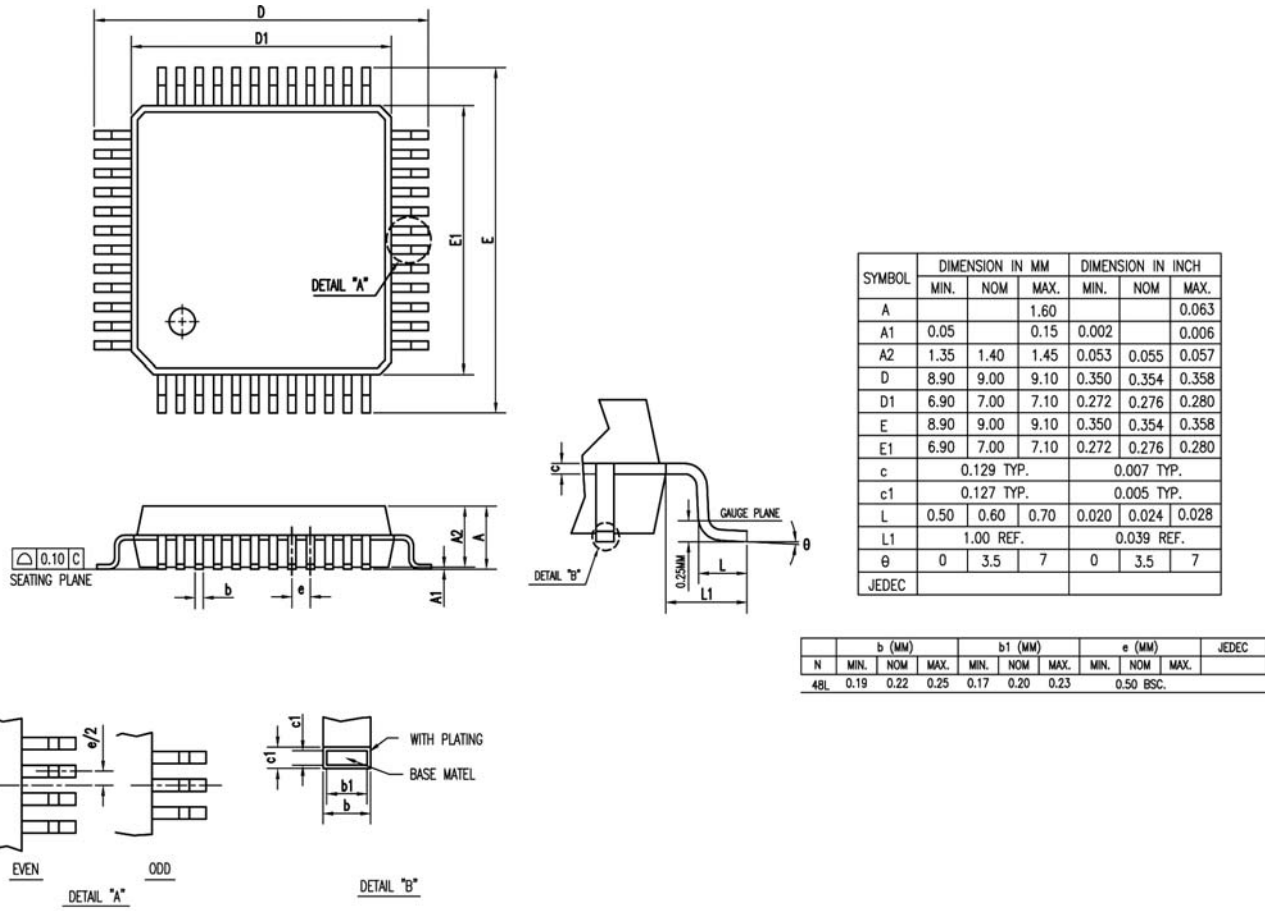




SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.413	2.591	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.014
b1	0.203	0.254	0.305	0.008	0.010	0.012
c	0.127		0.254	0.005		0.010
c1	0.127		0.216	0.005		0.009
E	10.058	10.312	10.566	0.396	0.406	0.416
E1	7.391	7.493	7.595	0.291	0.295	0.299
e	0.635 BASIC			0.025 BASIC		
h	0.381		0.635	0.015		0.025
L	0.508		1.016	0.020		0.040
L1	0.254 BASIC			0.010 BASIC		
R1						
θ	0		5	0		5

	D (MM)			JEDEC
N	MIN.	NOM	MAX.	
48	15.748	15.875	16.002	MO-118AA
56	18.288	18.415	18.542	MO-118AB

48-Pin SSOP (SM)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.129 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23		0.50 BSC.		

48-Pin LQFP (LQ)

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL: +1 (408) 944-0800 FAX: +1 (408) 944-0970 WEB: http:/www.micrel.com