

## PIN DESCRIPTION

| SYMBOL             | FUNCTION | DESCRIPTION                                                                                                     |
|--------------------|----------|-----------------------------------------------------------------------------------------------------------------|
| VCC                | POWER    | +5V $\pm 5\%$                                                                                                   |
| 429DI1 (A)         | INPUT    | ARINC receiver 1 positive input                                                                                 |
| 429DI1 (B)         | INPUT    | ARINC receiver 1 negative input                                                                                 |
| 429DI2 (A)         | INPUT    | ARINC receiver 2 positive input                                                                                 |
| 429DI2 (B)         | INPUT    | ARINC receiver 2 negative input                                                                                 |
| $\overline{D/R1}$  | OUTPUT   | Receiver 1 data ready flag                                                                                      |
| $\overline{D/R2}$  | OUTPUT   | Receiver 2 data ready flag                                                                                      |
| SEL                | INPUT    | Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2)                                                          |
| $\overline{EN1}$   | INPUT    | Data Bus control, enables receiver 1 data to outputs                                                            |
| $\overline{EN2}$   | INPUT    | Data Bus control, enables receiver 2 data to outputs if $\overline{EN1}$ is high                                |
| BD15               | I/O      | Data Bus                                                                                                        |
| BD14               | I/O      | Data Bus                                                                                                        |
| BD13               | I/O      | Data Bus                                                                                                        |
| BD12               | I/O      | Data Bus                                                                                                        |
| BD11               | I/O      | Data Bus                                                                                                        |
| BD10               | I/O      | Data Bus                                                                                                        |
| BD09               | I/O      | Data Bus                                                                                                        |
| BD08               | I/O      | Data Bus                                                                                                        |
| BD07               | I/O      | Data Bus                                                                                                        |
| BD06               | I/O      | Data Bus                                                                                                        |
| GND                | POWER    | 0 V                                                                                                             |
| BD05               | I/O      | Data Bus                                                                                                        |
| BD04               | I/O      | Data Bus                                                                                                        |
| BD03               | I/O      | Data Bus                                                                                                        |
| BD02               | I/O      | Data Bus                                                                                                        |
| BD01               | I/O      | Data Bus                                                                                                        |
| BD00               | I/O      | Data Bus                                                                                                        |
| $\overline{PL1}$   | INPUT    | Latch enable for byte 1 entered from data bus to transmitter FIFO.                                              |
| $\overline{PL2}$   | INPUT    | Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{PL1}$ .               |
| TX/R               | OUTPUT   | Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty. |
| 429DO              | OUTPUT   | "ONES" data output from transmitter.                                                                            |
| $\overline{429DO}$ | OUTPUT   | "ZEROES" data output from transmitter.                                                                          |
| ENTX               | INPUT    | Enable Transmission                                                                                             |
| $\overline{CWSTR}$ | INPUT    | Clock for control word register                                                                                 |
| CLK                | INPUT    | Master Clock input                                                                                              |
| TX CLK             | OUTPUT   | Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.                                      |
| $\overline{MR}$    | INPUT    | Master Reset, active low                                                                                        |

## FUNCTIONAL DESCRIPTION

### CONTROL WORD REGISTER

The HI-8282 contains 10 data flip flops whose D inputs are connected to the data bus and clocks connected to CWSTR. Each flip flop provides options to the user as follows:

| DATA BUS PIN | FUNCTION             | CONTROL            | DESCRIPTION                                                                                      |
|--------------|----------------------|--------------------|--------------------------------------------------------------------------------------------------|
| BDO5         | SELF TEST            | 0 = ENABLE         | If enabled, an internal connection is made passing 429DO and 429D0 to the receiver logic inputs  |
| BDO6         | RECEIVER 1 DECODER   | 1 = ENABLE         | If enabled, ARINC bits 9 and, 10 must match the next two control word bits                       |
| BDO7         | -                    | -                  | If Receiver 1 Decoder is enabled, the ARINC bit 9 must match this bit                            |
| BDO8         | -                    | -                  | If Receiver 1 Decoder is enabled, the ARINC bit 10 must match this bit                           |
| BDO9         | RECEIVER 2 DECODER   | 1 = ENABLE         | If enabled, ARINC bits 9 and 10 must match the next two control word bits                        |
| BD10         | -                    | -                  | If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit                           |
| BD11         | -                    | -                  | If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit                          |
| BD12         | INVERT XMTR PARITY   | 1 = ENABLE         | Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit |
| BD13         | XMTR DATA CLK SELECT | 0 = ÷10<br>1 = ÷80 | CLK is divided either by 10 or 80 to obtain XMTR data clock                                      |
| BD14         | RCVR DTA CLK SELECT  | 0 = ÷10<br>1 = ÷80 | CLK is divided either by 10 or 80 to obtain RCVR data clock                                      |

### ARINC 429 DATA FORMAT

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

| BYTE 1       |          |          |          |          |          |          |          |          |          |          |          |          |          |          |          |          |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| DATA<br>BUS  | BD<br>15 | BD<br>14 | BD<br>13 | BD<br>12 | BD<br>11 | BD<br>10 | BD<br>09 | BD<br>08 | BD<br>07 | BD<br>06 | BD<br>05 | BD<br>04 | BD<br>03 | BD<br>02 | BD<br>01 | BD<br>00 |
| ARINC<br>BIT | 13       | 12       | 11       | 10       | 9        | 31       | 30       | 32       | 1        | 2        | 3        | 4        | 5        | 6        | 7        | 8        |

| BYTE 2       |          |          |          |          |          |          |          |          |          |          |          |          |          |          |          |          |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| DATA<br>BUS  | BD<br>15 | BD<br>14 | BD<br>13 | BD<br>12 | BD<br>11 | BD<br>10 | BD<br>09 | BD<br>08 | BD<br>07 | BD<br>06 | BD<br>05 | BD<br>04 | BD<br>03 | BD<br>02 | BD<br>01 | BD<br>00 |
| ARINC<br>BIT | 29       | 28       | 27       | 26       | 25       | 24       | 23       | 22       | 21       | 20       | 19       | 18       | 17       | 16       | 15       | 14       |

### THE RECEIVERS

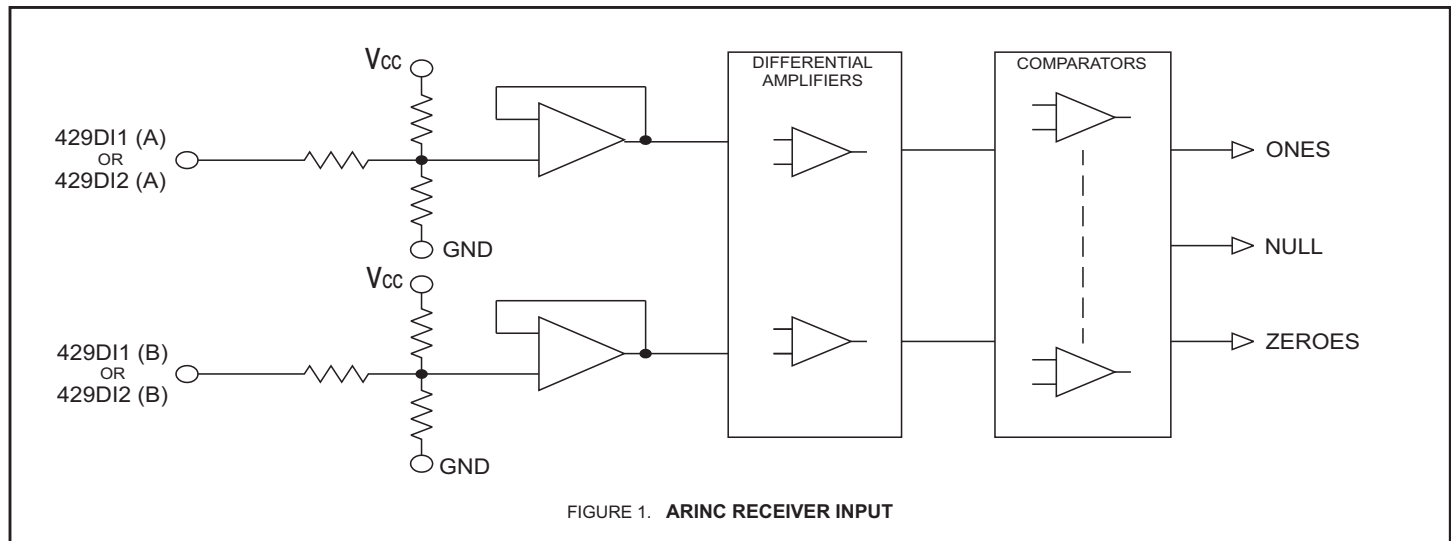
#### ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

| STATE | DIFFERENTIAL VOLTAGE     |
|-------|--------------------------|
| ONE   | +6.5 Volts to +13 Volts  |
| NULL  | +2.5 Volts to -2.5 Volts |
| ZERO  | -6.5 Volts to -13 Volts  |

The HI-8282 guarantees recognition of these levels with a common mode voltage with respect to GND less than  $\pm 4V$  for the worst case condition (4.75V supply and 13v signal level).

Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.



# FUNCTIONAL DESCRIPTION (cont.)

## RECEIVER LOGIC OPERATION

Figure 2 is a block diagram showing each receiver's logic.

### BIT TIMING

ARINC 429 specifies the following timing for received data:

|                 | HIGH SPEED              | LOW SPEED             |
|-----------------|-------------------------|-----------------------|
| BIT RATE        | 100K BPS $\pm$ 1%       | 12K -14.5K BPS        |
| PULSE RISE TIME | 1.5 $\pm$ 0.5 $\mu$ sec | 10 $\pm$ 5 $\mu$ sec  |
| PULSE FALL TIME | 1.5 $\pm$ 0.5 $\mu$ sec | 10 $\pm$ 5 $\mu$ sec  |
| PULSE WIDTH     | 5 $\mu$ sec $\pm$ 5%    | 34.5 - 41.7 $\mu$ sec |

The HI-8282 accepts signals meeting these specifications and rejects signals outside these tolerances using the method described here:

1. The timing logic requires an accurate 1.0 MHz clock source. Less than 0.1% error is recommended.
2. The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. To qualify data bits, One or Zero in the upper bits of the sampling shift register must be followed by Null in the lower bits within the data bit time. A word gap Null requires three consecutive Nulls in both the upper and lower bits of the sampling shift register. This guarantees the minimum pulse width.
3. Each data bit must follow its predecessor by not less than 8 samples and not more than 12 samples. In this manner the bit rate is checked. With exactly 1 MHz input clock frequency, the acceptable data bit rates are as follows:

|                   | HIGH SPEED | LOW SPEED |
|-------------------|------------|-----------|
| DATA BIT RATE MIN | 83K BPS    | 10.4K BPS |
| DATA BIT RATE MAX | 125K BPS   | 15.6K BPS |

4. The Word Gap timer samples the Null shift register every 10 input clocks (80 for low speed) after the last data bit of a valid reception. If the Null is present, the Word Gap counter is incremented. A count of 3 enables the next reception.

### RECEIVER PARITY

The 32nd bit of received ARINC words stored in the receive FIFO is used as a Parity Flag indicating whether good Odd parity is received from the incoming ARINC word.

#### Odd Parity Received

The parity bit is reset to indicate correct parity was received and the resulting word is then written to the receive FIFO.

#### Even Parity Received

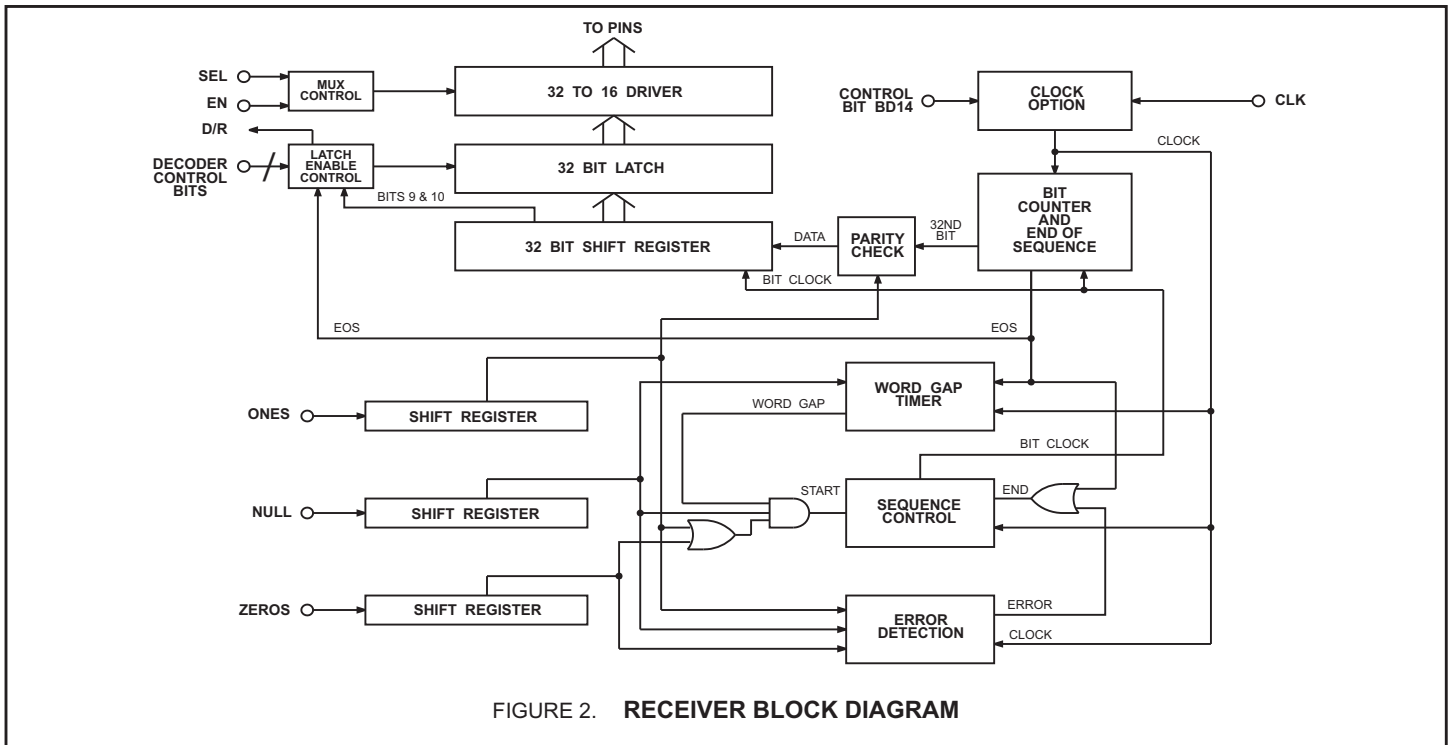
The receiver sets the 32nd bit to a "1", indicating a parity error and the resulting word is then written to the receive FIFO.

Therefore, the 32nd bit retrieved from the receiver FIFO will always be a "0" when valid (odd parity) ARINC 429 words are received.

### RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a "1", D/R1 or D/R2 (or both) will go low. The data flag for a receiver remains low until after both ARINC bytes from that receiver are retrieved. This is accomplished by first activating EN with SEL, the byte selector, low to retrieve the first byte and then activating EN with SEL high to retrieve the second byte. EN1 retrieves data from receiver 1 and EN2 retrieves data from receiver 2.

If another ARINC word is received and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.



## FUNCTIONAL DESCRIPTION (cont.)

### TRANSMITTER

A block diagram of the transmitter section is shown in Figure 3.

### FIFO OPERATION

The FIFO is loaded sequentially by first pulsing  $\overline{PL1}$  to load byte 1 and then  $\overline{PL2}$  to load byte 2. The control logic automatically loads the 31 bit word in the next available position of the FIFO. If TX/R, the transmitter ready flag, is high (FIFO empty), then 8 words, each 31 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 8 positions are full, the FIFO ignores further attempts to load data.

### DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either 429DO or 429D $\overline{O}$ . The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

|                     | <u>HIGH SPEED</u> | <u>LOW SPEED</u> |
|---------------------|-------------------|------------------|
| ARINC DATA BIT TIME | 10 Clocks         | 80 Clocks        |
| DATA BIT TIME       | 5 Clocks          | 40 Clocks        |
| NULL BIT TIME       | 5 Clocks          | 40 Clocks        |
| WORD GAP TIME       | 40 Clocks         | 320 Clocks       |

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

### TRANSMITTER PARITY

The parity generator counts the ONES in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high, the parity is even.

### SELF TEST

If the BD05 control word bit is set low, the digital outputs of the transmitter are internally connected to the logic inputs of the receivers, bypassing the analog bus interface circuitry. Data to Receiver 1 is as transmitted and data to Receiver 2 is the complement. All data transmitted during self test is also present on the TXA(OUT) and TXB(OUT) line driver outputs.

### SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.
2. The FIFO can store 8 words maximum and ignores attempts to load addition data if full.
3. Byte 1 of the transmitter data must be loaded first.
4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.
5. After ENTX, transmission enable, goes high it cannot go low until TX/R, transmitter ready flag, goes high. Otherwise, one ARINC word is lost during transmission.

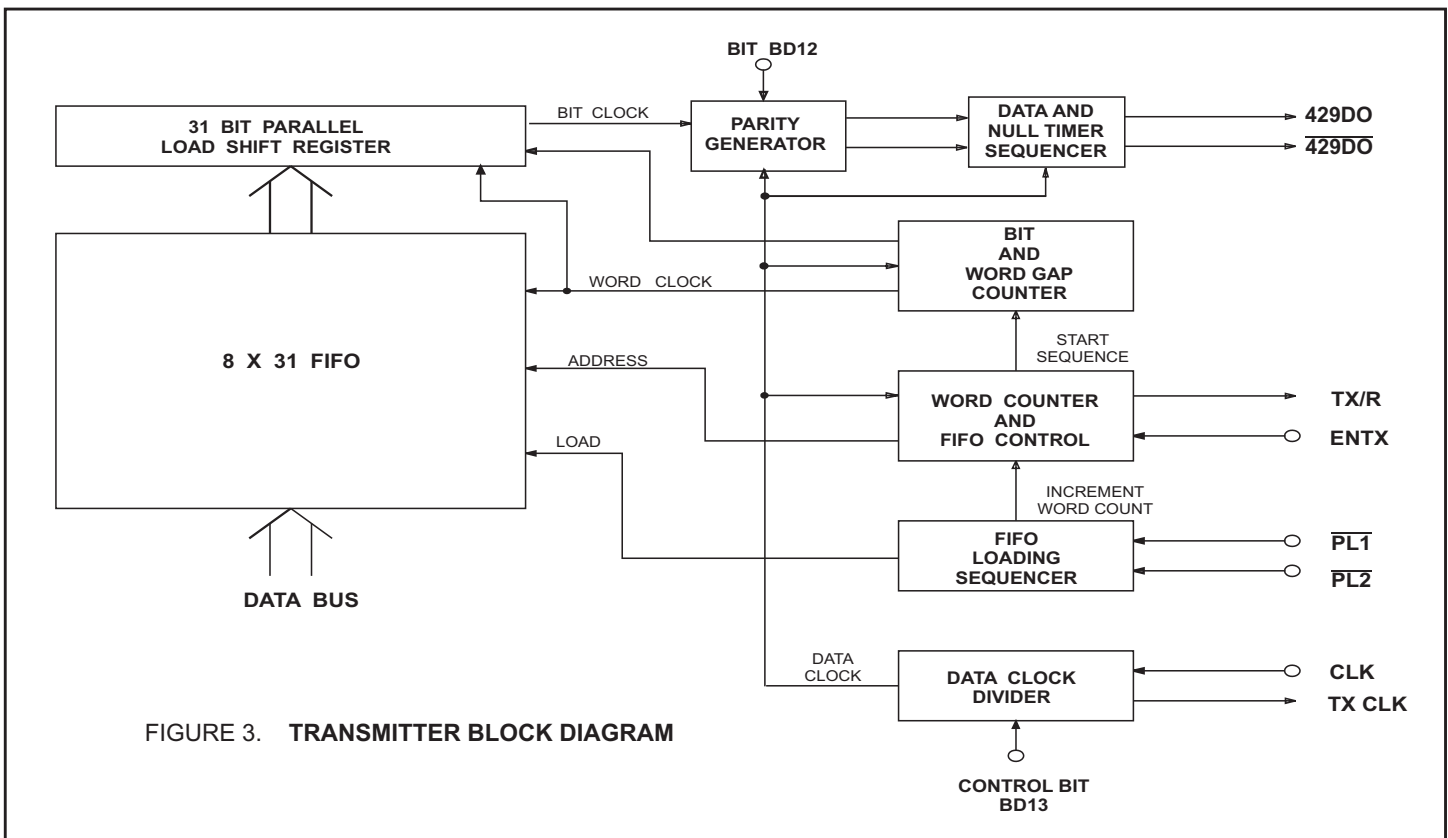


FIGURE 3. TRANSMITTER BLOCK DIAGRAM

## REPEATER OPERATION

In normal (non-repeater) operation, either byte of the received data word may be read first by using the SEL input. During repeater operation however, data word lower byte must always be read first. While the data is being read, it is loading concurrently into the Transmit FIFO, which always loads lower byte first.

Upon Master Reset, data transmission and reception are immediately terminated, all three FIFOs are cleared as are the FIFO flags at the device pins and in the Status Register. The Control Word register is not affected by a Master Reset.

The diagram illustrates the timing relationship between the 429DO and 429DI signals for a specific data rate example. The 429DO signal is shown as a high-level signal with a single pulse. The 429DI signal is shown as a low-level signal with multiple pulses. The timing is defined by the following periods:

- ARINC BIT:** The period between the start of the 429DO pulse and the start of the first 429DI pulse.
- DATA:** The period between the start of one 429DI pulse and the start of the next 429DI pulse.
- NULL:** The period between the end of one 429DI pulse and the start of the next 429DI pulse.
- WORD GAP:** The period between the end of the last 429DI pulse and the start of the next 429DO pulse.

The diagram also indicates the bit positions for the data pulses: BIT 30, BIT 31, and BIT 32. The next word is indicated as BIT 1 NEXT WORD.

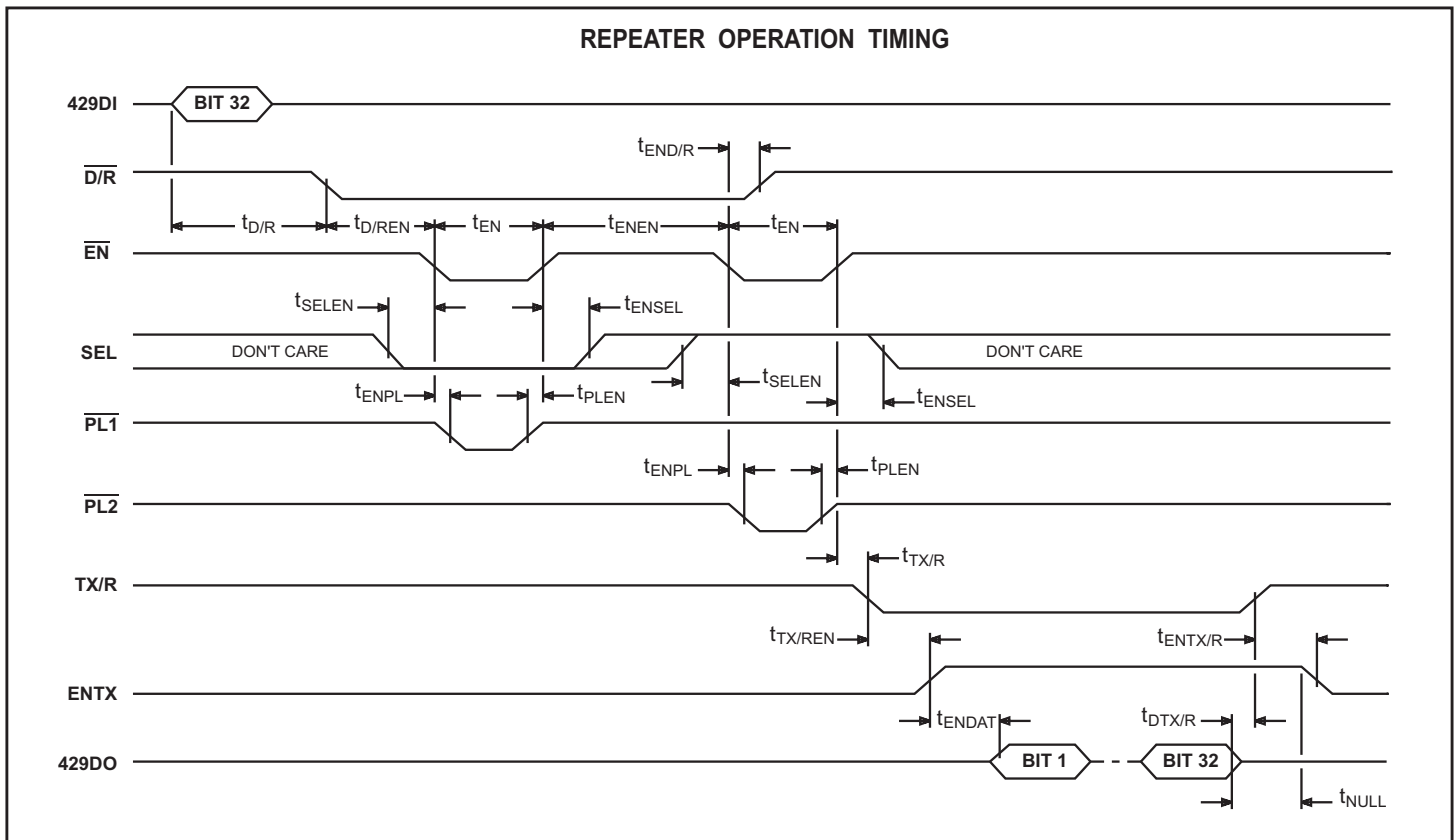
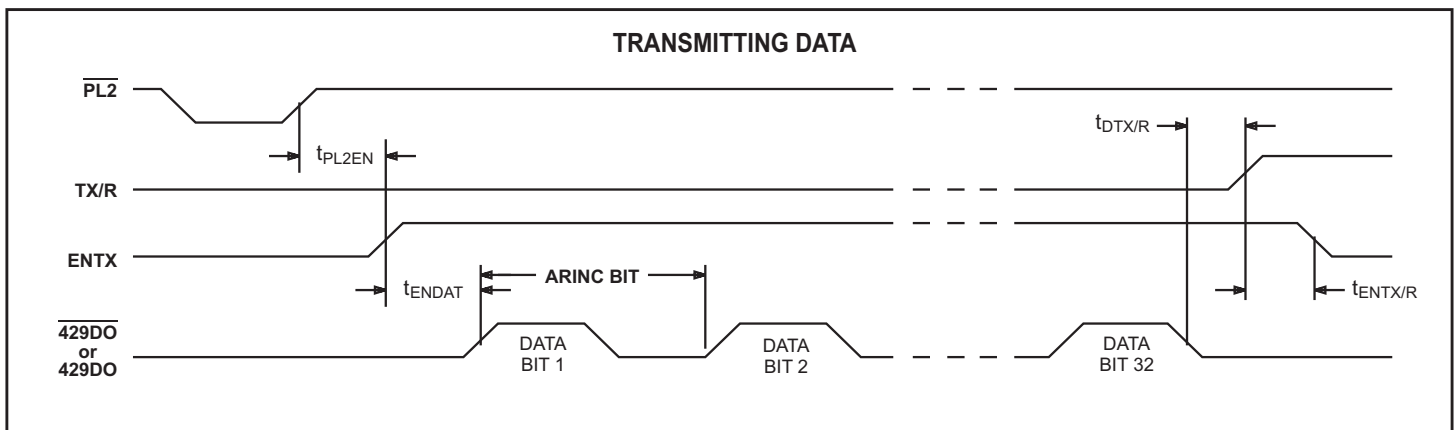
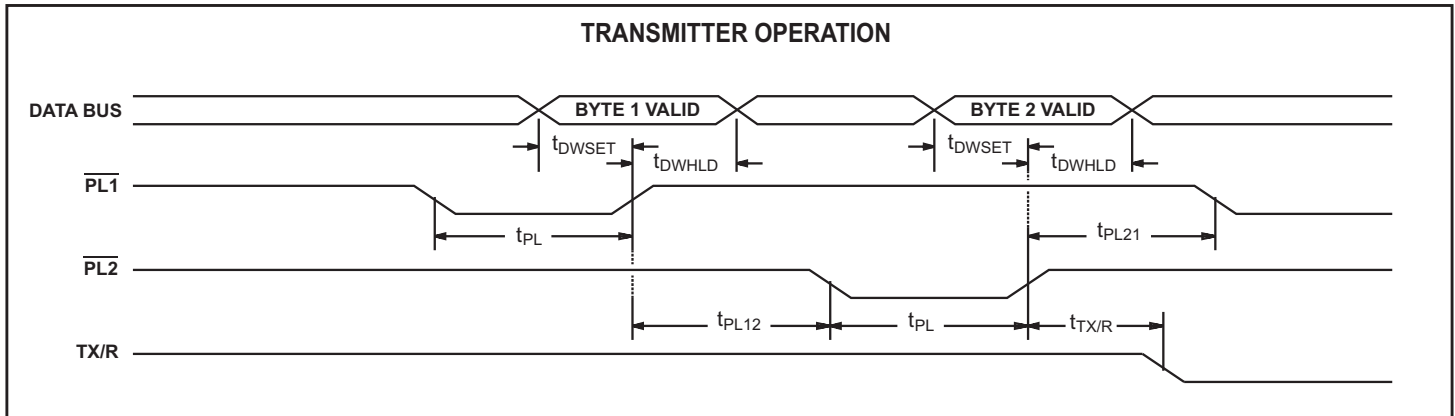
The diagram illustrates the timing relationship between the **DATA BUS** and the **CWSTR** (Control Word Strobe) signal during the loading of a control word.

- LOADING CONTROL WORD**: This label is positioned above the data bus signal.
- DATA BUS**: The signal is shown as a horizontal line that transitions from a high state to a low state, then back to high. The period during which the data is valid is indicated by a double-headed arrow labeled **VALID**.
- CWSTR**: This signal is shown as a horizontal line that transitions from a high state to a low state, then back to high. The duration of the low pulse is indicated by a double-headed arrow labeled **t<sub>CWSTR</sub>**.
- t<sub>CWSET</sub>**: This is the setup time, indicated by a double-headed arrow between the falling edge of the **CWSTR** signal and the start of the **VALID** data period.
- t<sub>CWHLD</sub>**: This is the hold time, indicated by a double-headed arrow between the end of the **VALID** data period and the rising edge of the **CWSTR** signal.

### RECEIVER OPERATION

The diagram illustrates the receiver operation timing. It shows the relationship between the ARINC DATA (BIT 31 and BIT 32), the DATA READY FLAG ( $\overline{D/R}$ ), the BYTE SELECT ( $\overline{SEL}$ ), the ENABLE BYTE ON BUS ( $\overline{EN}$ ), and the DATA BUS. The data bus shows two bytes of data, labeled "BYTE 1 VALID" and "BYTE 2 VALID". The timing parameters shown are  $t_{D/R}$ ,  $t_{END/R}$ ,  $t_{SELEN}$ ,  $t_{ENSEL}$ ,  $t_{ENEN}$ ,  $t_{D/REN}$ ,  $t_{DATAEN}$ , and  $t_{ENDATA}$ .

# TIMING DIAGRAMS (cont.)



## ABSOLUTE MAXIMUM RATINGS

|                                          |                        |                                                     |                 |
|------------------------------------------|------------------------|-----------------------------------------------------|-----------------|
| Supply Voltage $V_{CC}$ . . . . .        | -0.3V to +7V           | Power Dissipation . . . . .                         | 500mW           |
| Voltage at ARINC input pins . . . . .    | -120V to +120V         | Operating Temperature Range: (Industrial) . . . . . | -40°C to +85°C  |
| Voltage at any other pin . . . . .       | -0.3V to $V_{CC}+0.3V$ | (Extended) . . . . .                                | -55°C to +125°C |
| DC Current Drain per input pin . . . . . | 10mA                   | Storage Temperature Range: . . . . .                | -65°C to +150°C |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V \pm 5\%$ ,  $GND = 0V$ ,  $T_A$  = Operating Temperature Range (unless otherwise specified).

| PARAMETER                                         | SYMBOL                                               | CONDITIONS                        | LIMITS                                                                          |                      |                    | UNIT                |                                        |
|---------------------------------------------------|------------------------------------------------------|-----------------------------------|---------------------------------------------------------------------------------|----------------------|--------------------|---------------------|----------------------------------------|
|                                                   |                                                      |                                   | MIN                                                                             | TYP                  | MAX                |                     |                                        |
| ARINC INPUTS                                      |                                                      |                                   |                                                                                 |                      |                    |                     |                                        |
| Differential Input Voltage:                       | ONE<br>ZERO<br>NULL                                  | $V_{IH}$<br>$V_{IL}$<br>$V_{NUL}$ | Pins 2 to 3, 4 to 5: Common mode voltage less than $\pm 4V$ with respect to GND | 6.5<br>-13.0<br>-2.5 | 10.0<br>-10.0<br>0 | 13.0<br>-6.5<br>2.5 | V<br>V<br>V                            |
| Input Resistance:                                 | Differential<br>To GND<br>To Vcc                     | $R_I$<br>$R_G$<br>$R_H$           |                                                                                 | 12<br>12<br>12       | 27<br>27           |                     | K $\Omega$<br>K $\Omega$<br>k $\Omega$ |
| Input Current:                                    | Input Sink<br>Input Source                           | $I_{IH}$<br>$I_{IL}$              |                                                                                 | -450                 |                    | 200                 | $\mu A$<br>$\mu A$                     |
| Input Capacitance:<br>(Guaranteed but not tested) | Differential<br>To GND<br>To Vcc                     | $C_I$<br>$C_G$<br>$C_H$           | Pins 2 to 3, 4 to 5                                                             |                      |                    | 20<br>20<br>20      | pF<br>pF<br>pF                         |
| BI-DIRECTIONAL INPUTS                             |                                                      |                                   |                                                                                 |                      |                    |                     |                                        |
| Input Voltage:                                    | Input Voltage HI<br>Input Voltage LO                 | $V_{IH}$<br>$V_{IL}$              |                                                                                 | 2.1                  |                    | 0.7                 | V<br>V                                 |
| Input Current:                                    | Input Sink<br>Input Source                           | $I_{IH}$<br>$I_{IL}$              |                                                                                 | -1.5                 |                    | 1.5                 | $\mu A$<br>$\mu A$                     |
| ALL OTHER INPUTS                                  |                                                      |                                   |                                                                                 |                      |                    |                     |                                        |
| Input Voltage:                                    | Input Voltage HI<br>Input Voltage LO                 | $V_{IH}$<br>$V_{IL}$              |                                                                                 | 3.5                  |                    | 0.7                 | V<br>V                                 |
| Input Current:                                    | Input Sink<br>Input Source                           | $I_{IH}$<br>$I_{IL}$              |                                                                                 | -20                  |                    | 10                  | $\mu A$<br>$\mu A$                     |
| OUTPUTS                                           |                                                      |                                   |                                                                                 |                      |                    |                     |                                        |
| Output Voltage:                                   | Logic "1" Output Voltage<br>Logic "0" Output Voltage | $V_{OH}$<br>$V_{OL}$              | $I_{OH} = -1.5mA$<br>$I_{OL} = 1.8mA$                                           | 2.7                  |                    | 0.4                 | V<br>V                                 |
| Output Current:<br>(Bi-directional Pins)          | Output Sink<br>Output Source                         | $I_{OL}$<br>$I_{OH}$              | $V_{OUT} = 0.4V$<br>$V_{OUT} = V_{CC} - 0.4V$                                   | 3.0<br>1.5           |                    |                     | mA<br>mA                               |
| Output Current:<br>(All Other Outputs)            | Output Sink<br>Output Source                         | $I_{OL}$<br>$I_{OH}$              | $V_{OUT} = 0.4V$<br>$V_{OUT} = V_{CC} - 0.4V$                                   | 3.6<br>1.5           |                    |                     | mA<br>mA                               |
| Output Capacitance:                               |                                                      | $C_O$                             |                                                                                 |                      |                    | 15                  | pF                                     |
| SUPPLY INPUT                                      |                                                      |                                   |                                                                                 |                      |                    |                     |                                        |
| Standby Supply Current:                           |                                                      | $I_{CC1}$                         |                                                                                 |                      |                    | 20                  | mA                                     |
| Operating Supply Current:                         |                                                      | $I_{CC2}$                         |                                                                                 |                      |                    | 20                  | mA                                     |

# AC ELECTRICAL CHARACTERISTICS

V<sub>cc</sub> = 5V, GND = 0V, TA = Operating Temperature Range and f<sub>clk</sub> = 1MHz ±0.1% with 60/40 duty cycle

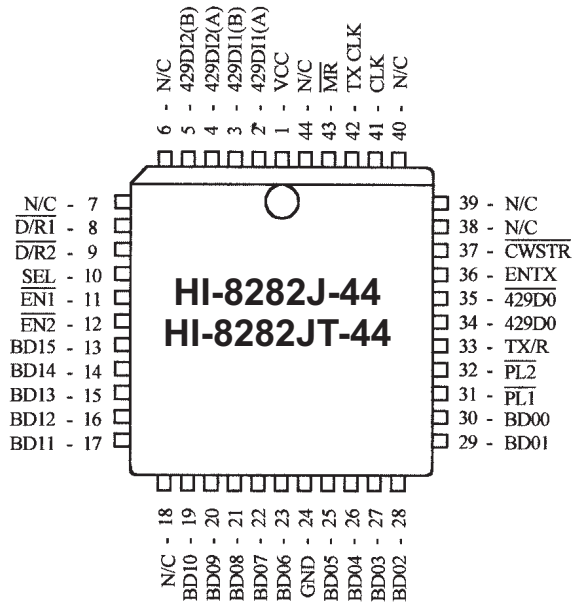
| PARAMETER                                                                                                                                | SYMBOL                     | LIMITS          |     |           | UNITS              |
|------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------|-----|-----------|--------------------|
|                                                                                                                                          |                            | MIN             | TYP | MAX       |                    |
| CONTROL WORD TIMING                                                                                                                      |                            |                 |     |           |                    |
| Pulse Width - $\overline{CWSTR}$<br>Setup - DATA BUS Valid to $\overline{CWSTR}$ HIGH<br>Hold - $\overline{CWSTR}$ HIGH to DATA BUS Hi-Z | tCWSTR<br>tCWSET<br>tCWHLd | 130<br>140<br>0 |     |           | ns<br>ns<br>ns     |
| RECEIVER TIMING                                                                                                                          |                            |                 |     |           |                    |
| Delay - Start ARINC 32nd Bit to $\overline{D/R}$ LOW: High Speed<br>Low Speed                                                            | tD/R<br>tD/R               |                 |     | 16<br>128 | $\mu$ s<br>$\mu$ s |
| Delay - $\overline{D/R}$ LOW to $\overline{EN}$ LOW<br>Delay - $\overline{EN}$ LOW to $\overline{D/R}$ HIGH                              | tD/REN<br>tEND/R           | 0               |     | 200       | ns<br>ns           |
| Setup - SEL to $\overline{EN}$ LOW<br>Hold - SEL to $\overline{EN}$ HIGH                                                                 | tSELEN<br>tENSEL           | 20<br>50        |     |           | ns<br>ns           |
| Delay - $\overline{EN}$ LOW to DATA BUS Valid<br>Delay - $\overline{EN}$ HIGH to DATA BUS Hi-Z                                           | tENDATA<br>tDATAEN         |                 |     | 200<br>30 | ns<br>ns           |
| Pulse Width - $\overline{EN1}$ or $\overline{EN2}$<br>Spacing - $\overline{EN}$ HIGH to next $\overline{EN}$ LOW                         | tEN<br>tENEN               | 240<br>50       |     |           | ns<br>ns           |
| FIFO TIMING                                                                                                                              |                            |                 |     |           |                    |
| Pulse Width - $\overline{PL1}$ or $\overline{PL2}$                                                                                       | tPL                        | 200             |     |           | ns                 |
| Setup - DATA BUS Valid to $\overline{PL}$ HIGH<br>Hold - $\overline{PL}$ HIGH to DATA BUS Hi-Z                                           | tDWSET<br>tDWHLD           | 110<br>20       |     |           | ns<br>ns           |
| Spacing - $\overline{PL1}$ to $\overline{PL2}$                                                                                           | tPL12                      | 0               |     |           | ns                 |
| Spacing - $\overline{PL2}$ to $\overline{PL1}$                                                                                           | tPL21                      | 250             |     |           | ns                 |
| Delay - $\overline{PL2}$ HIGH to TX/R LOW                                                                                                | tTX/R                      |                 |     | 840       | ns                 |
| TRANSMISSION TIMING                                                                                                                      |                            |                 |     |           |                    |
| Spacing - $\overline{PL2}$ HIGH to ENTX HIGH                                                                                             | tPL2EN                     | 0               |     |           | $\mu$ s            |
| Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): High Speed<br>Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): Low Speed                            | tENDAT<br>tENDAT           |                 |     | 25<br>200 | $\mu$ s<br>$\mu$ s |
| Delay - 32nd ARINC Bit to TX/R HIGH                                                                                                      | tDTX/R                     |                 |     | 400       | ns                 |
| Spacing - TX/R HIGH to ENTX LOW                                                                                                          | tENTX/R                    | 0               |     |           | ns                 |
| REPEATER OPERATION TIMING                                                                                                                |                            |                 |     |           |                    |
| Delay - $\overline{EN}$ LOW to $\overline{PL}$ LOW                                                                                       | tENPL                      | 0               |     |           | ns                 |
| Hold - $\overline{PL}$ HIGH to $\overline{EN}$ HIGH                                                                                      | tPLEN                      | 0               |     |           | ns                 |
| Delay - TX/R LOW to ENTX HIGH                                                                                                            | tTX/REN                    | 0               |     |           | ns                 |
| Master Reset Pulse Width                                                                                                                 | tMR                        | 400             |     |           | ns                 |
| ARINC Data Rate and Bit Timing                                                                                                           |                            |                 |     | $\pm 1\%$ |                    |



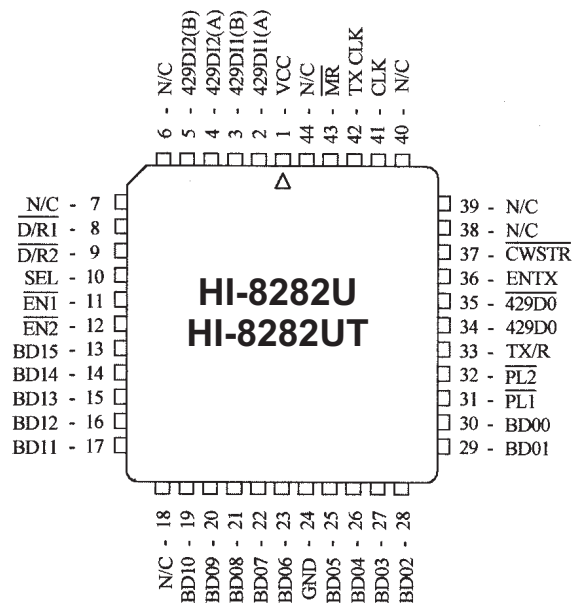
# ADDITIONAL HI-8282 PIN CONFIGURATIONS

(See page 1 for the 40-pin Ceramic Side-Brazed DIP Package )

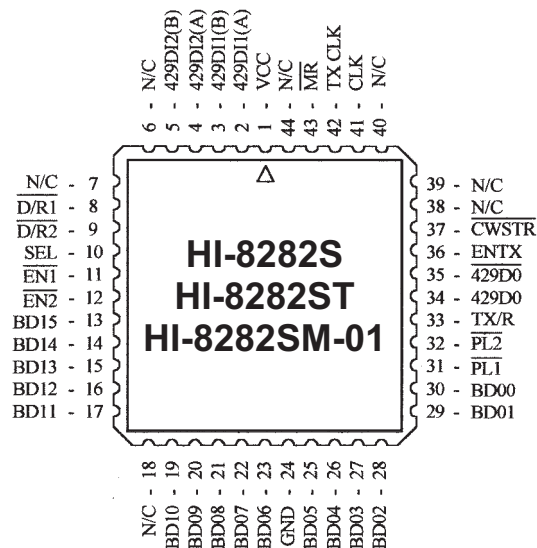
## 44-PIN PLASTIC PLCC



## 44-PIN J-LEAD CERQUAD



## 44-PIN CERAMIC LCC



## ORDERING INFORMATION

### HI - 8282 x x - xx (Ceramic)

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN | NOTES     |
|-------------|-------------------|------|---------|-----------|
| Blank       | -40°C to +85°C    | I    | No      |           |
| T           | -55°C to +125°C   | T    | No      |           |
| M-01        | -55°C to +125°C   | M    | Yes     | (1)       |
| M-03        | -55°C to +125°C   | DSCC | Yes     | (1) & (2) |

| PART NUMBER | PACKAGE DESCRIPTION                              | LEAD FINISH     | NOTES     |
|-------------|--------------------------------------------------|-----------------|-----------|
| C           | 40 PIN CERAMIC SIDE BRAZED DIP (40C)             | Gold            | (3) & (1) |
| S           | 44 PIN CERAMIC LEADLESS CHIP CARRIER (44S)       | Gold            | (3) & (1) |
| U           | 44 PIN CERQUAD (44U) not available with 'M' flow | Tin/Lead Solder |           |

Notes:

- (1) Process Flows M and DSCC always have Tin / Lead (Sn/Pb) solder lead finish.
- (2) DSSC SMD# 5962-8688002QA. Only available in 'C' package with Sn/Pb solder lead finish.
- (3) Gold terminal finish is Pb-Free, RoHS compliant.

### HI - 8282J x x - 44 (Plastic)

| PART NUMBER | LEAD FINISH                              |
|-------------|------------------------------------------|
| Blank       | Tin / Lead (Sn / Pb) Solder              |
| F           | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| Blank       | -40°C TO +85°C    | I    | No      |
| T           | -55°C TO +125°C   | T    | No      |

| PART NUMBER | PACKAGE DESCRIPTION                  |
|-------------|--------------------------------------|
| 8282J       | 44 PIN PLASTIC J LEAD (44J) Note (4) |

Notes:

- (4) NOT RECOMMENDED FOR NEW DESIGNS. The newer HI-8282APJI and HI-8282APJT replace the HI-8282J-44 and HI-8282JT-44 respectively.

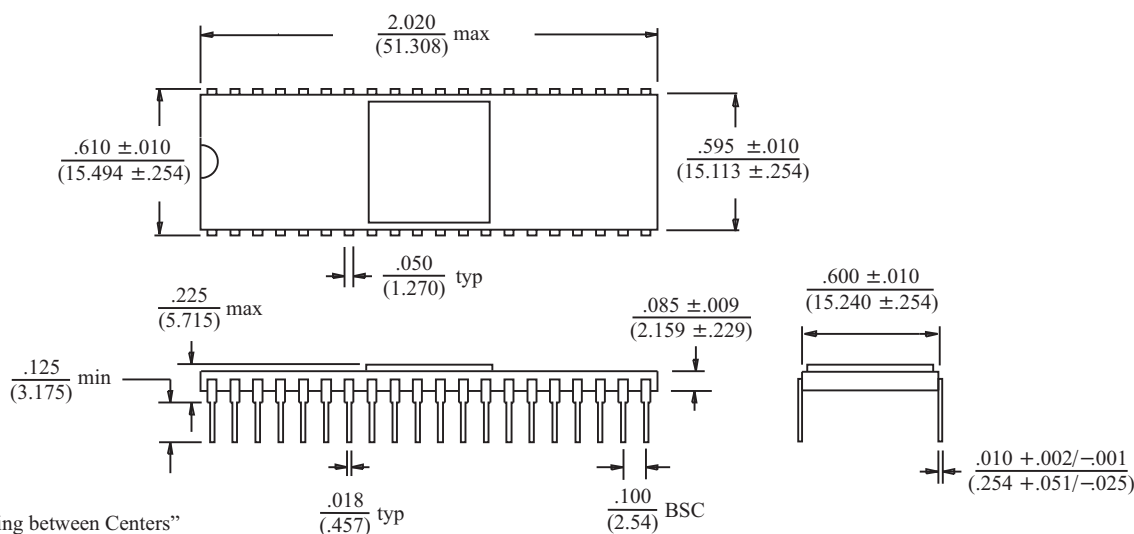
## REVISION HISTORY

| Revision       | Date     | Description of Change                                                                                                                    |
|----------------|----------|------------------------------------------------------------------------------------------------------------------------------------------|
| DS8282, Rev. G | 02/23/09 | Clarified the "T" temperature range. Clarified Note (4) in Ordering Information.                                                         |
| Rev. H         | 07/30/13 | Updated Bit Timing section (same as HI-8581) and Receiver Parity information. Update Voltage at ARINC input pins from +/-29V to +/-120V. |

### 40-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

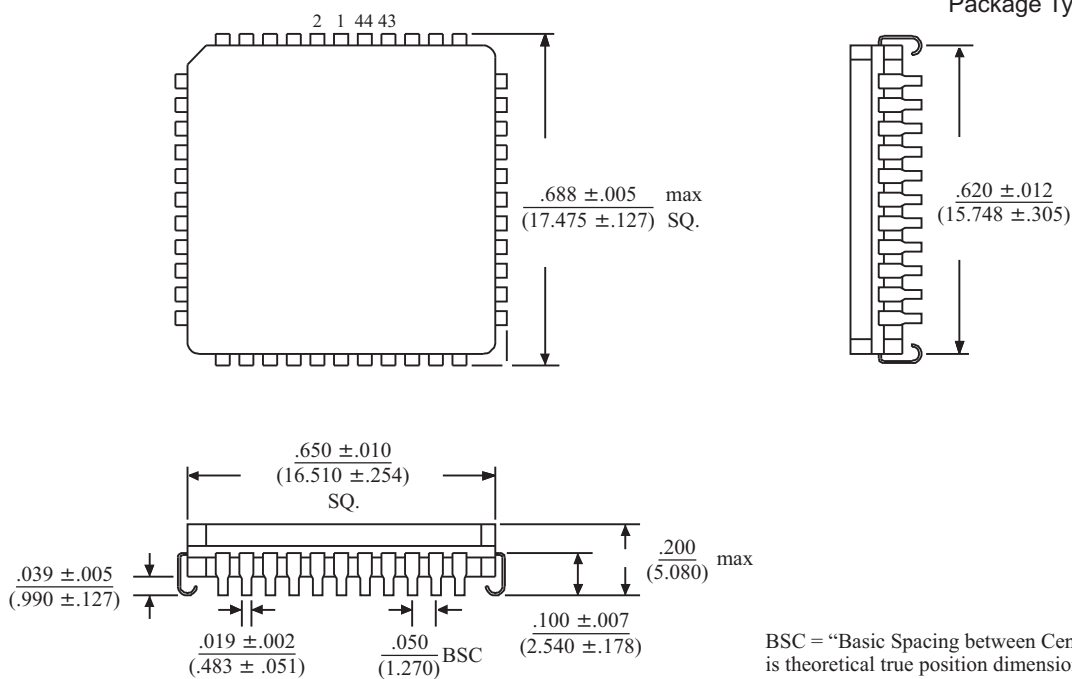
Package Type: 40C



### 44-PIN J-LEAD CERQUAD

inches (millimeters)

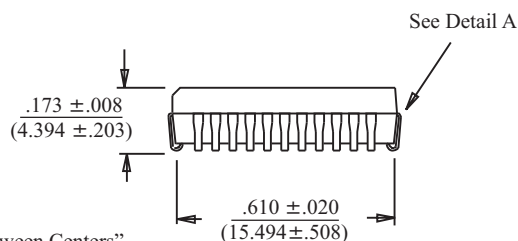
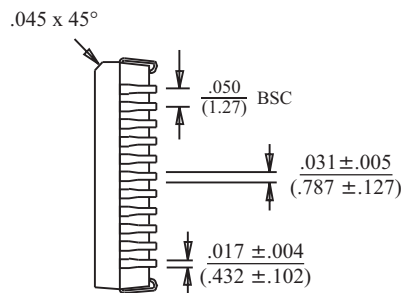
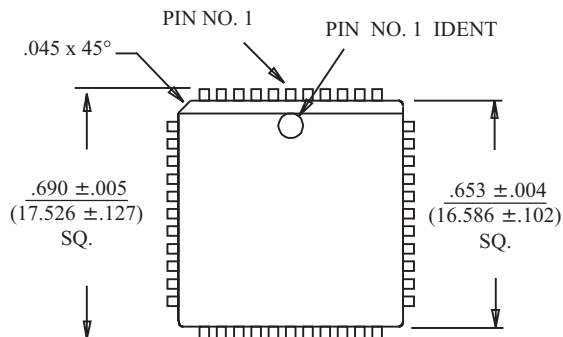
Package Type: 44U



### 44-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 44J

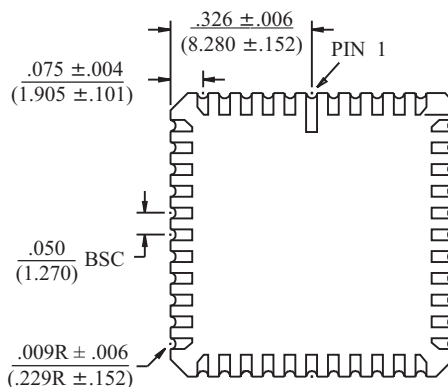
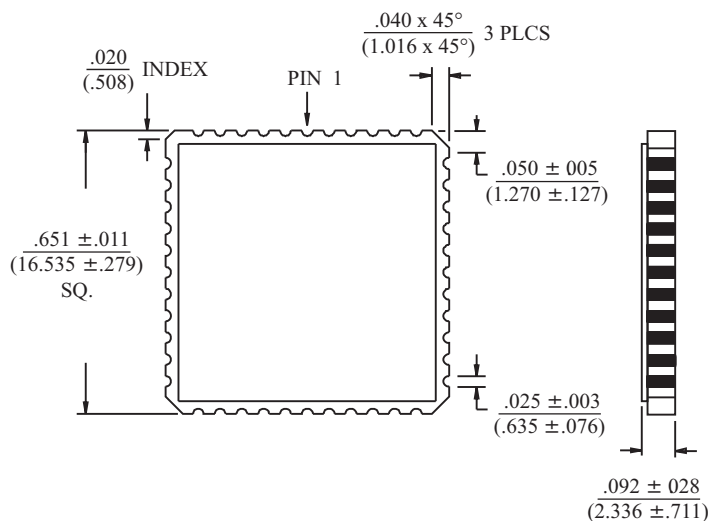


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

### 44-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 44S



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)