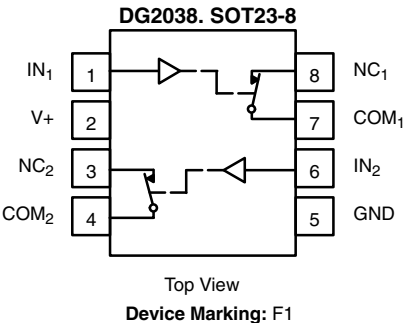
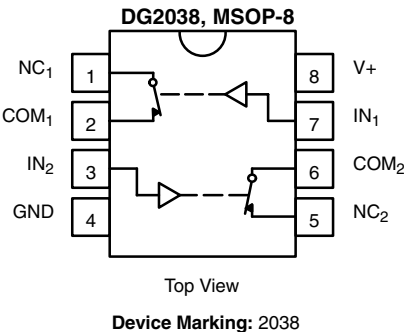




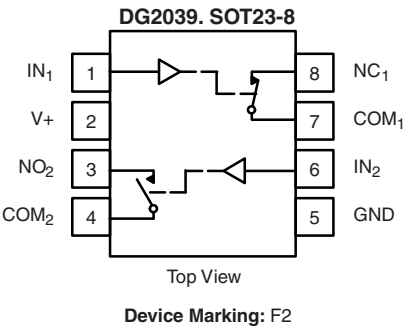
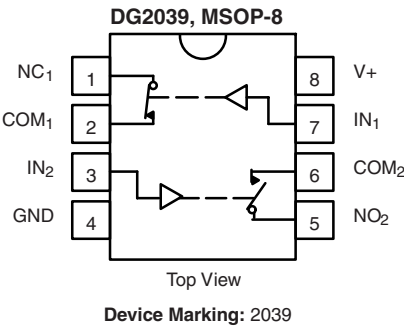
DG2037/2038/2039

Vishay Siliconix

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG2038/DG2039



TRUTH TABLE - DG2038	
Logic	Switch
0	On
1	Off



TRUTH TABLE - DG2039		
Logic	Switch-1	Switch-2
0	On	Off
1	Off	On

ORDERING INFORMATION		
Temp Range	Package	Part Number
- 40 to 85 °C	MSOP-8	DG2037DQ
		DG2038DQ
		DG2039DQ
	SOT23-8	DG2037DS
		DG2038DS
		DG2039DS

**ABSOLUTE MAXIMUM RATINGS**

Parameter		Limit	Unit
Referenced V+ to GND		- 0.3 to 6.0	V
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages) ^b	MSOP-8 ^c	320	mW
	SOT23-8 ^c	515	

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 6.5 mW/°C above 25 °C.

SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.4 or 1.5 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 1.5 V, I _{NO} , I _{NC} = 10 mA	Room Full		3	6 7	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 2.7 V, V _{COM} = 1.5 to V+, I _{NO} , I _{NC} = 10 mA	Room		0.5		
r _{ON} Match ^d	r _{ON} Match	V+ = 2.7 V, V _D = 1.5 to V+, I _D = 10 mA	Room		0.3		
Switch Off Leakage Current	I _{NO(off)} I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 1 V/3 V, V _{COM} = 3 V/1 V	Room Full	- 1 - 10		1 10	nA
	I _{COM(off)}		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 1 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V _{INH}		Full	1.5			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}	f = 1 MHz	Full		8		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2.0 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full		22	35 40	ns
Turn-Off Time	t _{OFF}		Room Full		17	31 35	
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		1		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk ^d	X _{TALK}		Room		- 67		
Source-Off Capacitance ^d	C _{NC/NO(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		17		pF
Drain-Off Capacitance ^d	C _{COM(off)}		Room		19		
Channel-On Capacitance ^d	C _{ON}		Room		35		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V _{IN} = 0 or V+			0.02	1.0	μA
Power Consumption	P _C					3.3	μW

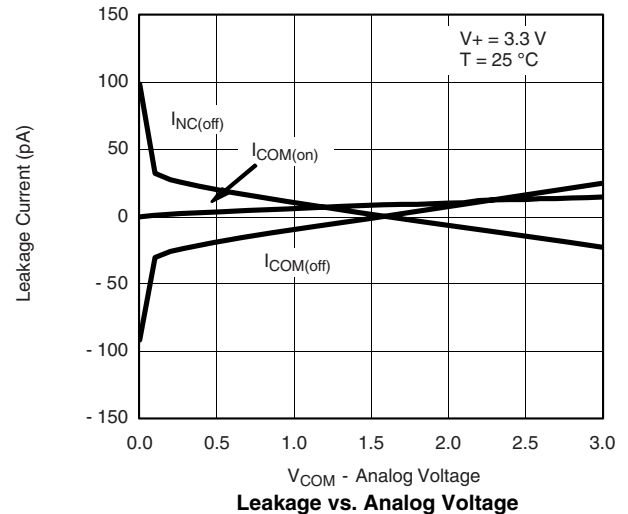
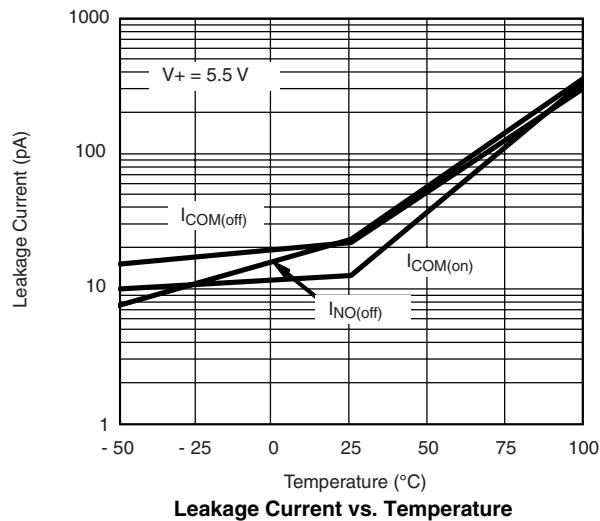
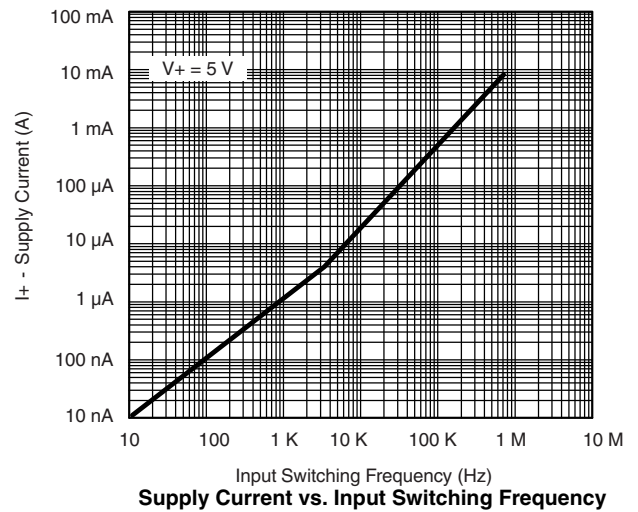
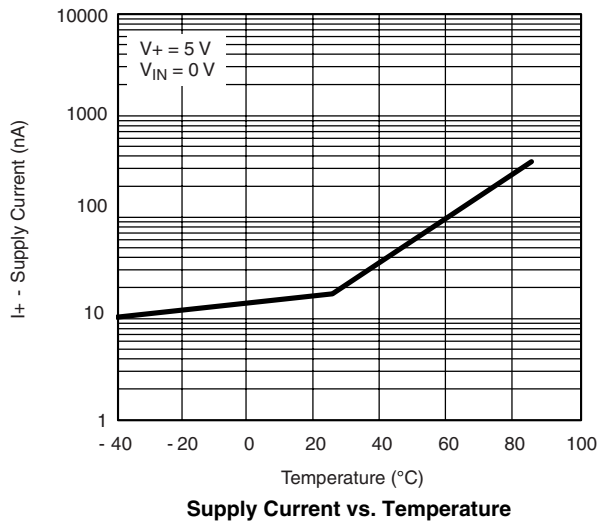
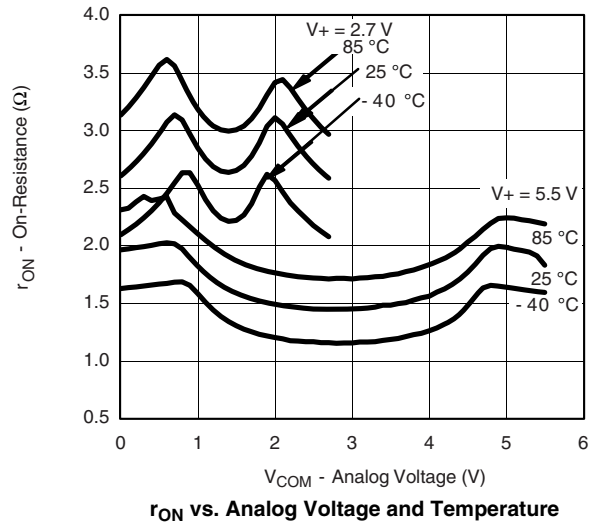
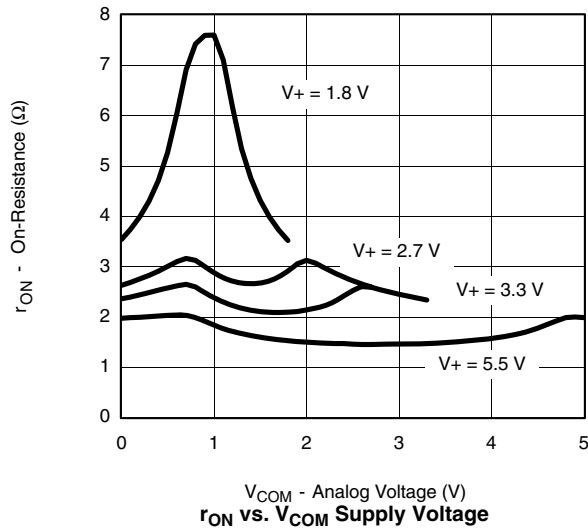


SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, VIN = 0.8 or 2.4 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 4.5 V, VCOM = 2.5 V, INO, INC = 10 mA	Room Full		2.5 1.6	5 6	Ω
rON Flatness ^d	rON Flatness	V+ = 4.5 V, VCOM = 2.5 to V+, INO, INC = 10 mA	Room		0.4		
rON Match ^d	rON Match	V+ = 4.5 V, ID = 10 mA, VCOM = 2.5 V	Room		0.2		
Switch Off Leakage Current	INO(off) INC(off)	V+ = 5.5 V VNO, VNC = 1 V/4.5 V, VCOM = 4.5 V/1 V	Room Full	- 1 - 10		1 10	nA
	ICOM(off)		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	ICOM(on)	V+ = 5.5 V VNO, VNC = VCOM = 1 V/4.5 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	VINH		Full	2.4			V
Input Low Voltage	VINL		Full			0.8	
Input Capacitance	Cin	f = 1 MHz	Full		8		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	tON	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF Figures 1 and 2	Room Full		19	30 35	ns
Turn-Off Time ^d	tOFF		Room Full		12	22 30	
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, Figure 3	Room		1		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk ^d	XTALK		Room		- 67		
Source-Off Capacitance ^d	CNC/NO(off)	VIN = 0 or V+, f = 1 MHz	Room		15		pF
Drain-Off Capacitance ^d	CCOM(off)		Room		17		
Channel-On Capacitance ^d	CON		Room		35		
Power Supply							
Power Supply Range	V+	VIN = 0 or V+		4.5		5.5	V
Power Supply Current	I+				0.02	1.0	μA
Power Consumption	PC					5.5	μW

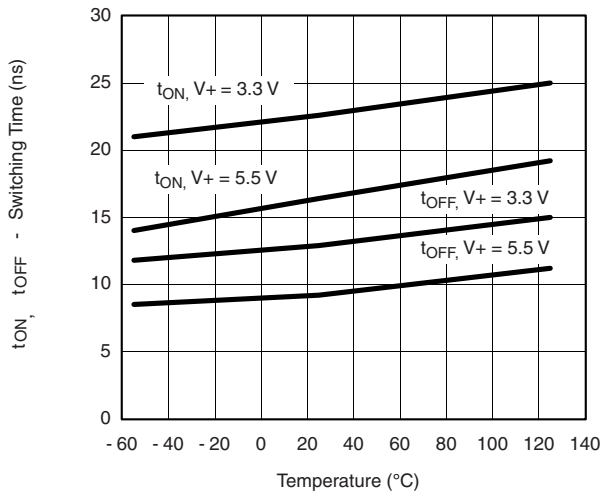
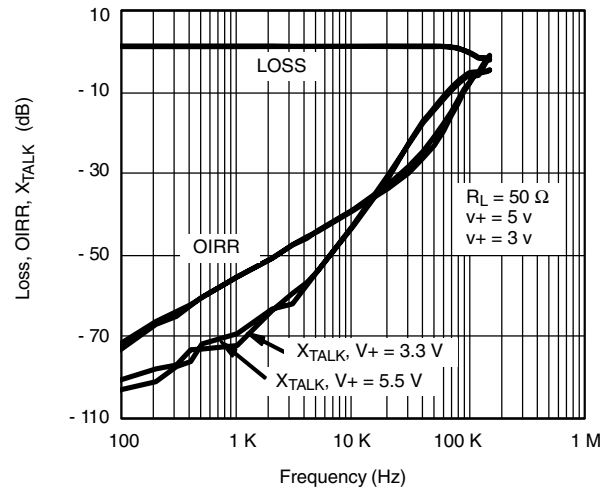
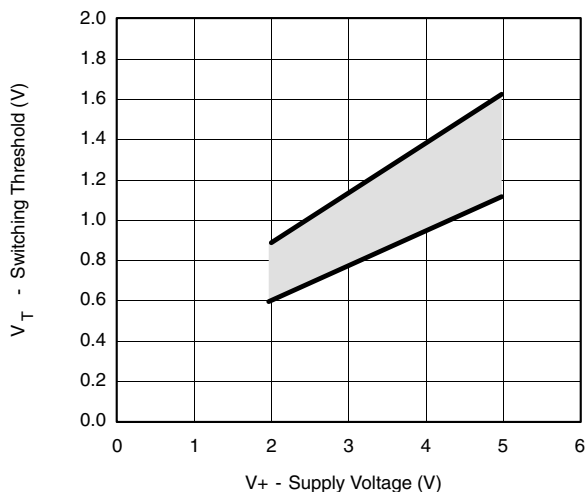
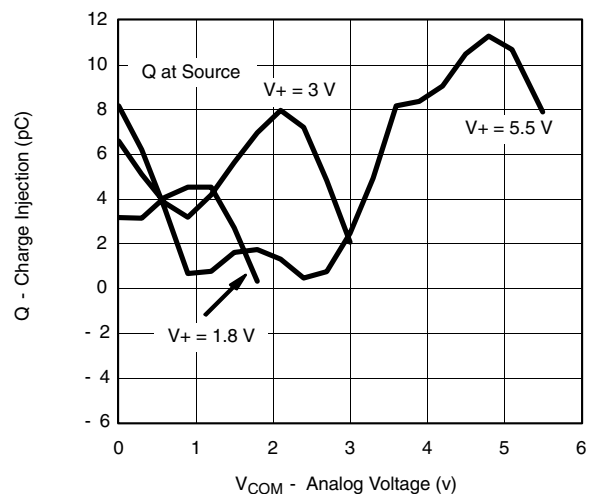
Notes:

- Room = 25 °C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Switching Time vs. Temperature and Supply Voltage****Insertion Loss, Off-Isolation Crosstalk vs. Frequency****Switching Threshold vs. Supply Voltage****Charge Injection vs. Analog Voltage**

TEST CIRCUITS

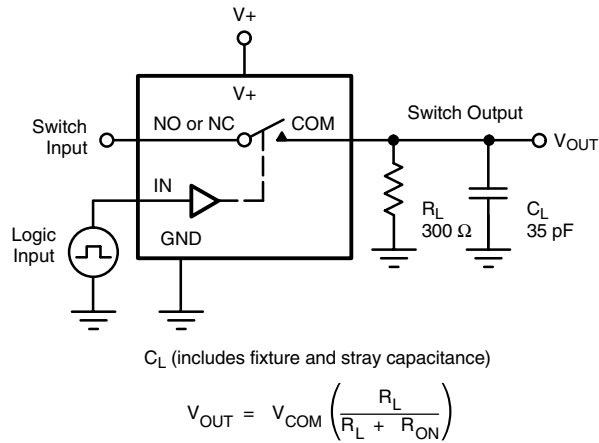
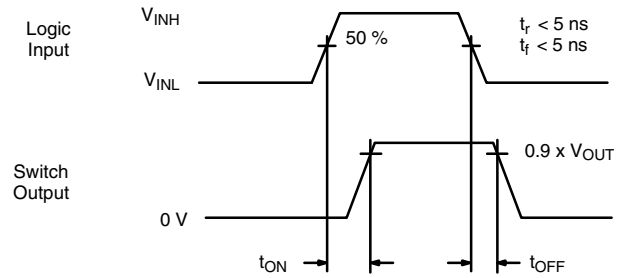
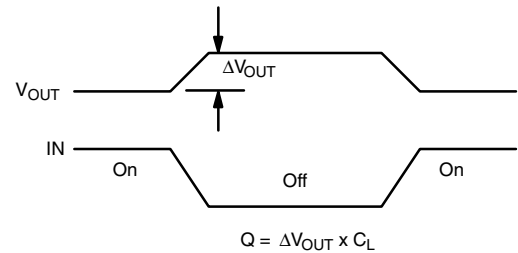
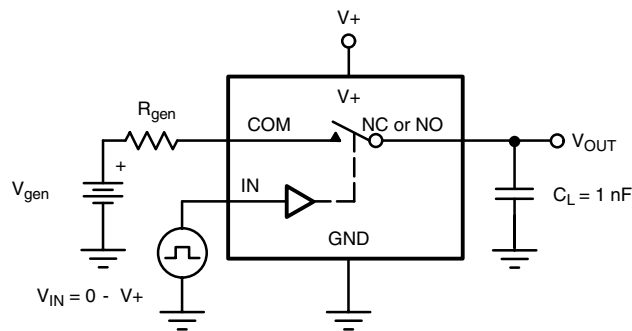


Figure 1. Switching Time



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection

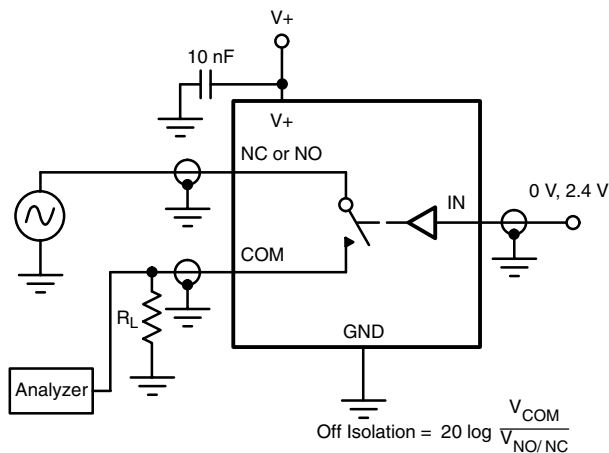


Figure 3. Off-Isolation

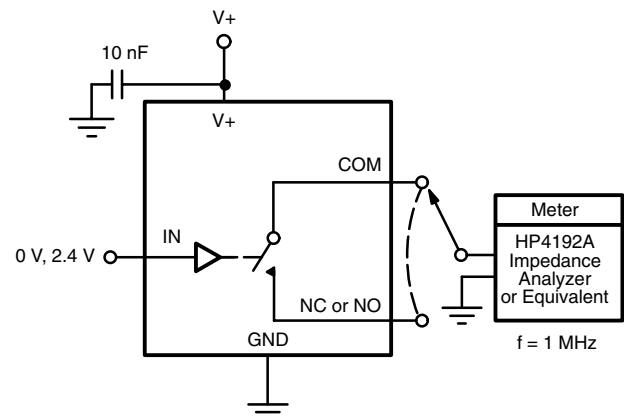


Figure 4. Channel Off/On Capacitance

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