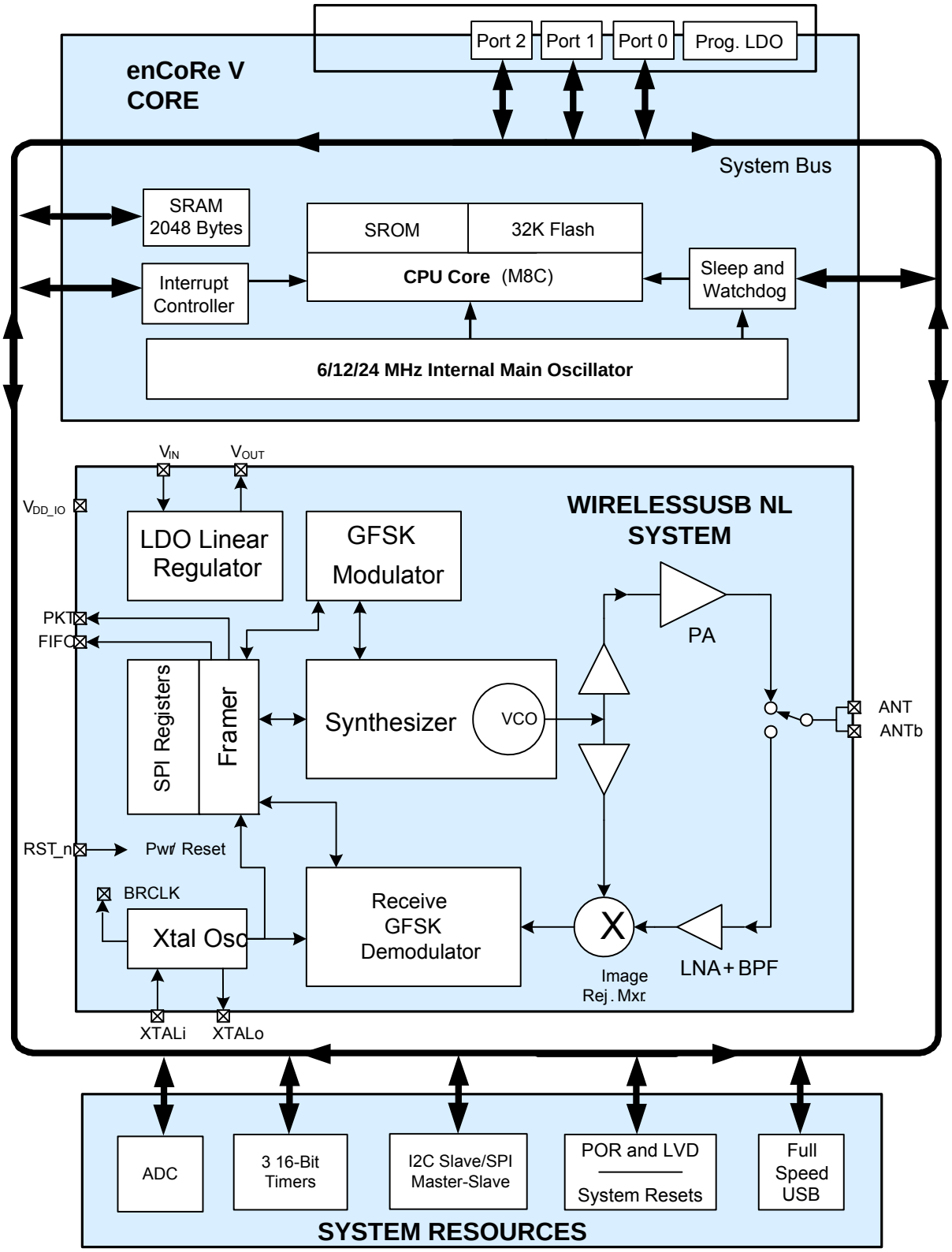
PRoC-USB Logical Block Diagram



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Functional Overview

The enCoRe V family of devices are designed to replace multiple traditional full-speed USB microcontroller system components with one, low cost single-chip programmable component. Communication peripherals (I^2C/SPI), a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in the PRoC-USB Logical Block Diagram on page 2, consists of three main areas: the CPU core, the WirelessUSB™ NL subsystem and the system resources.

This product is an enhanced version of Cypress's successful full speed-USB peripheral controllers. Enhancements include faster CPU at lower voltage operation, lower current consumption, twice the RAM and flash, hot-swappable I/Os, I^2C hardware address recognition, new very low current sleep mode, and new package options.

The enCoRe V Core

The enCoRe V Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

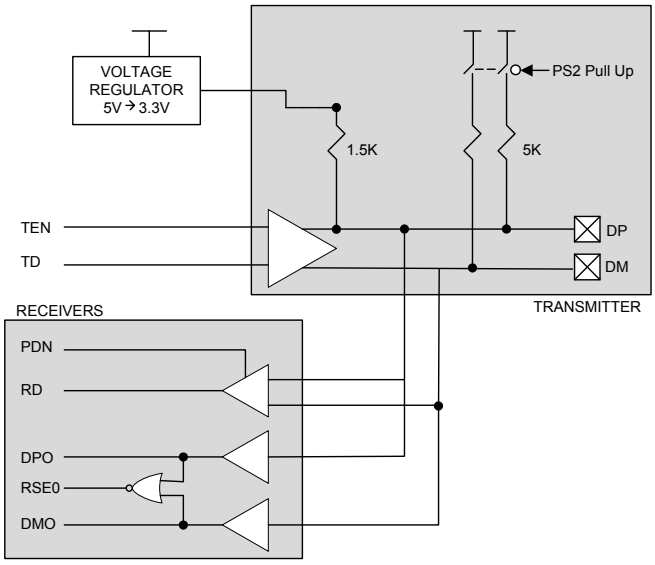
System resources provide additional capability, such as a configurable I^2C slave and SPI master-slave communication interface and various system resets supported by the M8C.

Full-Speed USB

The enCoRe V USB system resource adheres to the USB 2.0 Specification for full-speed devices operating at 12 Mb/second with one upstream port and one USB address. enCoRe V USB consists of these components:

- Serial interface engine (SIE) block.
- PSoC memory arbiter (PMA) block.
- 512 bytes of dedicated SRAM.
- A full-speed USB Transceiver with internal regulator and two dedicated USB pins.

Figure 1. USB Transceiver Regulator



At the enCoRe V system level, the full-speed USB system resource interfaces to the rest of the enCoRe V by way of the M8C's register access instructions and to the outside world by way of the two USB pins. The SIE supports nine endpoints including a bidirectional control endpoint (endpoint 0) and eight unidirectional data endpoints (endpoints 1 to 8). The unidirectional data endpoints are individually configurable as either IN or OUT.

The USB serial interface engine (SIE) allows the enCoRe V device to communicate with the USB host at full-speed data rates (12 Mb/s). The SIE simplifies the interface to USB traffic by automatically handling the following USB processing tasks without firmware intervention:

- Translates the encoded received data and formats the data to be transmitted on the bus.
- Generates and checks cyclical redundancy checks (CRCs). Incoming packets failing checksum verification are ignored.
- Checks addresses. Ignores all transactions not addressed to the device.
- Sends appropriate ACK/NAK/Stall handshakes.
- Identifies token type (SETUP, IN, OUT) and sets the appropriate token bit once a valid token in received.
- Identifies Start-of-Frame (SOF) and saves the frame count.
- Sends data to or retrieves data from the USB SRAM, by way of the PSoC Memory Arbiter (PMA).

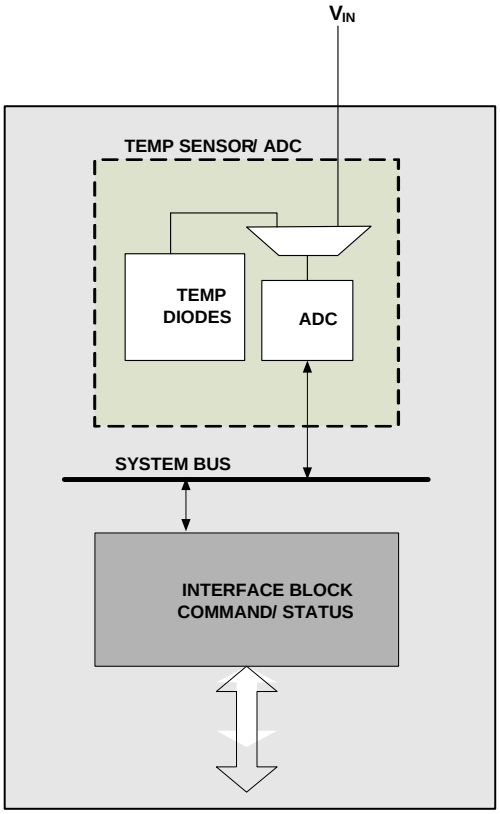
Firmware is required to handle various parts of the USB interface. The SIE issues interrupts after key USB events to direct firmware to appropriate tasks:

- Fill and empty the USB data buffers in USB SRAM.
- Enable PMA channels appropriately.
- Coordinate enumeration by decoding USB device requests.
- Suspend and resume coordination.
- Verify and select data toggle values.

10-bit ADC

The ADC on enCoRe V device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog mux bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 2. ADC System Performance Block Diagram



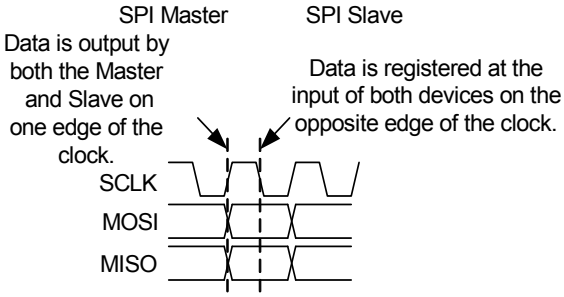
The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the analog global input mux or the temperature sensor with an input voltage range of 0 V to V_{REFADC}.

In the ADC only configuration (the ADC MUX selects the Analog mux bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the desired resolution of the ADC. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

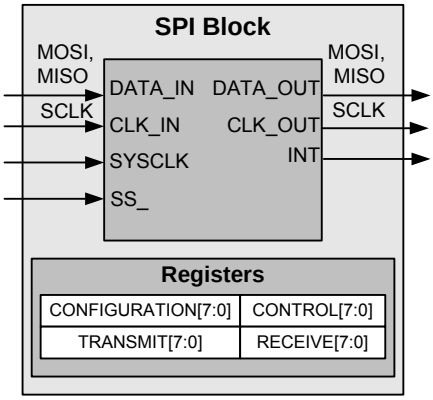
Figure 3. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 4. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed, and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is dependent on the application and enCoRe V device and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions:

- To allow for the selection of a given slave in a multi-slave environment.
- To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I²C slave enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing. The basic I²C features include:

- Slave, transmitter, and receiver operation.
- Byte processing for low CPU overhead.
- Interrupt or polling CPU interface.
- Support for clock rates of up to 400 kHz.
- 7- or 10-bit addressing (through firmware support).
- SMBus operation (through firmware support).

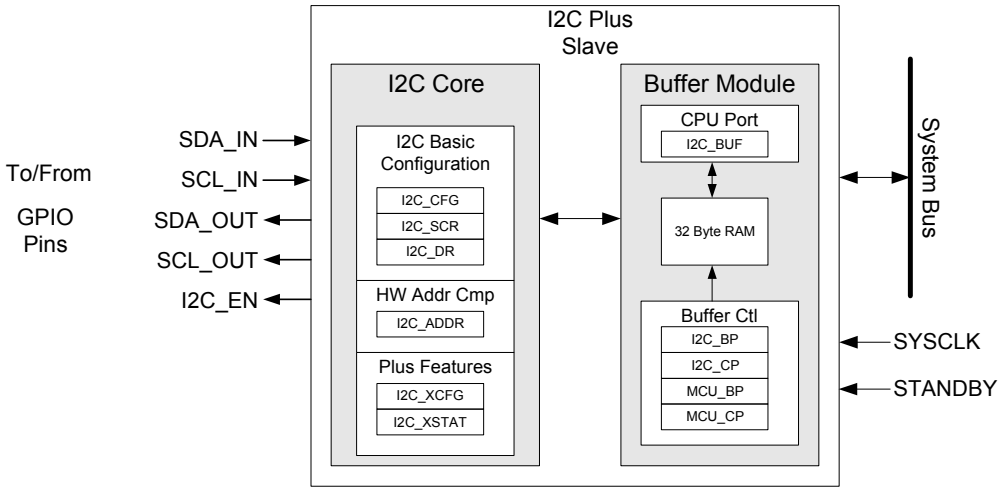
Enhanced features of the I²C Slave Enhanced Module include:

- Support for 7-bit hardware address compare.
- Flexible data buffering schemes.
- A "no bus stalling" operating mode.
- A low power bus monitoring mode.

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Figure 5. I²C Block Diagram



WirelessUSB-NL Subsystem

WirelessUSB-NL, optimized to operate in the 2.4-GHz ISM band, is Cypress's third generation of 2.4-GHz low-power RF technology. WirelessUSB-NL implements a Gaussian frequency-shift keying (GFSK) radio using a differentiated single-mixer, closed-loop modulation design that optimizes power efficiency and interference immunity. Closed-loop modulation effectively eliminates the problem of frequency drift, enabling WirelessUSB-NL to transmit up to 255-byte payloads without repeatedly having to pay power penalties for re-locking the phase-locked loop (PLL) as in open-loop designs

Among the advantages of WirelessUSB-NL are its fast lock times and channel switching, along with the ability to transmit larger payloads. Use of longer payload packets, compared to multiple short payload packets, can reduce overhead, improve overall power efficiency, and help alleviate spectrum crowding.

Combined with Cypress's enCoRe V based full-speed USB controllers, WirelessUSB-NL also provides the lowest bill of materials (BOM) cost solution for sophisticated PC peripheral applications such as wireless keyboards and mice, as well as best-in-class wireless performance in other demanding applications, such as toys, remote controls, fitness, automation, presenter tools, and gaming.

With PRoC-USB, the WirelessUSB-NL transceiver can add wireless capability to a wide variety of full speed USB applications.

The WirelessUSB-NL is a fully-integrated CMOS RF transceiver, GFSK data modem, and packet framer, optimized for use in the 2.4-GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver uses extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

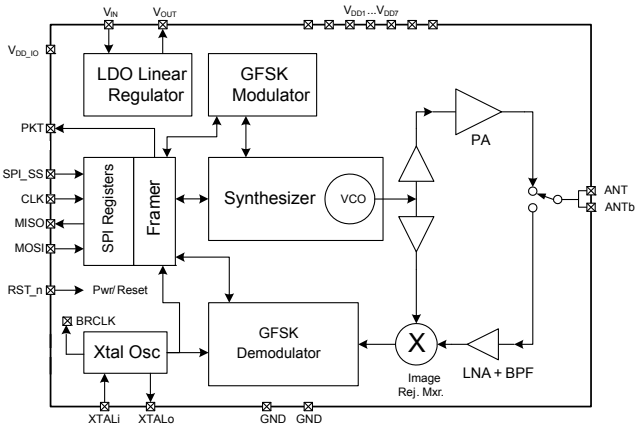
The product transmits GFSK data at approximately 0-dBm output power. Sigma-Delta PLL delivers high-quality DC-coupled transmit data path.

The low-IF receiver architecture produces good selectivity and image rejection, with typical sensitivity of –87 dBm or better on most channels. Sensitivity on channels that are integer multiples of the crystal reference oscillator frequency (12 MHz) may show approximately 5 dB degradation. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

For more details on the radio's implementation details and timing requriements, please go through the WirelessUSB-NL datasheet in www.cypress.com.

Figure 6. WirelessUSB-NL logic Block Diagram



Transmit Power Control

The following table lists recommended settings for register 9 for short-range applications, where reduced transmit RF power is a desirable trade off for lower current.

Table 1. Transmit Power Control

Power Setting Description	Typical Transmit Power (dBm)	Value of Register 9	
		Silicon ID 0x1002	Silicon ID 0x2002
PA0 - Highest power	+1	0x1820	0x7820
PA2 - High power	0	0x1920	0x7920
PA4 - High power	–3	0x1A20	0x7A20
PA8 - Low power	–7.5	0x1C20	0x7C20
PA12 - Lower power	–11.2	0x1E20	0x7E20

Note: Silicon ID can be read from Register 31.

Power-on and Register Initialization Sequence

For proper initialization at power up, V_{IN} must ramp up at the minimum overall ramp rate no slower than shown by T_{VIN} specification in the following figure. During this time, the RST_n line must track the V_{IN} voltage ramp-up profile to within approximately 0.2 V. Since most MCU GPIO pins automatically default to a high-Z condition at power up, it only requires a pull-up resistor. When power is stable and the MCU POR releases, and MCU begins to execute instructions, RST_n must then be pulsed low as shown in Figure 18 on page 39, followed by writing Reg 27 = 0x4200. During or after this SPI transaction, the State Machine status can be read to confirm FRAMER_ST = 1, indicating a proper initialization.

Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low-voltage detection and power-on reset. The following statements describe the merits of each system resource.

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 5 V maximum input, 1.8, 2.5, or 3 V selectable output, LDO regulator provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V family of parts.

Getting Started

The quickest path to understanding the PRoC-USB silicon is by reading this data sheet and using the PSoC® Designer™ integrated development environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, see the enCoRe™ V CY7C643xx, enCoRe™ V LV CY7C604xx Technical Reference Manual (TRM) for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC development kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, including Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to http://www.cypress.com and look for CYPros Consultants.

Solutions Library

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Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Device Programmers

Firmware needs to be downloaded to PRoC USB device only at 3.3 V using Miniprog3 Programmer. This Programmer kit can be purchased from Cypress Store using part# ‘CY8CKIT-002 - MiniProg3’. It is a small, compact programmer which connects PC via a USB 2.0 cable (provided along with CY8cKIT-002)

Note: MiniProg1 Programmer should not be used as it does not support programming at 3.3 V.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called user modules. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse-width modulator (PWM) user module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

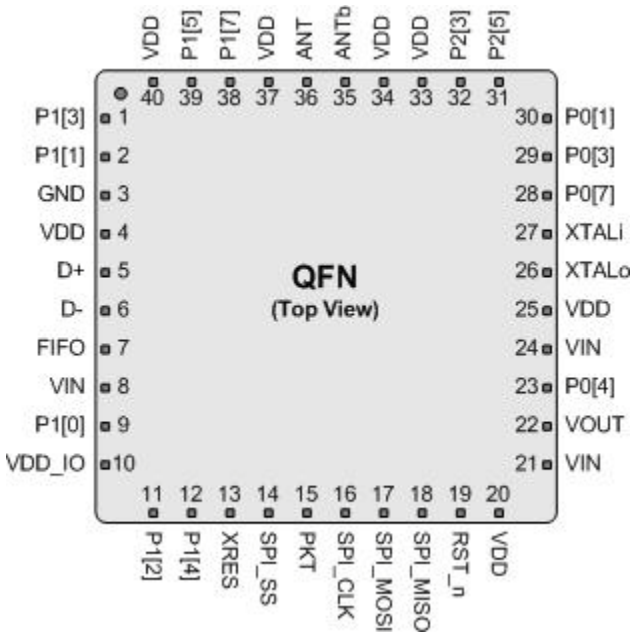
A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pin Configuration

The PRoC-USB device is available in a 40-pin QFN package, which is illustrated in the subsequent tables.

Figure 7. 40-pin QFN pinout



Pin Definitions

Pin No	Pin name	Pin Description
1	P1[3]/SCLK	Digital I/O, Analog I/O, SPI CLK
2	P1[1]/MOSI [1, 2]	Digital I/O, Analog I/O, TC CLK, I2C SCL, SPI MOSI
3	GND	Ground connection
4, 20, 25, 33, 34, 37	V_{DD}	Core power supply voltage. Connect all V_{DD} pins to VOUT pin.
5	D+	USB PHY, Digital I/O
6	D-	USB PHY, Digital I/O
7	FIFO	FIFO status indicator bit
8, 21, 24	VIN	Unregulated input voltage to the on-chip low drop out (LDO) voltage regulator
9	P1[0] [1, 2]	Analog I/O, Digital I/O, TC DATA, I^2C SDA
10	VDD_IO	VDD for the digital interface
11	P1[2]	Analog I/O, Digital I/O
12	P1[4]	Analog I/O, Digital I/O, EXT CLK
13	XRES	Active high external reset with internal pull-down
14	SPI_SS	Enable input for SPI, active low. Also used to bring device out of sleep state.
15	PKT	Transmit/receive packet status indicator bit
16	SPI_CLK	Clock input for SPI interface
17	SPI_MOSI	Data input for the SPI bus
18	SPI_MISO	Data output (tristate when not active)
19	RST_n	RST_n Low: Chip shutdown to conserve power. Register values lost RST_n High: Turn on chip, registers restored to default value
22	VOUT	1.8 V output from on-chip LDO. Connect to all V_{DD} pins, do not connect to external loads.
23	P0[4]	Analog I/O, Digital I/O, VREF
26	XTALO	Output of the crystal oscillator gain block
27	XTALI	Input to the crystal oscillator gain block
28	P0[7]	Analog I/O, Digital I/O,SPI CLK
29	P0[3]	Analog I/O, Digital I/O, Integrating input
30	P0[1]	Analog I/O, Digital I/O, Integrating input
31	P2[5]	Analog I/O, Digital I/O, XTAL Out
32	P2[3]	Analog I/O, Digital I/O, XTAL In
35	ANTb	Differential RF input/output. Each of these pins must be DC grounded, 20 kΩ or less
36	ANT	Differential RF input/output. Each of these pins must be DC grounded, 20 kΩ or less
38	P1[7]/SS_N	Digital I/O, Analog I/O, I^2C SCL, SPI SS
39	P1[5]/MISO	Digital I/O, Analog I/O, I^2C SDA, SPI MISO
40	VDD	Core power supply voltage. Connect all V_{DD} pins to VOUT pin.

Notes
1. During power up or reset event, device P1[0] and P1[1] may disturb the I^2C bus. Use alternate pins if issues are encountered.
2. These are the in-system serial programming (ISSP) pins that are not High Z at power-on reset (POR).

Register Reference

The section discusses the registers of the enCoRe V device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 2. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Table 3. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	EP1_CNT0	40	#		80			C0	
PRT0IE	01	RW	EP1_CNT1	41	RW		81			C1	
	02		EP2_CNT0	42	#		82			C2	
	03		EP2_CNT1	43	RW		83			C3	
PRT1DR	04	RW	EP3_CNT0	44	#		84			C4	
PRT1IE	05	RW	EP3_CNT1	45	RW		85			C5	
	06		EP4_CNT0	46	#		86			C6	
	07		EP4_CNT1	47	RW		87			C7	
PRT2DR	08	RW	EP5_CNT0	48	#		88		I2C_XCFG	C8	RW
PRT2IE	09	RW	EP5_CNT1	49	RW		89		I2C_XSTAT	C9	R
	0A		EP6_CNT0	4A	#		8A		I2C_ADDR	CA	RW
	0B		EP6_CNT1	4B	RW		8B		I2C_BP	CB	R
PRT3DR	0C	RW	EP7_CNT0	4C	#		8C		I2C_CP	CC	R
PRT3IE	0D	RW	EP7_CNT1	4D	RW		8D		CPU_BP	CD	RW
	0E		EP8_CNT0	4E	#		8E		CPU_CP	CE	R
	0F		EP8_CNT1	4F	RW		8F		I2C_BUF	CF	RW
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18		PMA0_DR	58	RW		98		I2C_DR	D8	RW
	19		PMA1_DR	59	RW		99			D9	
	1A		PMA2_DR	5A	RW		9A		INT_CLR0	DA	RW
	1B		PMA3_DR	5B	RW		9B		INT_CLR1	DB	RW
	1C		PMA4_DR	5C	RW		9C		INT_CLR2	DC	RW
	1D		PMA5_DR	5D	RW		9D			DD	
	1E		PMA6_DR	5E	RW		9E		INT_MSK2	DE	RW
	1F		PMA7_DR	5F	RW		9F		INT_MSK1	DF	RW
	20			60			A0		INT_MSK0	E0	RW
	21			61			A1		INT_SW_EN	E1	RW
	22			62			A2		INT_VC	E2	RC
	23			63			A3		RES_WDT	E3	W
	24		PMA8_DR	64	RW		A4			E4	
	25		PMA9_DR	65	RW		A5			E5	
	26		PMA10_DR	66	RW		A6			E6	
	27		PMA11_DR	67	RW		A7			E7	
	28		PMA12_DR	68	RW		A8			E8	
SPI_TXR	29	W	PMA13_DR	69	RW		A9			E9	
SPI_RXR	2A	R	PMA14_DR	6A	RW		AA			EA	
SPI_CR	2B	#	PMA15_DR	6B	RW		AB			EB	
	2C		TMP_DR0	6C	RW		AC			EC	
	2D		TMP_DR1	6D	RW		AD			ED	
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		PT0_CFG	B0	RW		F0	
USB_SOF0	31	R		71		PT0_DATA1	B1	RW		F1	
USB_SOF1	32	R		72		PT0_DATA0	B2	RW		F2	
USB_CR0	33	RW		73		PT1_CFG	B3	RW		F3	
USBIO_CR0	34	#		74		PT1_DATA1	B4	RW		F4	
USBIO_CR1	35	#		75		PT1_DATA0	B5	RW		F5	
EP0_CR	36	#		76		PT2_CFG	B6	RW		F6	
EP0_CNT0	37	#		77		PT2_DATA1	B7	RW	CPU_F	F7	RL
EP0_DR0	38	RW		78		PT2_DATA0	B8	RW		F8	
EP0_DR1	39	RW		79			B9			F9	
EP0_DR2	3A	RW		7A			BA			FA	
EP0_DR3	3B	RW		7B			BB			FB	
EP0_DR4	3C	RW		7C			BC			FC	
EP0_DR5	3D	RW		7D			BD			FD	
EP0_DR6	3E	RW		7E			BE		CPU_SCR1	FE	#
EP0_DR7	3F	RW		7F			BF		CPU_SCR0	FF	#

Gray fields are reserved; do not access these fields. # Access is bit specific.

Table 4. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA4_RA	40	RW		80			C0	
PRT0DM1	01	RW	PMA5_RA	41	RW		81			C1	
	02		PMA6_RA	42	RW		82			C2	
	03		PMA7_RA	43	RW		83			C3	
PRT1DM0	04	RW	PMA8_WA	44	RW		84			C4	
PRT1DM1	05	RW	PMA9_WA	45	RW		85			C5	
	06		PMA10_WA	46	RW		86			C6	
	07		PMA11_WA	47	RW		87			C7	
PRT2DM0	08	RW	PMA12_WA	48	RW		88			C8	
PRT2DM1	09	RW	PMA13_WA	49	RW		89			C9	
	0A		PMA14_WA	4A	RW		8A			CA	
	0B		PMA15_WA	4B	RW		8B			CB	
PRT3DM0	0C	RW	PMA8_RA	4C	RW		8C			CC	
PRT3DM1	0D	RW	PMA9_RA	4D	RW		8D			CD	
	0E		PMA10_RA	4E	RW		8E			CE	
	0F		PMA11_RA	4F	RW		8F			CF	
PRT4DM0	10	RW	PMA12_RA	50	RW		90			D0	
PRT4DM1	11	RW	PMA13_RA	51	RW		91			D1	
	12		PMA14_RA	52	RW		92		EC0_ENBUS	D2	RW
	13		PMA15_RA	53	RW		93		EC0_TRIM	D3	RW
	14		EP1_CR0	54	#		94			D4	
	15		EP2_CR0	55	#		95			D5	
	16		EP3_CR0	56	#		96			D6	
	17		EP4_CR0	57	#		97			D7	
	18		EP5_CR0	58	#		98		MUX_CR0	D8	RW
	19		EP6_CRO	59	#		99		MUX_CR1	D9	RW
	1A		EP7_CR0	5A	#		9A		MUX_CR2	DA	RW
	1B		EP8_CR0	5B	#		9B		MUX_CR3	DB	RW
	1C			5C			9C		IO_CFG1	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E		IO_CFG2	DE	RW
	1F			5F			9F		MUX_CR4	DF	RW
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
USB_CR1	30	#		70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
PMA0_WA	34	RW		74			B4			F4	
PMA1_WA	35	RW		75			B5			F5	
PMA2_WA	36	RW		76			B6			F6	
PMA3_WA	37	RW		77			B7		CPU_F	F7	RL
PMA4_WA	38	RW		78			B8			F8	
PMA5_WA	39	RW		79			B9			F9	
PMA6_WA	3A	RW		7A			BA		IMO_TR1	FA	RW
PMA7_WA	3B	RW		7B			BB			FB	
PMA0_RA	3C	RW		7C			BC			FC	
PMA1_RA	3D	RW		7D		USB_MISC_CR	BD	RW		FD	
PMA2_RA	3E	RW		7E			BE			FE	
PMA3_RA	3F	RW		7F			BF			FF	

Gray fields are reserved; do not access these fields. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V USB devices. For the most up-to-date electrical specifications, verify that you have the most recent data sheet available by visiting the company web site at http://www.cypress.com

Figure 8. Voltage versus CPU Frequency

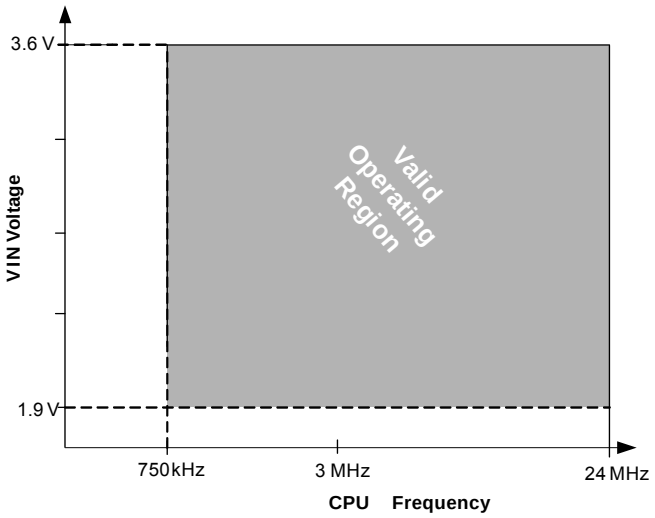
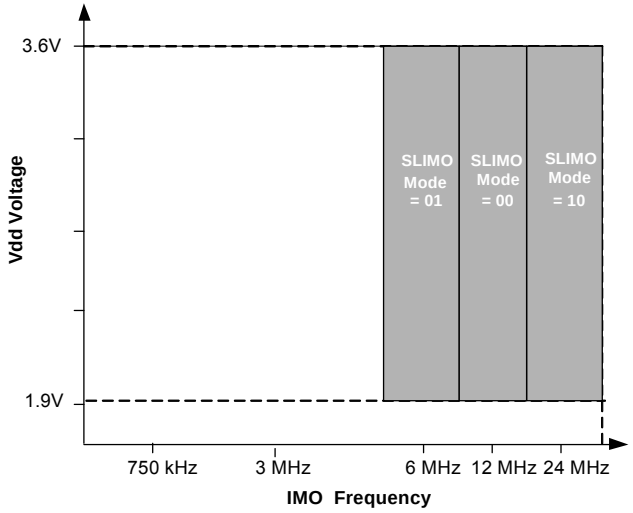


Figure 9. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 5. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	25	125	°C
V_{IN}[3]		–	1.9	–	3.63	V
V_{IO}	DC input voltage	–	–0.5	–	V_{IN} + 0.5	V
V_{IOZ}[4]	DC voltage applied to tristate	–	–0.5	–	V_{IN} + 0.5	V
I_{MIO}	Maximum current into any port pin	–	–25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD i) RF pins (ANT, ANTb) ii) Analog pins (XTALi, XTALo) iii) Remaining pins	 500 500 2000	–	–	V
LU	Latch-up current	In accordance with JESD78 standard	–	–	140	mA

Operating Temperature

Table 6. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature	–	0	–	70	°C

Notes
3. Program the device at 3.3 V only. Hence use Miniprog3 only since Miniprog1 does not support programming at 3.3 V.
4. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V_{IN}.

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 7. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN} [5, 6, 7, 8]	Supply voltage	No USB activity. Refer the table DC POR and LVD Specifications on page 23	1.9	–	3.6	V
V_{INUSB} [5, 6, 7, 8]	Operating voltage	USB activity, USB regulator bypassed	3.15	3.3	3.45	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are VIN ≤ 3.0 V, T_A = 25 °C, CPU = 24 MHz. no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are VIN ≤ 3.0 V, T_A = 25 °C, CPU = 12 MHz. no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are VIN ≤ 3.0 V, T_A = 25 °C, CPU = 6 MHz. no I/O sourcing current	–	1.16	1.80	mA
I_{SB0}	Deep sleep current	VIN ≤ 3.0 V, T_A = 25 °C, I/O regulator turned off	–	0.10	1.05	µA
I_{SB1}	Standby current with POR, LVD and sleep timer	VIN ≤ 3.0 V, T_A = 25 °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C}	Standby current with I^2C enabled	Conditions are VIN = 3.3 V, T_A = 25 °C and CPU = 24 MHz	–	1.64	–	µA

Notes

5. If powering down in standby sleep mode, to properly detect and recover from a VIN brown out condition any of the following actions must be taken:
   Bring the device out of sleep before powering down.
   Assure that VIN falls below 100 mV before powering back up.
   Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   Increase the buzz rate to assure that the falling edge of VIN is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
   For the referenced registers, refer to the enCoRe V Technical Reference Manual. In deep sleep mode, additional low power voltage monitoring circuitry allows VIN brown out conditions to be detected for edge rates slower than 1 V/ms.
6. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
7. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
8. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.

DC USB Interface Specifications

Table 8. DC USB Interface Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{USBI}	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
R_{USBA}	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
V_{OHUSB}	Static output high	–	2.8	–	3.6	V
V_{OLUSB}	Static output low	–	–	–	0.3	V
V_{DI}	Differential input sensitivity	–	0.2	–		V
V_{CM}	Differential input common mode range	–	0.8	–	2.5	V
V_{SE}	Single ended receiver threshold	–	0.8	–	2.0	V
C_{IN}	Transceiver capacitance	–	–	–	50	pF
I_{IO}	High Z state data line leakage	On D+ or D– line	–10	–	+10	µA
R_{PS2}	PS/2 pull-up resistance	–	3000	5000	7000	Ω
R_{EXT}	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

ADC Electrical Specifications

Table 9. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (VIN > 3.0 V)	–	24	–	dB
		PSRR (VIN < 3.0 V)	–	30	–	dB

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R_{GND}	Resistance of initialization switch to GND	–	–	–	800	Ω

The maximum pin voltage for measuring R_W and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{IN}	0.0	–	1.8	V
I_{LPC}	LPC supply current	–	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	–	3	30	mV

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: 0 °C ≤ T_A ≤ 70 °C, 1.9 V ≤ V_{IN} ≤ 3.6 V.

Table 12. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to V_{IN} – 0.2 V	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0		1.5	V

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 13. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	VIN – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	VIN – 0.40	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	VIN – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	VIN – 0.50	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, VIN > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, VIN > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.40	–		V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT2.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
$V_{IHLVT2.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 14. 1.9 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	VIN – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	VIN – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	VIN – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	VIN – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage	–	–	–	0.30 × VIN	V
V_{IH}	Input high voltage	–	0.65 × VIN	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR1}	2.36 V selected in PSoC Designer	VIN must be greater than or equal to 1.9 V during startup, reset from the XRES pin, or reset from watchdog.	–	2.36	2.41	V
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[9]	2.71	2.78	
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[10]	2.92	2.99	
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[11]	3.02	3.09	
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	

Notes
9. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
10. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
11. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Supply voltage for flash write operations	–	1.91	–	3.6	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See the appropriate DC Analog Mux Bus Specifications on page 20	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See the appropriate DC Analog Mux Bus Specifications on page 20	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC Analog Mux Bus Specifications on page 20. For VIN > 3 V use V_{OH4} in Table 6 on page 16.	V_{OH}	–	VIN	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

DC I²C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3, 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 17. DC I²C Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{ILI2C}	Input low level	3.1 V ≤ VIN ≤ 3.6 V	–	–	0.25 × VIN	V
		2.5 V ≤ VIN ≤ 3.0 V	–	–	0.3 × VIN	V
		1.9 V ≤ VIN ≤ 2.4 V	–	–	0.3 × VIN	V
V_{IHI2C}	Input high level	1.9 V ≤ VIN ≤ 3.6 V	0.65 × VIN	–	–	V

DC Reference Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and 0 °C ≤ T_A ≤ 70 °C, or 1.9 V to 2.4 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Reference Buffer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{Ref}	Reference buffer output	1.9 V to 3.6 V	1	–	1.05	V
V_{RefHi}	Reference buffer output	1.9 V to 3.6 V	1.2	–	1.25	V

DC IDAC Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–4.5	–	+4.5	LSB	
IDAC_INL	Integral nonlinearity	–5	–	+5	LSB	
IDAC_Gain (Source)	Range = 0.5x	6.64	–	22.46	µA	DAC setting = 128 dec.
	Range = 1x	14.5	–	47.8	µA	
	Range = 2x	42.7	–	92.3	µA	
	Range = 4x	91.1	–	170	µA	DAC setting = 128 dec.
	Range = 8x	184.5	–	426.9	µA	DAC setting = 128 dec.

AC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F_{32K1}	ILO frequency	–	19	32	50	kHz
F_{32K_U}	ILO untrimmed frequency	–	13	32	82	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	ILO duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	VIN slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up	Applies after part has booted	10	–	–	µs
t_{OS}	Startup time of ECO	–	–	1	–	s
t_{JIT_IMO}	N=32	6 MHz IMO cycle-to-cycle jitter (RMS)	–	0.7	6.7	ns
		6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	4.3	29.3	ns
		6 MHz IMO period jitter (RMS)	–	0.7	3.3	ns
		12 MHz IMO cycle-to-cycle jitter (RMS)	–	0.5	5.2	ns
		12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	2.3	5.6	ns
		12 MHz IMO period jitter (RMS)	–	0.4	2.6	ns
		24 MHz IMO cycle-to-cycle jitter (RMS)	–	1.0	8.7	ns
		24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	1.4	6.0	ns
		24 MHz IMO period jitter (RMS)	–	0.6	4.0	ns

AC USB Data Timings Specifications

Table 21. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DRATE}	Full speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
t_{JR1}	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
t_{JR2}	Receiver jitter tolerance	To pair transition	–9.0	–	9	ns
t_{DJ1}	FS Driver jitter	To next transition	–3.5	–	3.5	ns
t_{DJ2}	FS Driver jitter	To pair transition	–4.0	–	4.0	ns
t_{FDEOP}	Source jitter for differential transition	To SE0 transition	–2.0	–	5	ns
t_{FEOPT}	Source SE0 interval of EOP	–	160.0	–	175	ns
t_{FEOPR}	Receiver SE0 interval of EOP	–	82.0	–	–	ns
t_{FST}	Width of SE0 interval during differential transition	–	–	–	14	ns

AC USB Driver Specifications

Table 22. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{FR}	Transition rise time	50 pF	4	–	20	ns
t_{FF}	Transition fall time	50 pF	4	–	20	ns
t_{FRFM}	Rise/fall time matching	–	90	–	111	%
V_{CRS}	Output signal crossover voltage	–	1.30	–	2.00	V

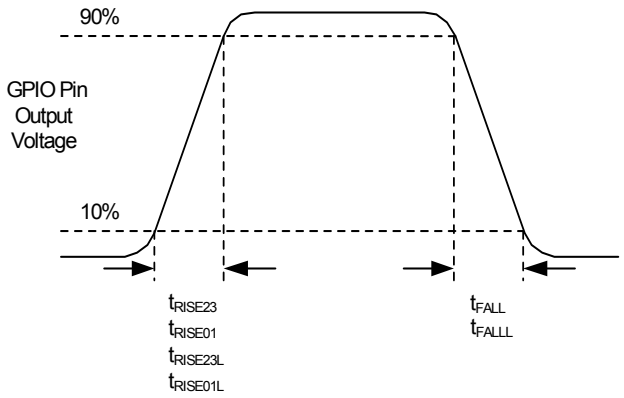
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode Port 0, 1	0 0	– –	6 MHz for 1.9 V <VIN < 2.40 V 12 MHz for 2.40 V < VIN< 3.6 V	MHz MHz
t_{RISE23}	Rise time, strong mode, Cload = 50 pF Port 2 or 3 or 4 pins	VIN = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Port 2 or 3 or 4 pins	VIN = 1.9 to 3.0 V, 10% to 90%	15	–	80	ns
t_{RISE01}	Rise time, strong mode, Cload = 50 pF, Ports 0 or 1	VIN = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	VIN = 1.9 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t_{FALL}	Fall time, strong mode, Cload = 50 pF, all ports	VIN = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	VIN = 1.9 to 3.0 V, 10% to 90%	10	–	70	ns

Figure 10. GPIO Timing Diagram



AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	µs

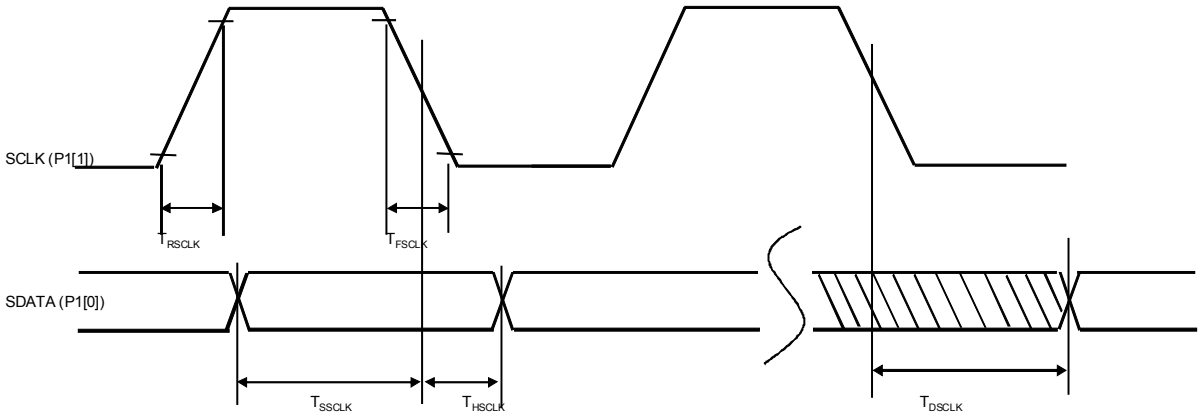
AC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
t_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	–	40	–	–	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
t_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
t_{WRITE}	Flash block write time	–	–	–	25	ms
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.9 \le V_{DD} \le 3.0$	–	–	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	µs
t_{XRES}	XRES pulse length	–	300	–	–	µs
$t_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$	V_{DD} stable to XRES assertion delay	–	14.27	–	–	ms
t_{POLL}	SDATA high pulse time	–	0.01	–	200	ms
t_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	µs

Figure 11. AC Waveform



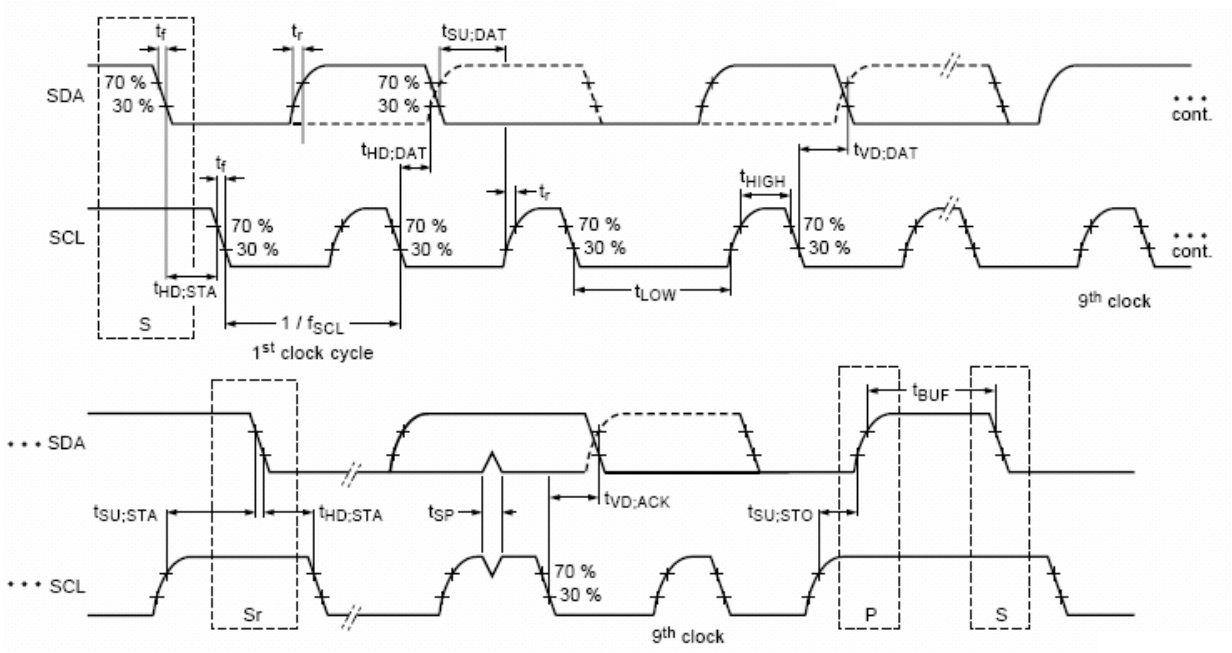
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 27. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.90	µs
$t_{SU;DAT}$	Data setup time	250	–	100[12]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 12. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

12. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

SPI Master AC Specifications

Table 28. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	VIN ≥ 2.4 V VIN < 2.4 V	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	VIN ≥ 2.4 V VIN < 2.4 V	60 100	– –	– –	ns ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_HIGH}	MOSI high time	–	40	–	–	ns

Figure 13. SPI Master Mode 0 and 2

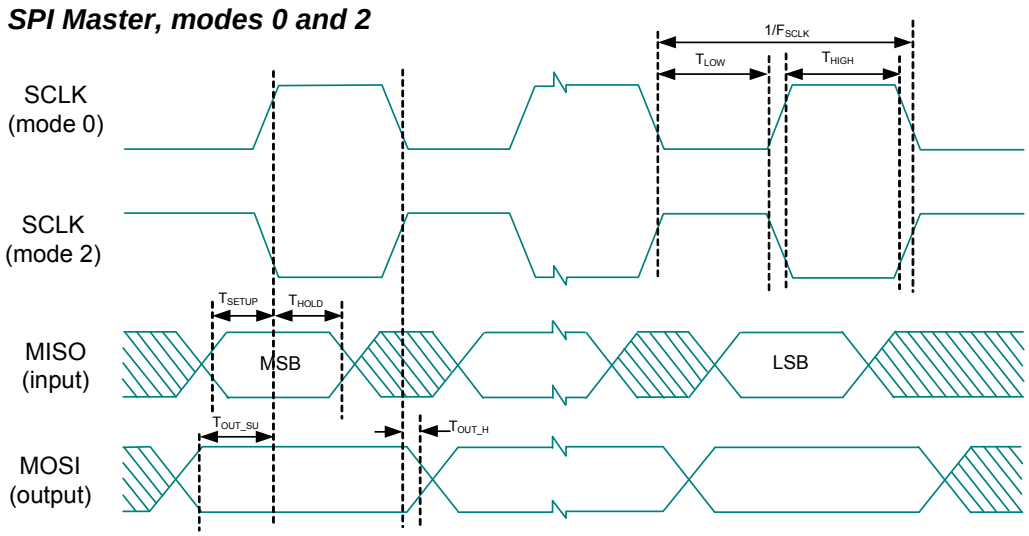
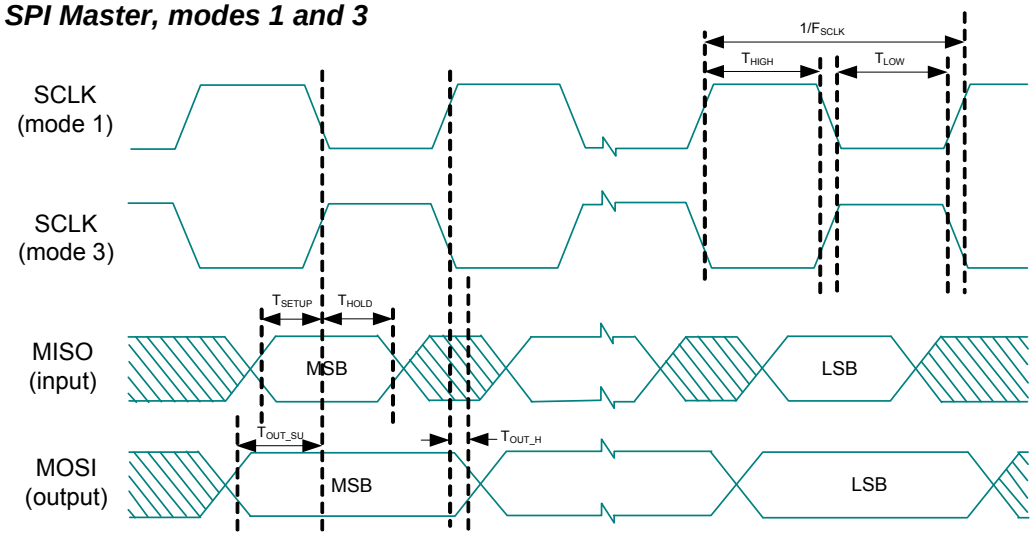


Figure 14. SPI Master Mode 1 and 3



SPI Slave AC Specifications

Table 29. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	42	–	–	ns
t_{HIGH}	SCLK high time	–	42	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 15. SPI Slave Mode 0 and 2

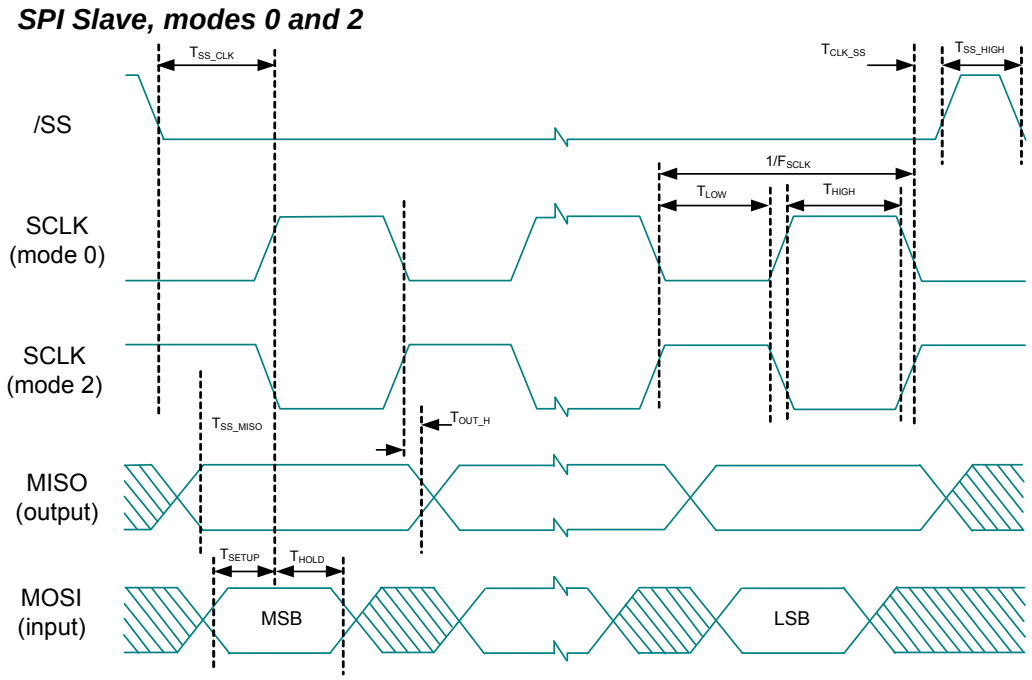
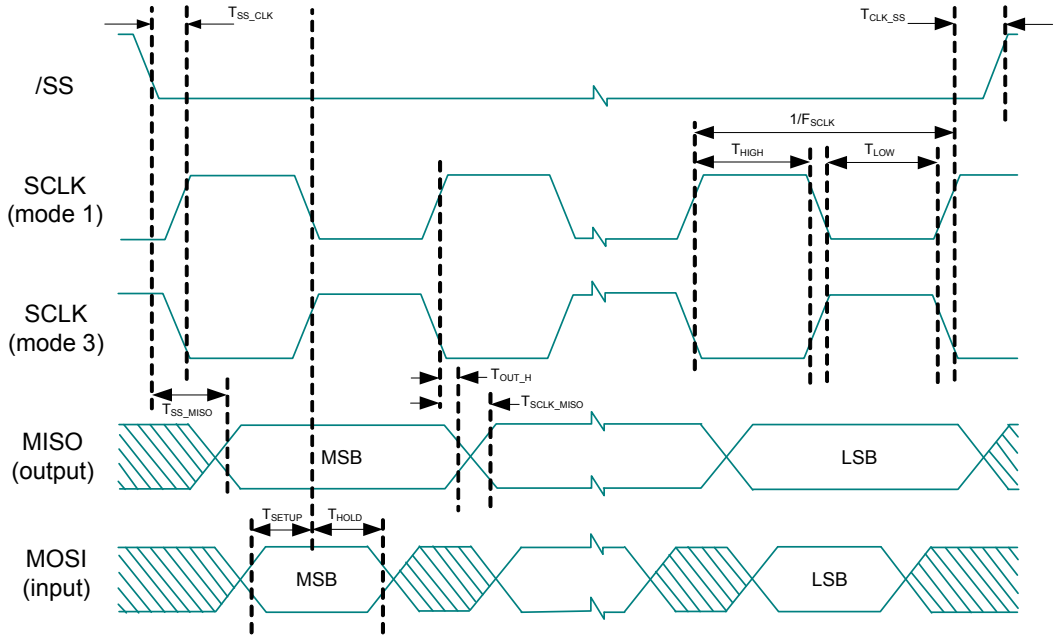


Figure 16. SPI Slave Mode 1 and 3

SPI Slave, modes 1 and 3



Electrical Specifications - RF Section

Symbol	Description	Min	Typ	Max	Units	Test Condition and Notes
	Supply voltage					
V_{IN}	DC power supply voltage range	1.9	–	3.6	VDC	Input to V_{IN} pins
	Current consumption					
I_{DD_TX2}	Current consumption – Tx	–	18.5	–	mA	Transmit power PA2.
I_{DD_TX12}		–	13.7	–	mA	Transmit power PA12.
I_{DD_RX}	Current consumption – Rx	–	18	–	mA	
I_{DD_IDLE1}	Current consumption – idle	–	1.1	–	mA	
I_{DD_SLPx}	Current consumption – sleep	–	1	–	µA	Temperature = +25 °C. Using firmware sleep patch. Register 27 = 0x1200, for V_{IN} ≥ 3.00 VDC only
I_{DD_SLPr}		–	8	–	µA	Temperature = +25 °C; using firmware sleep patch Register 27 = 0x4200.
I_{DD_SLPh}		–	38	–	µA	Temperature = +70 °C 'C' grade part; using firmware sleep patch Register 27 = 0x4200
V_{IH}	Logic input high	0.8 VIN	–	1.2 VIN	V	
V_{IL}	Logic input low	0	–	0.8	V	
$I_{\_LEAK\_IN}$	Input leakage current	–	–	10	µA	
V_{OH}	Logic output high	0.8 VIN	–	–	V	I_{OH} = 100 µA source
V_{OL}	Logic output low	–	–	0.4	V	I_{OL} = 100 µA sink
$I_{\_LEAK\_OUT}$	Output leakage current	–	–	10	µA	MISO in tristate
$T_{\_RISE\_OUT}$	Rise/fall time (SPI MISO)	–	8	25	ns	7 pF cap. load
$T_{\_RISE\_IN}$	Rise/fall time (SPI MOSI)	–	–	25	ns	
T_{r_spi}	CLK rise, fall time (SPI)	–	–	25	ns	Requirement for error-free register reading, writing.
$F_{\_OP}$	Operating frequency range	2400	–	2482	MHz	Usage on-the-air is subject to local regulatory agency restrictions regarding operating frequency.
V_{SWR_I}	Antenna port mismatch (Z_0 = 50 Ω)	–	<2:1	–	VSWR	Receive mode. Measured using LC matching circuit
$VSWR_{\_O}$		–	<2:1	–	VSWR	Transmit mode. Measured using LC matching circuit
Receive section						Measured using LC matching circuit for BER ≤ 0.1%

Electrical Specifications - RF Section *(continued)*

Symbol	Description	Min	Typ	Max	Units	Test Condition and Notes
RxS_{base}	Receiver sensitivity (FEC off)	–	–87	–	dBm	Room temperature only 0-ppm crystal frequency error.
RxS_{temp}		–	–84	–	dBm	Over temperature; 0-ppm crystal frequency error.
RxS_{ppm}		–	–84	–	dBm	Room temperature only 80-ppm total frequency error (± 40-ppm crystal frequency error, each end of RF link)
$RxS_{temp+ppm}$		–	–80	–	dBm	Over temperature; 80-ppm total frequency error (± 40-ppm crystal frequency error, each end of RF link)
$R_{xmax-sig}$	Maximum usable signal	–20	0	–	dBm	Room temperature only
Ts	Data (Symbol) rate	–	1	–	µs	
Minimum Carrier/Interference ratio						For BER ≤ 0.1%. Room temperature only.
$CI_{\_cochannel}$	Co-channel interference	–	+9	–	dB	–60-dBm desired signal
$CI_{\_1}$	Adjacent channel interference, 1-MHz offset	–	+6	–	dB	–60-dBm desired signal
$CI_{\_2}$	Adjacent channel interference, 2-MHz offset	–	–12	–	dB	–60-dBm desired signal
$CI_{\_3}$	Adjacent channel interference, 3-MHz offset	–	–24	–	dB	–67-dBm desired signal
OBB	Out-of-band blocking	–	≥ –27	–	dBm	30 MHz to 12.75 GHz Measured with ACX BF2520 ceramic filter on ant. pin. –67-dBm desired signal, BER ≤ 0.1%. Room temperature only.
Transmit section						Measured using a LC matching circuit
P_{AVH}	RF output power	–	+1	–	dBm	PA0 (PA_GN = 0, Reg9 = 0x1820). Room temperature only
P_{AVL}		–	–11.2	–	dBm	PA12 (PA_GN = 12, Reg9 = 0x1E20). Room temperature only.
TxP_{fx2}	Second harmonic	–	–45	–	dBm	Measured using a LC matching circuit. Room temperature only.
TxP_{fx3}	Third and higher harmonics	–	≤ –45	–	dBm	Measured using a LC matching circuit. Room temperature only.
Modulation characteristics						
$Df1_{avg}$		–	263	–	kHz	Modulation pattern: 11110000...
$Df2_{avg}$		–	255	–	kHz	Modulation pattern: 10101010...
In-band spurious emission						
IBS_2	2-MHz offset	–	–	–20	dBm	
IBS_3	3-MHz offset	–	–	–30	dBm	
IBS_4	≥ 4-MHz offset	–	≤ –30	–	dBm	

Electrical Specifications - RF Section *(continued)*

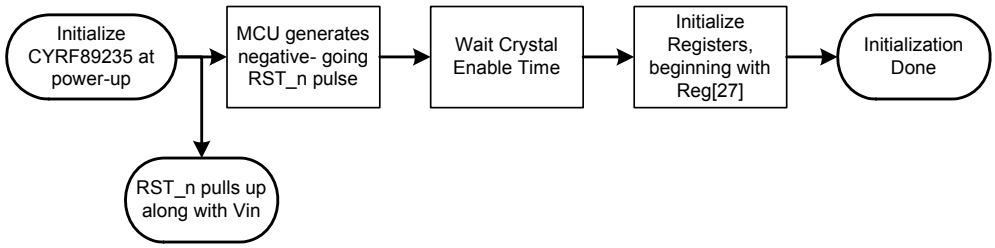
Symbol	Description	Min	Typ	Max	Units	Test Condition and Notes
RF VCO and PLL section						
F_{step}	Channel (Step) size		1	–	MHz	
L_{100k}	SSB phase noise		–75	–	dBc/Hz	100-kHz offset
L_{1M}			–105	–	dBc/Hz	1-MHz offset
dF_{X0}	Crystal oscillator frequency error	–40	–	+40	ppm	Relative to 12-MHz crystal reference frequency
T_{HOP}	RF PLL settling time	–	100	150	µs	Settle to within 30 kHz of final value. AutoCAL off.
T_{HOP_AC}		–	250	350	µs	Settle to within 30 kHz of final value. AutoCAL on.
LDO voltage regulator section						
V_{DO}	Dropout voltage	–	0.17	0.3	V	Measured during receive state

Initialization Timing Requirements

Table 30. Initialization Timing Requirements

Timing Parameter	Min	Max	Unit	Notes
T_{RSU}	–	30 / 150	ms	30 ms Reset setup time necessary to ensure complete Reset for VIN = 6.5 mV/s, 150 ms Reset setup time necessary to ensure complete Reset for VIN = 2 mV/s
T_{RPW}	1	10	µs	Reset pulse width necessary to ensure complete reset
T_{CMIN}	3	–	ms	Minimum recommended crystal oscillator and APLL settling time
T_{VIN}	–	6.5 / 2	mV/s	Maximum ramp time for V_{IN}, measured from 0 to 100% of final voltage. For example, if V_{IN}= 3.3 V, the max ramp time is 6.5 × 3.3 = 21.45 ms. If V_{IN}= 1.9 V, the max ramp time = 6.5 × 1.9 = 12.35 ms. Reset setup time necessary to ensure complete Reset for VIN = 6.5mV/s Reset setup time necessary to ensure complete Reset for VIN = 6.5mV/s Reset setup time necessary to ensure complete Reset for VIN = 6.5mV/s

Figure 17. Initialization Flowchart

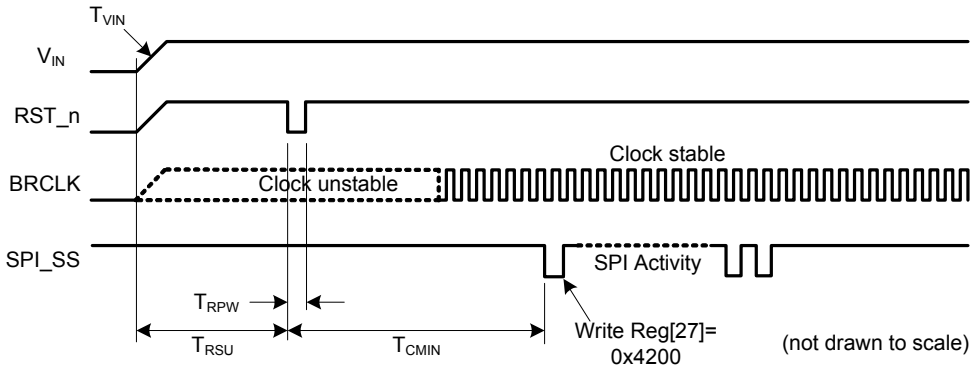


SPI Timing Requirements

Table 31. SPI Timing Requirements

Timing Parameter	Min	Max	Unit	Notes
T_{SSS}	20	–	ns	Setup time from assertion of SPI_SS to CLK edge
T_{SSH}	200	–	ns	Hold time required deassertion of SPI_SS
T_{SCKH}	40	–	ns	CLK minimum high time
T_{SCKL}	40	–	ns	CLK minimum low time
T_{SCK}	83	–	ns	Maximum CLK clock is 12 MHz
T_{SSU}	30	–	ns	MOSI setup time
T_{SHD}	10	–	ns	MOSI hold time
T_{SS_SU}	10	–	ns	Before SPI_SS enable, CLK hold low time requirement
T_{SS_HD}	200	–	ns	Minimum SPI inactive time
T_{SDO}	–	35	ns	MISO setup time, ready to read
T_{SDO1}	–	5	ns	If MISO is configured as tristate, MISO assertion time
T_{SDO2}	–	250	ns	If MISO is configured as tristate, MISO deassertion time
T1 Min_R50	350	–	ns	When reading register 50 (FIFO)
T1 Min	83	–	ns	When writing Register 50 (FIFO), or reading/writing any registers other than register 50.

Figure 18. Power-on and Register Programming Sequence



■ After register initialization, CYRF89235 is ready to transmit or receive.

Packaging Information

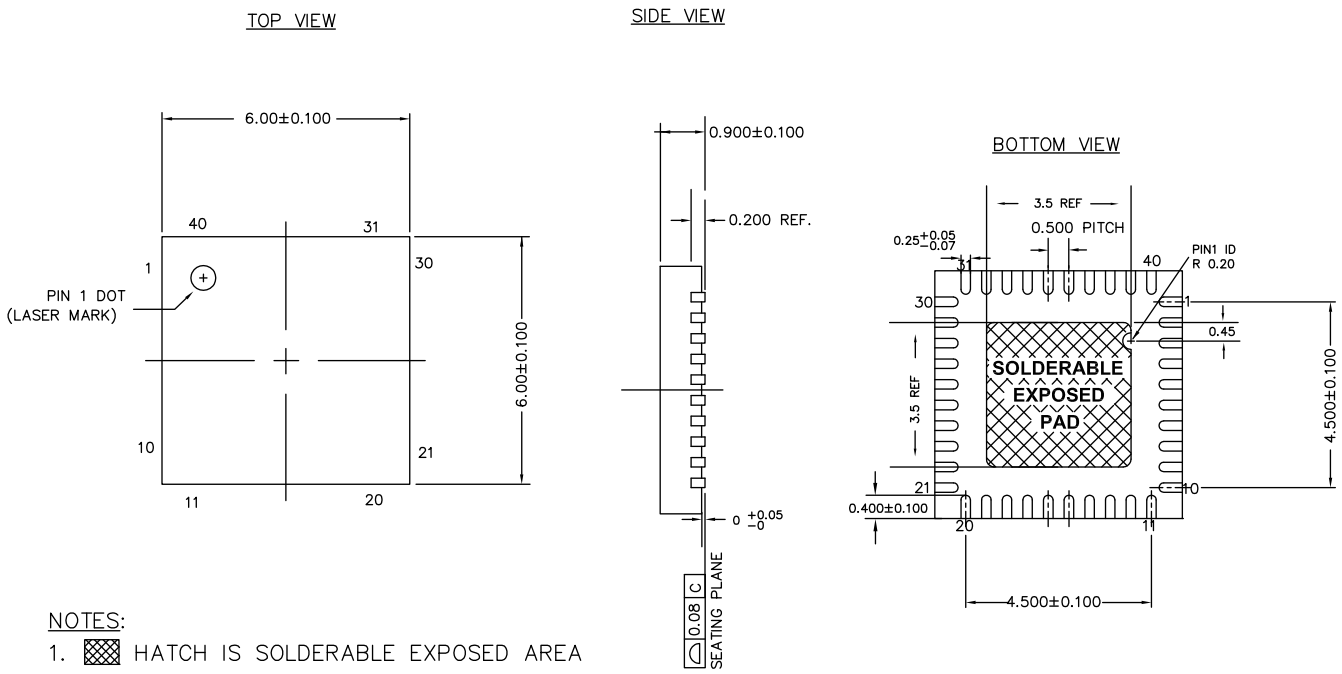
This section illustrates the packaging specifications for the PRoC-USB device, along with the thermal impedances for each package.

Important Note

Emulation tools may require a larger area on the target PCB than the chip's footprint.

Packaging Dimensions

Figure 19. 40-pin QFN (6 × 6 × 1.0 mm) LT40B 3.5 × 3.5 mm E-Pad (Sawn) Package Outline, 001-13190



NOTES:
1. HATCH IS SOLDERABLE EXPOSED AREA
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 0.086g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13190 *I

Thermal Impedances

Table 32. Thermal Impedances per Package

Package	Typical θ_{JA} [13]	Typical θ_{JC}
40-pin QFN [14]	27 °C/W	34 °C/W

Capacitance on Crystal Pins

Table 33. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
40-pin QFN	3.6 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 34. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [15]	Maximum Peak Temperature
40-pin QFN	260	265

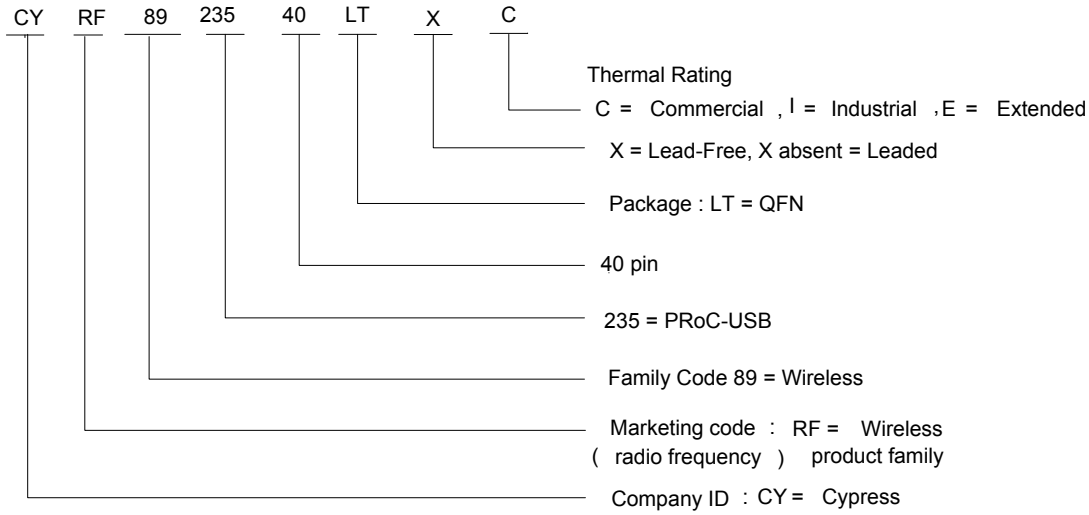
Notes
13. $T_J = T_A$ + Power x θ_{JA}.
14. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
15. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

Table 35. Ordering Information

Ordering Code	Package Information	Flash (KB)	SRAM (KB)	No. of GPIOs
CYRF89235-40LTXC	40-pin QFN (6 × 6 mm)	32	2	13

Ordering Code Definitions



Acronyms

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose I/O
ICE	in-circuit emulator
ILO	internal lowspeed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least significant bit
LVD	low voltage detect
MSb	most significant bit
POR	power-on reset
PPOR	precision power-on reset
PSoC	programmable system-on-chip
SLIMO	slow IMO
SRAM	static random access memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femtofarad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square
µW	microwatts
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volt

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are decimal.

Document History Page

Document Title: CYRF89235, PRoC™ USB Document Number: 001-77748				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3554967	ANTG	04/03/2012	New data sheet.
*A	3605878	ANTG	05/02/2012	Updated Document Title to read as “CYRF89235, PRoC™ USB”. Updated status as “Company Confidential”. Changed “PRoC NL Dongle” to “PRoC-USB” everywhere in the datasheet.
*B	3714928	AKHL	08/16/2012	Major text update. Added Electrical Specifications - RF Section.
*C	3747532	AKHL	09/18/2012	Removed “Company Confidential” status. Updated Packaging Information: Updated Packaging Dimensions: Removed spec 001-44328 *F. Added spec 001-13190 *H.
*D	3784571	AKHL	10/26/2012	Updated Functional Overview (Added Transmit Power Control). Updated Development Tools (Updated PSoC Designer Software Subsystems (Added Device Programmers)). Updated Electrical Specifications - RF Section (Replaced CYRF8935 with CYRF89235 in Figure 17 and also in the last bullet point below Figure 18). Updated Packaging Information (No update in package diagram, updated Thermal Impedances (Updated Table 32)). Updated to new template.
*E	3872679	AKHL	01/19/2013	Updated PRoC-USB Features (Replaced “Up to 37 general-purpose I/Os (GPIOs)” with “Up to 13 general-purpose I/Os (GPIOs)”). Updated Electrical Specifications (Updated DC Chip-Level Specifications (Changed maximum value of V_{INUSB} parameter from 3.60 V to 3.45 V in Table 7)).
*F	3982770	AKHL	05/15/2013	Updated PRoC-USB Features. Updated PRoC-USB Logical Block Diagram. Updated Functional Overview: Updated WirelessUSB-NL Subsystem (Updated Figure 6). Updated Transmit Power Control (Updated Table 1). Updated Electrical Specifications: Updated Absolute Maximum Ratings (Updated Table 5). Updated Operating Temperature (Updated Table 6). Updated DC Chip-Level Specifications (Updated Table 7). Updated DC IDAC Specifications (Updated Table 19). Updated Electrical Specifications - RF Section: Updated SPI Timing Requirements (Updated Table 31). Updated Packaging Information: No change in Package Diagram revision. Removed “Package Handling”. Updated Capacitance on Crystal Pins (Updated Table 33). Updated Solder Reflow Peak Temperature (Updated Table 34). Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions.
*G	5742799	SGUP	05/19/2017	Added watermark “Not recommended for new designs” across the document. Updated Packaging Information: Updated Packaging Dimensions: spec 001-13190 – Changed revision from *H to *I. Updated to new template.

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