Absolute Maximum Ratings @ 25ºC (Unless Otherwise Noted)

Parameter	Ratings	Units
Drain-to-Source Voltage	800	V
Gate-to-Source Voltage	±15	V
Pulsed Drain Current	150	mA
Total Package Dissipation [1]	0.4	W
Junction Temperature	125	ºC
Operational Temperature	-55 to +110	ºC
Storage Temperature	-55 to +125	ºC

[1] Mounted on 1"x1" 2 oz. Copper FR4 board.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

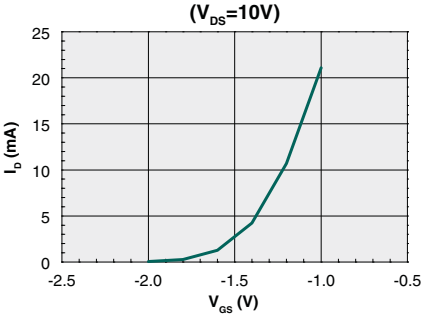
Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

Electrical Characteristics @ 25ºC (Unless Otherwise Noted)

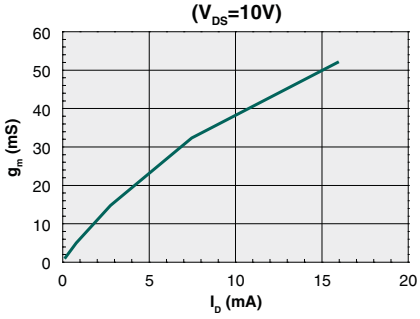
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	BV_{DSX}	V_{GS}= -5.5V, I_D=100µA	800	-	-	V
Gate-to-Source Off Voltage	$V_{GS(off)}$	V_{DS}= 15V, I_D=1µA	-1.4	-	-3.1	V
Change in $V_{GS(off)}$ with Temperature	$dV_{GS(off)}/dT$	V_{DS}= 15V, I_D=1µA	-	-	4.5	mV/ºC
Gate Body Leakage Current	I_{GSS}	V_{GS}=±15V, V_{DS}=0V	-	-	100	nA
Drain-to-Source Leakage Current	$I_{D(off)}$	V_{GS}= -5.5V, V_{DS}=800V	-	-	1	µA
Saturated Drain-to-Source Current	I_{DSS}	V_{GS}= 0V, V_{DS}=15V	20	-	-	mA
Static Drain-to-Source On-State Resistance	$R_{DS(on)}$	V_{GS}= 0V, I_D=20mA, V_{DS}=10V	-	-	380	Ω
Change in $R_{DS(on)}$ with Temperature	$dR_{DS(on)}/dT$		-	-	2.5	%/ºC
Forward Transconductance	G_{FS}	I_D= 10mA, V_{DS} = 10V	15	-	-	mʊ
Input Capacitance	C_{ISS}	V_{GS}= -3.5V V_{DS}= 25V f= 1MHz	-	20	-	pF
Common Source Output Capacitance	C_{OSS}			2.2		
Reverse Transfer Capacitance	C_{RSS}			1.3		
Source-Drain Diode Voltage Drop	V_{SD}	V_{GS}= -5V, I_{SD}=5mA	-	0.6	1	V
Thermal Impedance, Junction to Ambient	Θ_{JA}	-	-	250	-	ºC/W

PERFORMANCE DATA*

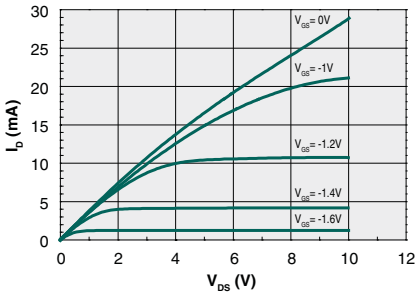
Input Admittance (V_{DS}=10V)



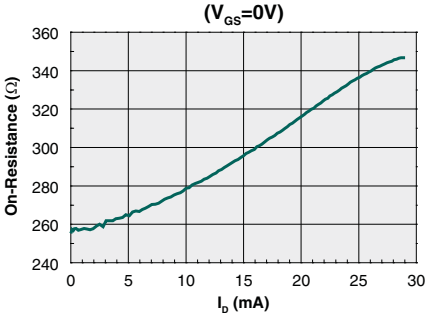
Transconductance vs. Drain Current (V_{DS}=10V)



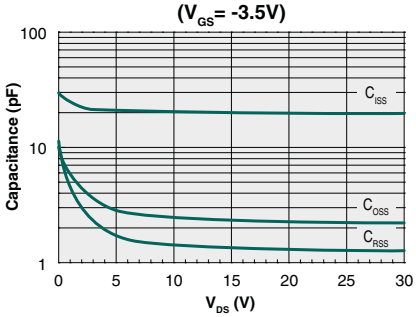
Output Characteristics



On-Resistance vs. Drain Current (V_{GS}=0V)



Capacitance vs. Drain-Source Voltage (V_{GS}= -3.5V)



*Unless otherwise noted, data presented in these graphs is typical of device operation at 25ºC.

Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC3982T	MSL 1

ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

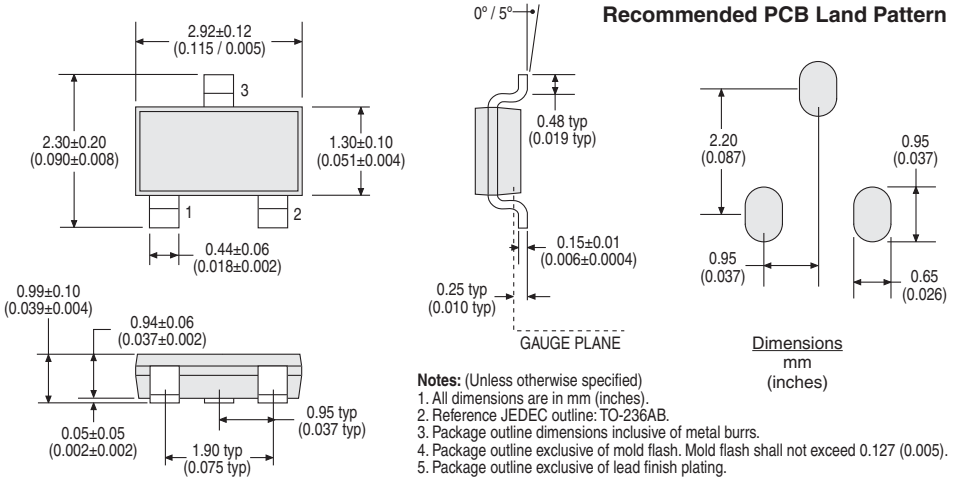
Device	Classification Temperature (T_c)	Dwell Time (t_p)	Max Reflow Cycles
CPC3982T	260°C	30 seconds	3

Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

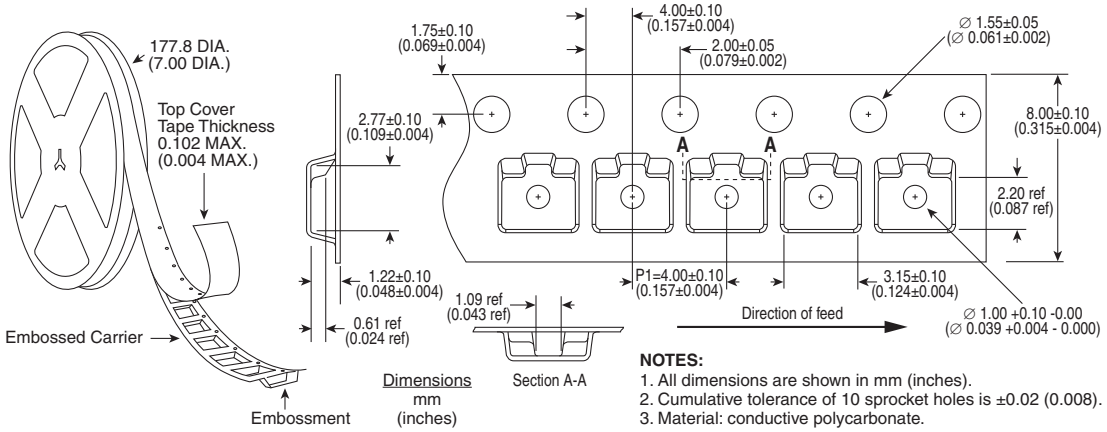
Mechanical Dimensions

CPC3982T



Notes: (Unless otherwise specified)
1. All dimensions are in mm (inches).
2. Reference JEDEC outline: TO-236AB.
3. Package outline dimensions inclusive of metal burrs.
4. Package outline exclusive of mold flash. Mold flash shall not exceed 0.127 (0.005).
5. Package outline exclusive of lead finish plating.

CPC3982TTR Tape & Reel



NOTES:
1. All dimensions are shown in mm (inches).
2. Cumulative tolerance of 10 sprocket holes is ±0.02 (0.008).
3. Material: conductive polycarbonate.

For additional information please visit our website at: www.ixysic.com

IXYS
A Littelfuse Technology

Specification: DS-CPC3982-R01

4/17/2020