Functional Diagrams

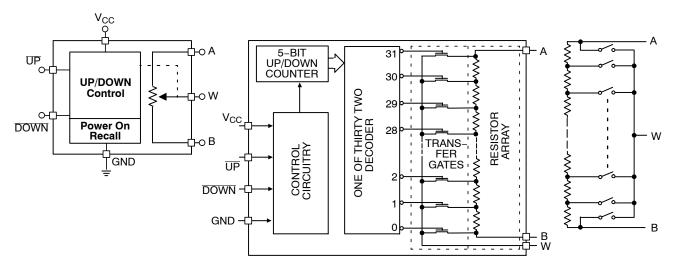


Figure 1. General

Figure 2. Detailed

Figure 3. Electronic Potentiometer Implementation

Pin Description

UP: Step-Up Control Input

When \overline{DOWN} input is high, a high-to-low transition on \overline{UP} input will cause the wiper to move one increment toward the A terminal.

DOWN: Step-Down Control Input

A high-to-low transition on \overline{DOWN} input will cause the wiper to move one increment towards the B terminal.

A: High End Potentiometer Terminal

A is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the B terminal. Voltage applied to the A terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

W: Wiper Potentiometer Terminal

W is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, \overline{UP} and \overline{DOWN} . Voltage applied to the W terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

B: Low End Potentiometer Terminal

B is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the A terminal. Voltage applied to the B terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. B and A are electrically interchangeable.

Device Operation

The CAT5128 operates like a digitally controlled potentiometer with A and B equivalent to the high and low terminals and W equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points, A and B. There are 31 resistor elements connected in series between the A and B terminals. The wiper terminal is connected to one of the 32 taps and controlled by two inputs, $\overline{\text{UP}}$ and $\overline{\text{DOWN}}$. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position.

A high-to-low transition on \overline{DOWN} input will decrement one step the wiper position (R_{WB} will decrease with 1LSB and R_{WA} will increase with 1LSB). If and only if \overline{DOWN} input is high, a high-to-low transition on \overline{UP} input will increment one step the wiper position (R_{WB} will increase with 1LSB and R_{WA} will decrease with 1LSB).

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. When the CAT5128 is powered-down, the wiper position is reset. When power is restored, the counter is set to the mid point, tap 15.

Table 1. OPERATION MODES

UP	DOWN	Operation		
High to Low	High	Wiper toward $A - R_W$ Increment		
X	Low	Wiper does not change		
High	High to Low	Wiper toward $B - R_W$ Decrement		
High to Low	High to Low	Wiper toward $B - R_W$ Decrement		
Low	Х	Wiper does not change		
High	High	Wiper does not change		

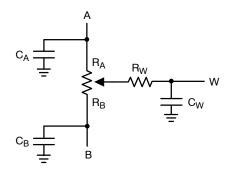


Figure 4. Potentiometer Equivalent Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V _{CC} to GND	-0.5 to +7 V	V
Inputs UP to GND DOWN to GND A, B, W to GND	-0.5 to V _{CC} +0.5 -0.5 to V _{CC} +0.5 -0.5 to V _{CC} +0.5	V
Operating Ambient Temperature Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to 150	°C
Lead Soldering (10 seconds max)	+300	°C
Thermal Resistance θ_{JA}	230	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
POWER SUPPLY						
V _{CC}	Operating Voltage Range		2.5	=	5.5	V
I _{CC1}	Supply Current (Increment)	$V_{CC} = 5.5 \text{ V}, f = 1 \text{ MHz}, I_{W} = 0$	_	_	100	μΑ
		$V_{CC} = 5.5 \text{ V}, f = 250 \text{ kHz}, I_W = 0$	_	_	50	μΑ
I _{SB1} (Note 1)	Supply Current (Standby)	UP, DOWN = V _{CC} or GND	=	0.01	1	μΑ

^{1.} These parameters are periodically sampled and are not production tested.

Table 4. LOGIC INPUTS ($V_{CC} = +2.5 \text{ V to } +5.5 \text{ V unless otherwise specified}$)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
I _{IH}	Input Leakage Current	$V_{IN} = V_{CC}$	_	_	10	μΑ
I _{IL}	Input Leakage Current	V _{IN} = 0 V	-	_	-10	μΑ
V _{IH1}	TTL High Level Input Voltage	$4.5 \text{ V} \le \text{V}_{CC} \le 5.5 \text{ V}$	2	_	V _{CC}	V
V _{IL1}	TTL Low Level Input Voltage		0	_	0.8	V
V _{IH2}	CMOS High Level Input Voltage	2.5 V ≤ V _{CC} ≤ 5.5 V	V _{CC} x 0.7	=	V _{CC} + 0.3	V
V _{IL2}	CMOS Low Level Input Voltage		-0.3	=	V _{CC} x 0.2	V

Table 5. POTENTIOMETER CHARACTERISTICS ($V_{CC} = +2.5 \text{ V}$ to +5.5 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
R _{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot. Resistance Tolerance				±20	%
V _A	Voltage on A pin		0		V _{CC}	V
V _B	Voltage on B pin		0		V _{CC}	V
	Resolution			3.2		%
INL	Integral Linearity Error	I _W ≤ 2 μA	-0.5	0.1	0.5	LSB
DNL	Differential Linearity Error	I _W ≤ 2 μA	-0.5	0.05	0.5	LSB
R _{WI}	Wiper Resistance	V _{CC} = 5 V, I _W = 1 mA		70		Ω
		V _{CC} = 2.5 V, I _W = 1 mA		150	300	Ω
I _W	Wiper Current	(Note 3)			1	mA
TC _{RPOT}	TC of Pot Resistance	(Note 4)		50		ppm/°C
TC _{RATIO}	Ratiometric TC	(Note 4)		5	20	ppm/°C
V _N (Note 4)	Noise	100 kHz / 1 kHz		8/24		nV/√Hz
C _A /C _B /C _W	Potentiometer Capacitances	(Note 4)		8/8/25		pF
fc (Note 4)	Frequency Response	Passive Attenuator, 10 kΩ		1.7		MHz

Table 6. AC CONDITIONS OF TEST

V _{CC} Range	$2.5 \text{ V} \le \text{V}_{CC} \le 5.5 \text{ V}$
Input Pulse Levels	0.2 V_{CC} to 0.7 V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V _{CC}

Typical values are for T_A = 25°C and nominal supply voltage.
 I_W = source or sink.
 These parameters are periodically sampled and are not production tested.

Table 7. AC OPERATING CHARACTERISTICS ($V_{CC} = +2.5 \text{ V}$ to +5.5 V, $V_H = V_{CC}$, $V_L = 0 \text{ V}$, unless othewise specified)

Symbol	Parameter	Min	Typ (Note 5)	Max	Units
t _{UP}	UP LOW Period	500	_	-	ns
t _{DOWN}	DOWN LOW Period	500	_	_	ns
t _{UP_CYC}	UP Cycle Time	1	-	1	μs
t _{DOWN_CYC}	DOWN Cycle Time	1	-	ı	μs
t _{UP_R} , t _{UP_F} (Note 6)	UP Rise and Fall Time	+	-	500	ns
t _{DOWN_R} , t _{DOWN_F} (Note 6)	DOWN Rise and Fall Time	+	-	500	ns
tup_set	UP Settling Time	200	_	_	ns
t _{DOWN} _SET	DOWN Settling Time	200	_		ns
t _{PU} (Note 6)	Power-up to Wiper Stable	_	_	1	ms

^{5.} Typical values are for T_A = 25°C and nominal supply voltage.
6. This parameter is periodically sampled and not 100% tested.

Interface Timing Diagrams

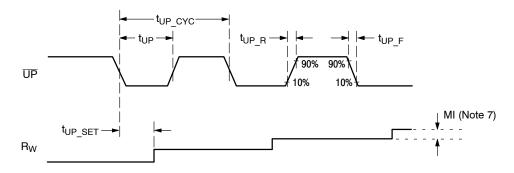
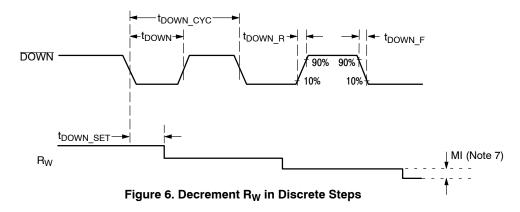


Figure 5. Increment R_W in Discrete Steps



7. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

Table 8. ORDERING INFORMATION

Orderable Part Number	Resistance (kΩ)	Lead Finish	Package	Shipping [†]
CAT5128TBI-10GT3	10			
CAT5128TBI-50GT3	50	NiPdAu SOT-23-8 (Pb-Free) 30	3000 / Tape & Reel	
CAT5128TBI-00GT3 (Note 12)	100		, ,	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{8.} For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

9. All packages are RoHS-compliant (Pb-Free, Halogen-Free).

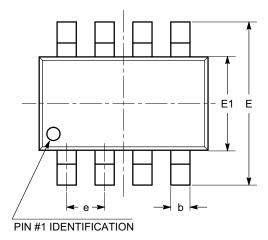
^{10.} The standard lead finish is NiPdAu.

^{11.} For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

^{12.} Contact factory for availability.

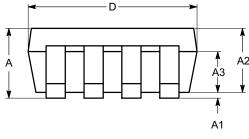
PACKAGE DIMENSIONS

SOT-23, 8 Lead CASE 527AK ISSUE A



TOP VIEW

SYMBOL	MIN	NOM	MAX	
Α	0.90		1.45	
A1	0.00		0.15	
A2	0.90	1.10	1.30	
АЗ	0.60		0.80	
b	0.28		0.38	
С	0.08		0.22	
D	2.90 BSC			
Е	2.80 BSC			
E1	1.60 BSC			
е		0.65 BSC		
L	0.30 0.45 0.60			
L1	0.60 REF			
L2	0.25 REF			
θ	0° 8°			





Notes:

- (1) All dimensions in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MO-178.

ON Semiconductor and IIII are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC which is a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any licenses under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Af

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5817-1050 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

CAT5128/D