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REVISION HISTORY

11/2016—Rev. C to Rev. D

Change to VDD Parameter, Table 2	5
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3/2016—Rev. B to Rev. C

Changes to Figure 3	7
Updated Outline Dimensions	14
Changes to Ordering Guide	15

8/2012—Rev. A to Rev. B

Changes to Table 1	3
Changes to Table 2	5
Change to Table 6	7
Updated Outline Dimensions	14
Changes to Ordering Guide	15

2/2009—Rev. 0 to Rev. A

Changes to Power Requirements, I_{DD} , Digital Inputs = 5 V	
Parameter, Table 1	4
Changes to Power Requirements, I_{DD} , Digital Inputs = 5 V	
Parameter, Table 2	5

7/2005—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Y Version ¹			Unit	Test Conditions/Comments
	25°C	–40°C to +85°C	–40°C to +125°C		
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance (R _{ON})	120			Ω typ	V _S = ±10 V, I _S = –1 mA; see Figure 20
	190	230	260	Ω max	V _{DD} = +13.5 V, V _{SS} = –13.5 V
On Resistance Match Between Channels (ΔR _{ON})	2.5			Ω typ	V _S = ±10 V, I _S = –1 mA
	6	10	11	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	20			Ω typ	V _S = –5 V/0 V/+5 V; I _S = –1 mA
	57	72	79	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.02			nA typ	V _{DD} = +16.5 V, V _{SS} = –16.5 V
	±0.1	±0.6	±1	nA max	V _S = ±10 V, V _D = ∓10 V; see Figure 21
Drain Off Leakage, I _D (Off)	±0.02			nA typ	V _S = ±10 V, V _D = ∓10 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I _D , I _S (On)	±0.02			nA typ	V _S = V _D = ±10 V; see Figure 22
	±0.1	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.005			μA typ	V _{IN} = V _{INL} or V _{INH}
			±0.1	μA max	
Digital Input Capacitance, C _{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS ²					
t _{ON}	110			ns typ	R _L = 300 Ω, C _L = 35 pF
	130	160	195	ns max	V _S = 10 V; see Figure 23
t _{OFF}	85			ns typ	R _L = 300 Ω, C _L = 35 pF
	115	130	150	ns max	V _S = 10 V; see Figure 23
Break-Before-Make Time Delay, t _D (ADG1213 Only)	25		10	ns typ	R _L = 300 Ω, C _L = 35 pF
				ns min	V _{S1} = V _{S2} = 10 V; see Figure 24
Charge Injection	–0.3			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 25
Off Isolation	80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	R _L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz
–3 dB Bandwidth	1000			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
C _S (Off)	0.9			pF typ	V _S = 0 V, f = 1 MHz
	1.1			pF max	V _S = 0 V, f = 1 MHz
C _D (Off)	1			pF typ	V _S = 0 V, f = 1 MHz
	1.2			pF max	V _S = 0 V, f = 1 MHz
C _D , C _S (On)	2.6			pF typ	V _S = 0 V, f = 1 MHz
	3			pF max	V _S = 0 V, f = 1 MHz

Parameter	Y Version ¹			Unit	Test Conditions/Comments
	25°C	–40°C to +85°C	–40°C to +125°C		
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
I_{DD}	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{DD}	220		380	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
I_{SS}	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	

¹ Temperature range for Y version is –40°C to +125°C.

² Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	Y Version ¹			Unit	Test Conditions/Comments
	25°C	–40°C to +85°C	–40°C to +125°C		
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	V _S = 0 V to 10 V, I _S = –1 mA; see Figure 20 V _{DD} = 10.8 V, V _{SS} = 0 V V _S = 0 V to 10 V, I _S = –1 mA
On Resistance (R _{ON})	300			Ω typ	
	475	567	625	Ω max	
On Resistance Match Between Channels (ΔR _{ON})	4.5			Ω typ	V _S = 0 V to 10 V, I _S = –1 mA
	12	26	27	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	60			Ω typ	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.02			nA typ	V _{DD} = 13.2 V, V _{SS} = 0 V V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I _D (Off)	±0.02			nA typ	V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I _D , I _S (On)	±0.02			nA typ	V _S = V _D = 1 V or 10 V; see Figure 22
	±0.1	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001			μA typ	
			±0.1	μA max	
Digital Input Capacitance, C _{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS ²					
t _{ON}	130			ns typ	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 23
	170	210	240	ns max	
t _{OFF}	95			ns typ	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 23
	120	145	180	ns max	
Break-Before-Make Time Delay, t _D (ADG1213 Only)	50		10	ns typ	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = 8 V; see Figure 24
				ns min	
Charge Injection	0			pC typ	V _S = 6 V, R _S = 0 Ω, C _L = 1 nF; see Figure 25
Off Isolation	80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 27
–3 dB Bandwidth	900			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
C _S (Off)	1.2			pF typ	V _S = 6 V, f = 1 MHz
	1.4			pF max	V _S = 6 V, f = 1 MHz
C _D (Off)	1.3			pF typ	V _S = 6 V, f = 1 MHz
	1.5			pF max	V _S = 6 V, f = 1 MHz
C _D , C _S (On)	3.2			pF typ	V _S = 6 V, f = 1 MHz
	3.9			pF max	V _S = 6 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001			μA typ	V _{DD} = 13.2 V Digital inputs = 0 V or V _{DD}
			1.0	μA max	
I _{DD}	220			μA typ	Digital inputs = 5 V
			1.0	μA max	
V _{DD}			5/16.5	V min/max	V _{SS} = 0 V, GND = 0 V

¹ Temperature range for Y version is –40°C to +125°C.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	GND − 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	72.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

Table 4. ADG1211/ADG1212 Truth Table

ADG1211 INx	ADG1212 INx	Switch Condition
0	1	On
1	0	Off

Table 5. ADG1213 Truth Table

ADG1213 INx	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

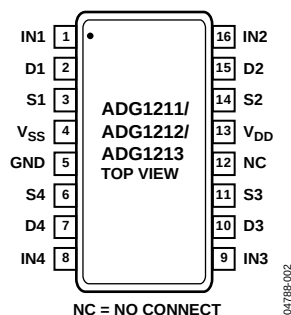
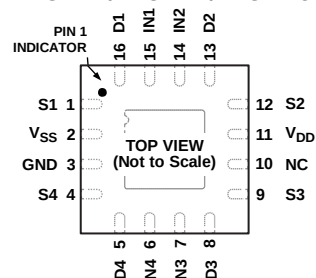


Figure 2. TSSOP Pin Configuration

ADG1211/ADG1212/ADG1213



NOTES

1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD MUST BE TIED TO SUBSTRATE, V_{SS} .

Figure 3. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. Can be an input or output.
3	1	S1	Source Terminal. Can be an input or output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. Can be an input or output.
7	5	D4	Drain Terminal. Can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. Can be an input or output.
11	9	S3	Source Terminal. Can be an input or output.
12	10	NC	No Internal Connection.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. Can be an input or output.
15	13	D2	Drain Terminal. Can be an input or output.
16	14	IN2	Logic Control Input.

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D (V_S)

The analog voltage on Terminals D and S.

R_{ON}

The ohmic resistance between D and S.

R_{FLAT(ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

C_S (Off)

The off switch source capacitance, measured with reference to ground.

C_D (Off)

The off switch drain capacitance, measured with reference

to ground.

C_D, C_S (On)

The on switch capacitance, measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between applying the digital control input and the output switching on. See Figure 23.

t_{OFF}

The delay between applying the digital control input and the output switching off. See Figure 23.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

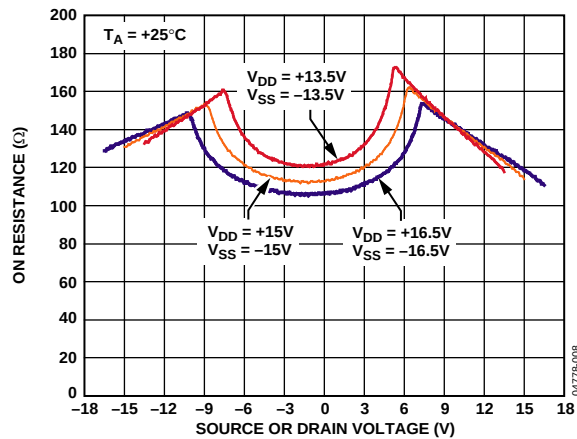
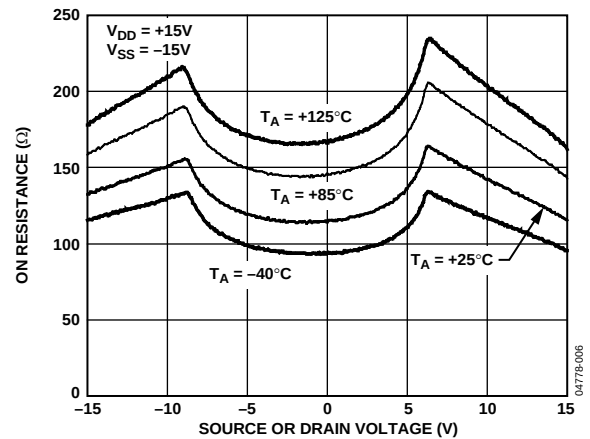
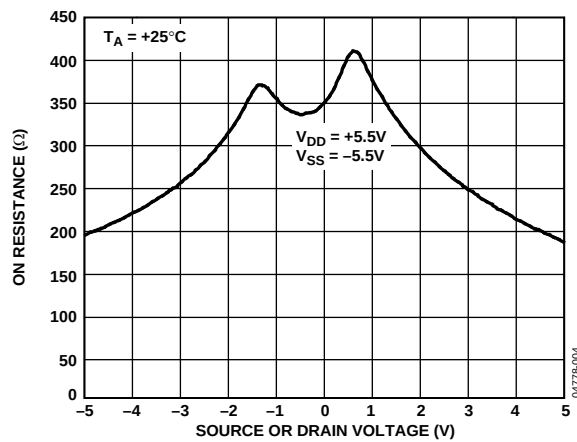
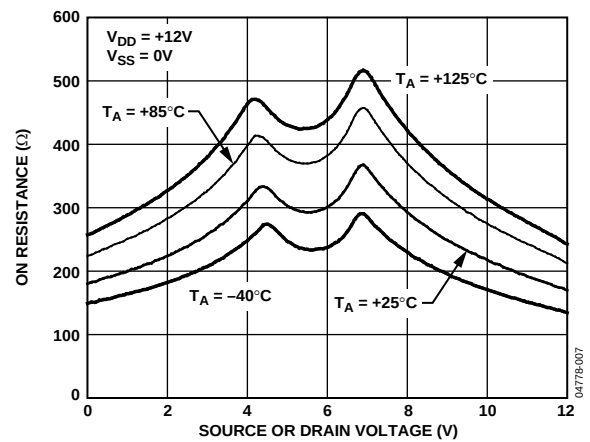
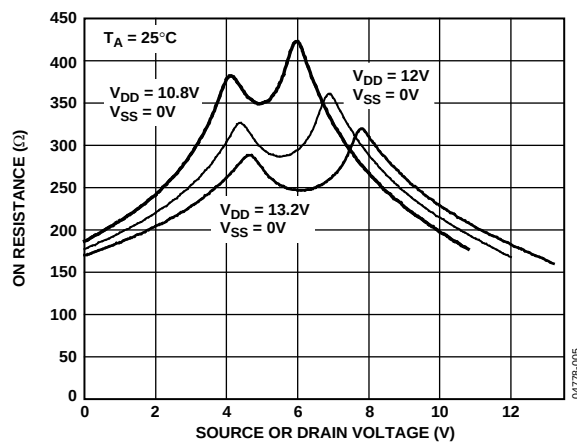
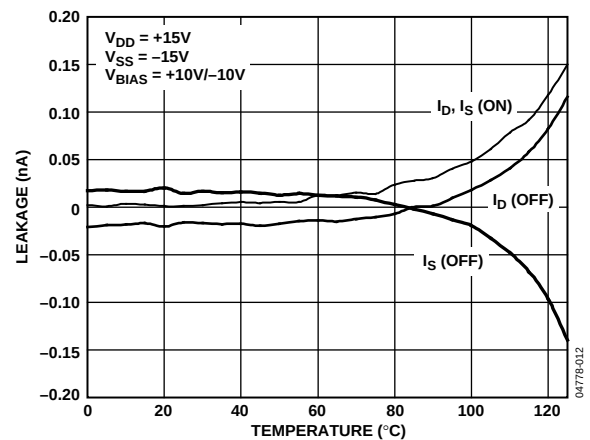
Figure 4. On Resistance as a Function of V_D (V_S) for Dual SupplyFigure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual SupplyFigure 5. On Resistance as a Function of V_D (V_S) for Dual SupplyFigure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single SupplyFigure 6. On Resistance as a Function of V_D (V_S) for Single Supply

Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

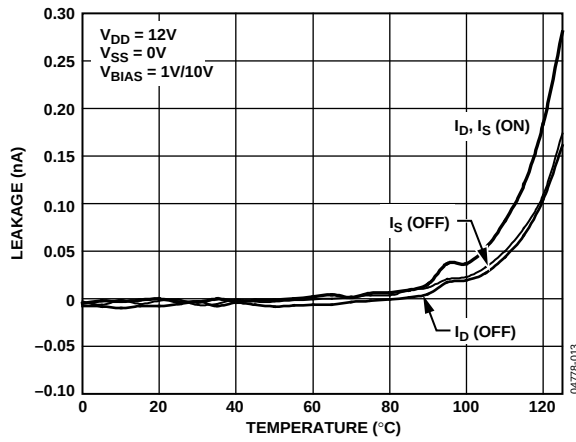


Figure 10. Leakage Currents as a Function of Temperature, Single Supply

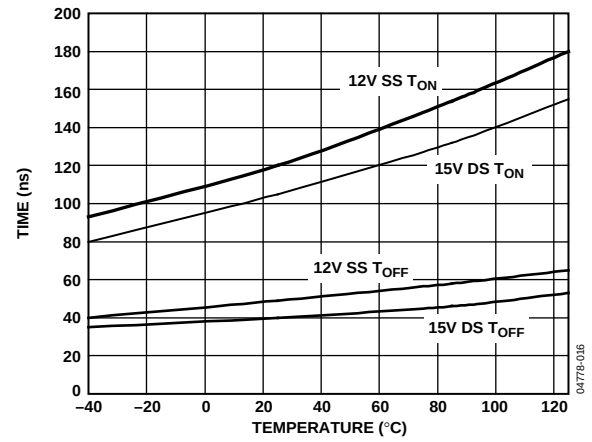


Figure 13. T_{ON}/T_{OFF} Times vs. Temperature

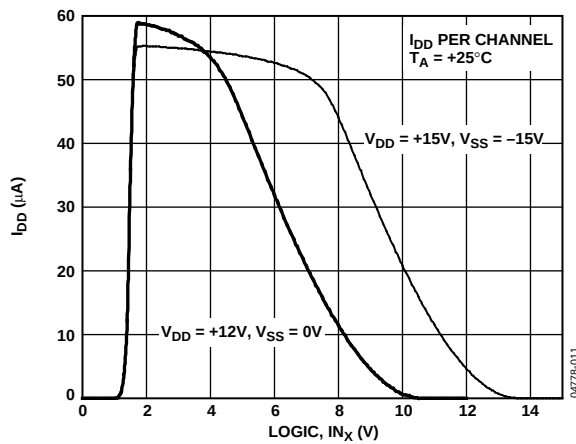


Figure 11. I_{DD} vs. Logic Level

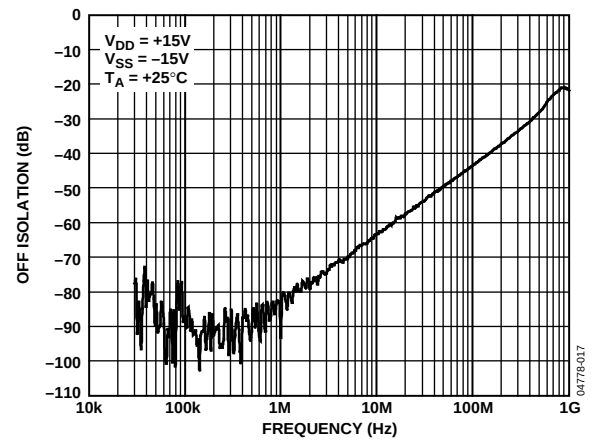


Figure 14. Off Isolation vs. Frequency

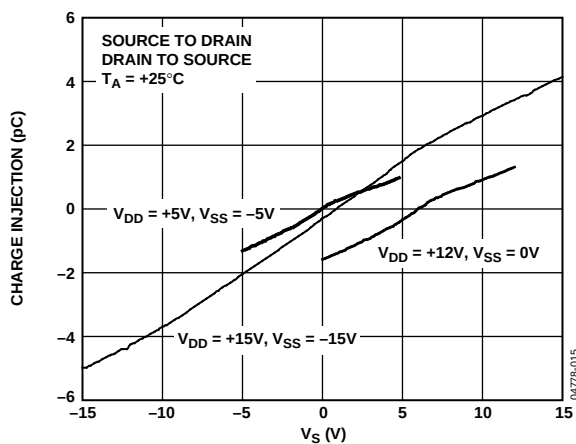


Figure 12. Charge Injection vs. Source Voltage

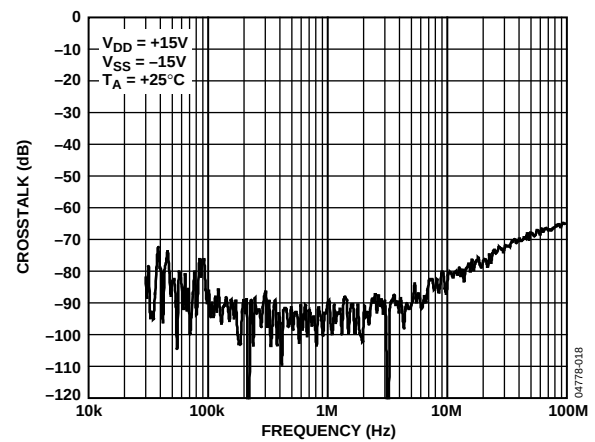


Figure 15. Crosstalk vs. Frequency

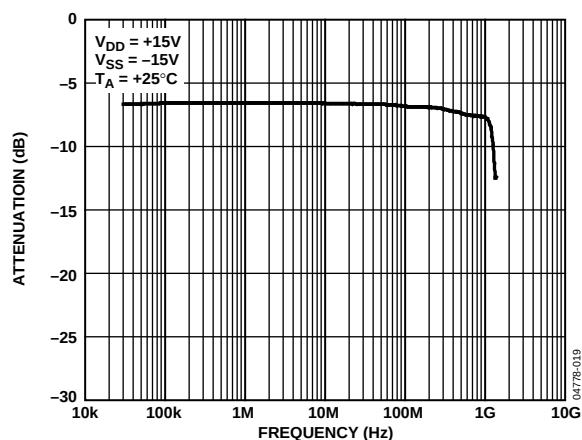


Figure 16. On Response vs. Frequency

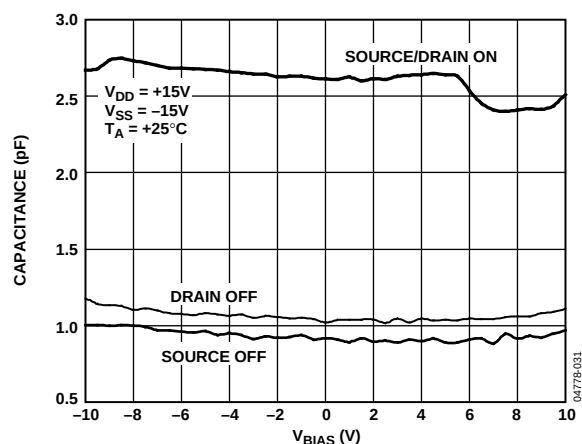


Figure 18. Capacitance vs. Source Voltage, Dual Supply

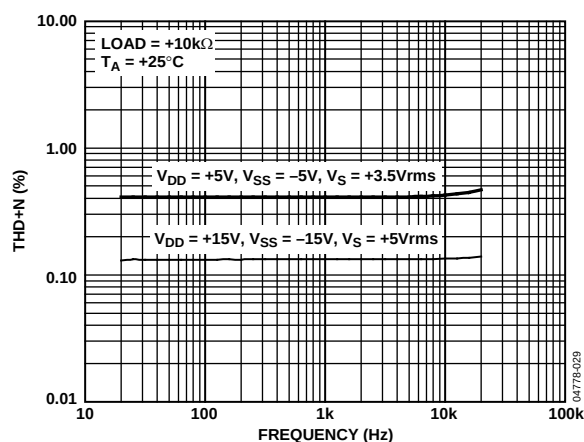


Figure 17. THD + N vs. Frequency

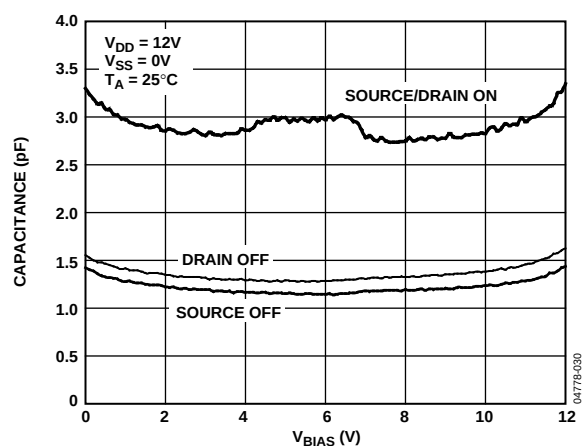


Figure 19. Capacitance vs. Source Voltage, Single Supply

TEST CIRCUITS

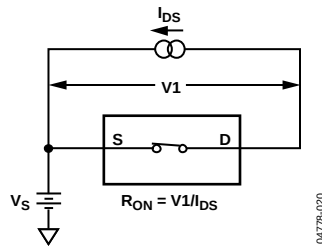


Figure 20. On Resistance

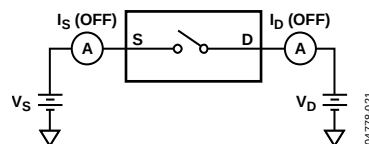


Figure 21. Off Leakage

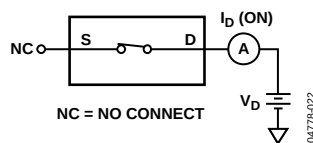


Figure 22. On Leakage

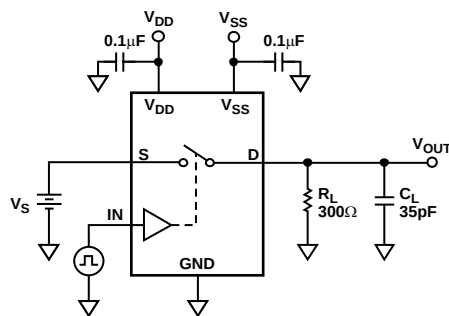


Figure 23. Switching Times

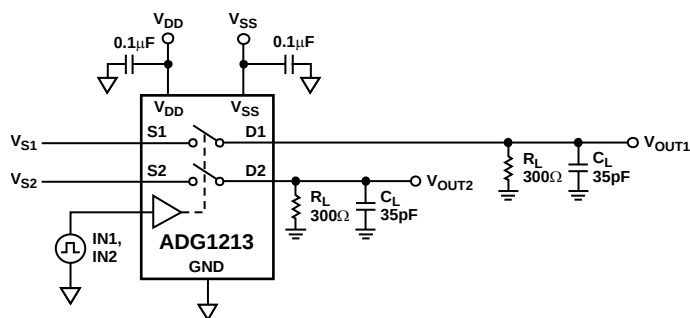
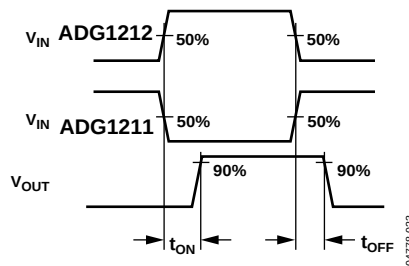
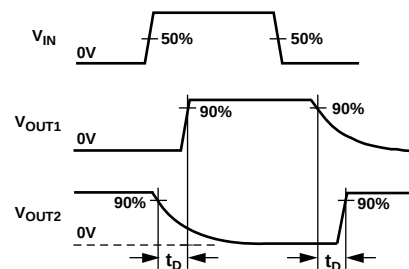


Figure 24. Break-Before-Make Time Delay



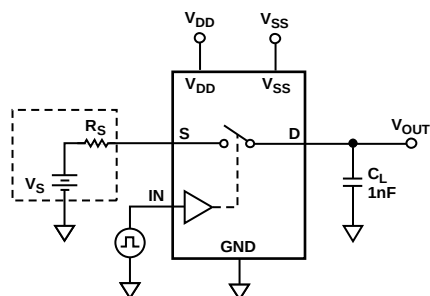
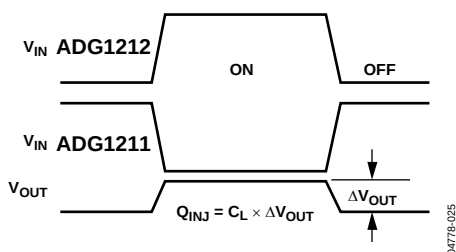


Figure 25. Charge Injection



04778-025

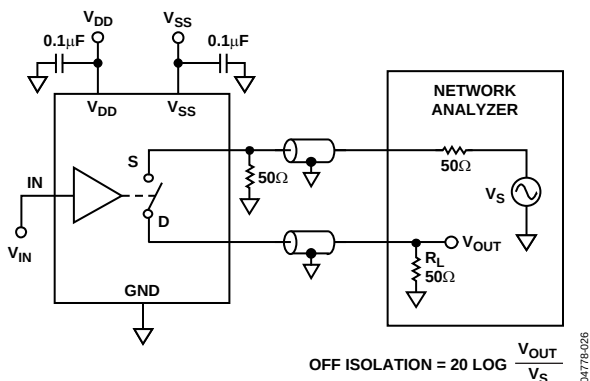


Figure 26. Off Isolation

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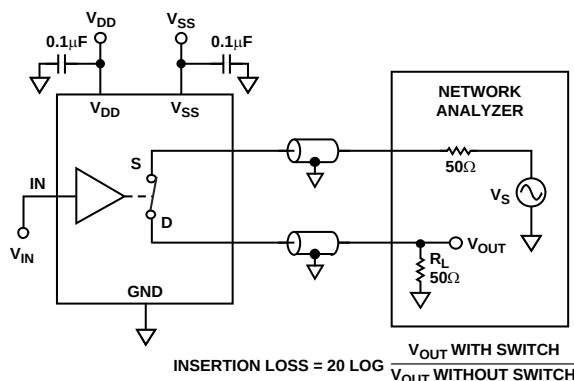


Figure 28. Bandwidth

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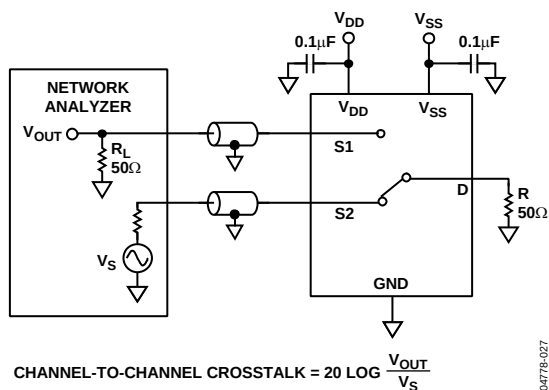


Figure 27. Channel-to-Channel Crosstalk

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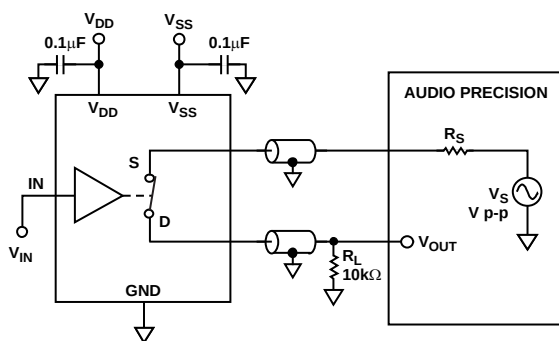


Figure 29. THD + Noise

04778-032

OUTLINE DIMENSIONS

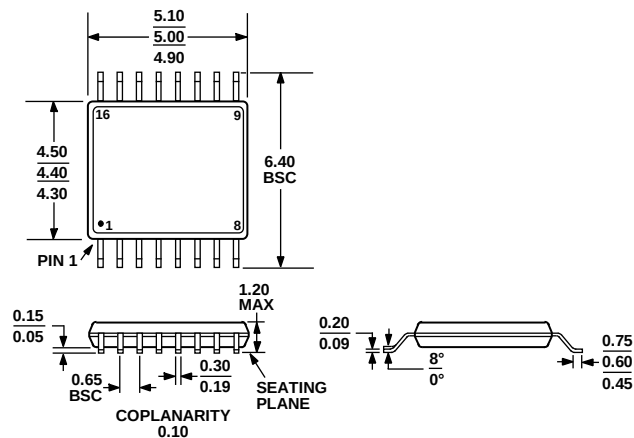
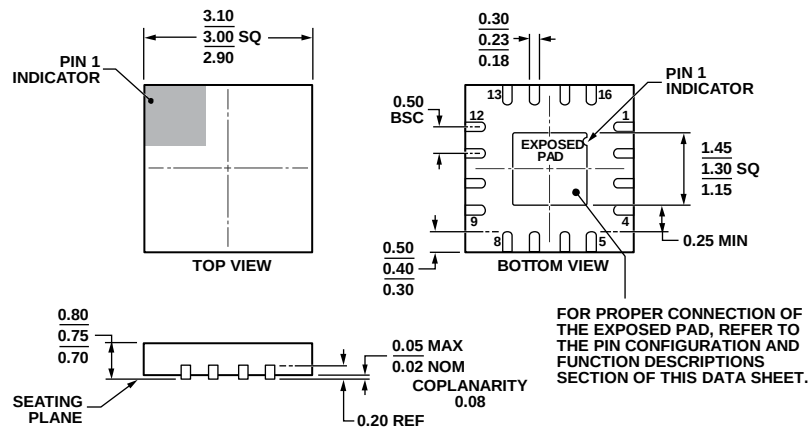


Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 31. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)

Dimensions shown in millimeters

111898-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG1211YRUZ	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	S07
ADG1211YRUZ-REEL	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1211YRUZ-REEL7	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1211YCPZ-500RL7	–40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	
ADG1211YCPZ-REEL7	–40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	
ADG1212YRUZ	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	S08
ADG1212YRUZ-REEL7	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1212YCPZ-500RL7	–40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	
ADG1212YCPZ-REEL7	–40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	
ADG1213YRUZ	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	S09
ADG1213YRUZ-REEL7	–40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1213YCPZ-500RL7	–40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	
ADG1213YCPZ-REEL7	–40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	

¹ Z = RoHS Compliant Part.

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