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SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 2 kΩ, Gain = +1, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.5 V p-p	300	350		MHz
	G = +2, V_O = 0.5 V p-p		175		MHz
	G = +1, V_O = 2 V p-p		100		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		45		MHz
Slew Rate	G = +1, V_O = 2 V step, R_L = 2 kΩ	400	425		V/µs
Overdrive Recovery Time	G = +2, 1 V overdrive		50		ns
Settling Time to 0.1%	G = +2, V_O = 2 V step		18		ns
NOISE/HARMONIC PERFORMANCE					
SFDR					
Second Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−90		dBc
Third Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−92		dBc
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−65		dBc
Third Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−70		dBc
Crosstalk, Output-to-Output (AD8039)	f = 5 MHz, G = +2		−70		dB
Input Voltage Noise	f = 100 kHz		8		nV/√Hz
Input Current Noise	f = 100 kHz		600		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.5	3	mV
Input Offset Voltage Drift			4.5		µV/°C
Input Bias Current			400	750	nA
Input Bias Current Drift			3		nA/°C
Input Offset Current			±25		nA
Open-Loop Gain	V_O = ±2.5 V		70		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		±4		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	61	67		dB
OUTPUT CHARACTERISTICS					
DC Output Voltage Swing	R_L = 2 kΩ, saturated output		±4		V
Capacitive Load Drive	30% overshoot, G = +2		20		pF
POWER SUPPLY					
Operating Range		3.0		12	V
Quiescent Current per Amplifier			1.0	1.5	mA
Power Supply Rejection Ratio	−Supply	−71	−77		dB
	+Supply	−64	−70		dB
POWER-DOWN DISABLE[1]					
Turn-On Time			180		ns
Turn-Off Time			700		ns
Disable Voltage—Part is Off			$+V_S$ − 4.5		V
Disable Voltage—Part is On			$+V_S$ − 2.5		V
Disabled Quiescent Current			0.2		mA
Disabled In/Out Isolation	f = 1 MHz		−60		dB

[1] Only available in AD8038 8-lead SOIC package.

T_A = 25°C, V_S = 5 V, R_L = 2 kΩ to V_S/2, Gain = +1, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	275	300		MHz
	G = +2, V_O = 0.2 V p-p		150		MHz
	G = +1, V_O = 2 V p-p		30		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		45		MHz
Slew Rate	G = +1, V_O = 2 V step, R_L = 2 kΩ	340	365		V/µs
Overdrive Recovery Time	G = +2, 1 V overdrive		50		ns
Settling Time to 0.1%	G = +2, V_O = 2 V step		18		ns
NOISE/HARMONIC PERFORMANCE					
SFDR					
Second Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−82		dBc
Third Harmonic	f_C = 1 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−79		dBc
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−60		dBc
Third Harmonic	f_C = 5 MHz, V_O = 2 V p-p, R_L = 2 kΩ		−67		dBc
Crosstalk, Output-to-Output	f = 5 MHz, G = +2		−70		dB
Input Voltage Noise	f = 100 kHz		8		nV/√Hz
Input Current Noise	f = 100 kHz		600		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.8	3	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current			400	750	nA
Input Bias Current Drift			3		nA/°C
Input Offset Current			±30		nA
Open-Loop Gain	V_O = ±2.5 V		70		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		1.0 – 4.0		V
Common-Mode Rejection Ratio	V_{CM} = ±1 V	59	65		dB
OUTPUT CHARACTERISTICS					
DC Output Voltage Swing	R_L = 2 kΩ, saturated output		0.9 – 4.1		V
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current per Amplifier			0.9	1.5	mA
Power Supply Rejection Ratio		−65	−71		dB
POWER-DOWN DISABLE[1]					
Turn-On Time			210		ns
Turn-Off Time			700		ns
Disable Voltage—Part is Off			$+V_S$ – 4.5		V
Disable Voltage—Part is On			$+V_S$ – 2.5		V
Disabled Quiescent Current			0.2		mA
Disabled In/Out Isolation	f = 1 MHz		−60		dB

[1] Only available in AD8038 8-lead SOIC package.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 5
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±4 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8038/AD8039 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8038/AD8039. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{quiescent power} + (\textit{total drive power} - \textit{load power})$$

$$P_D = [V_S \times I_S] + [(V_S/2) \times (V_{OUT}/R_L)] - [V_{OUT}^2/R_L]$$

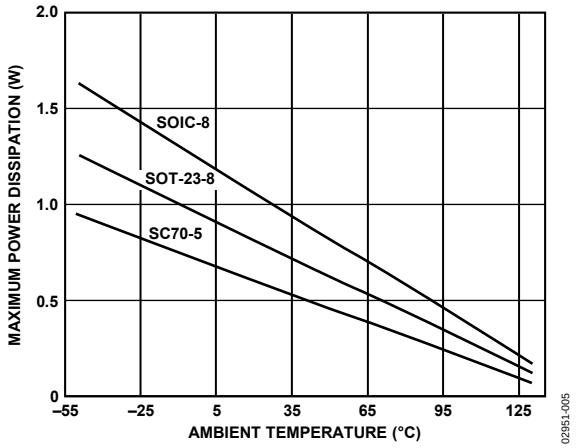


Figure 5. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

RMS output voltages should be considered. If R_L is referenced to V_{S-}, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply

$$P_D = (V_S \times I_S) + (V_S/4)^2/R_L$$

In single-supply operation with R_L referenced to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, throughholes, ground, and power planes reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the Layout, Grounding, and Bypassing Considerations section.

Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (125°C/W), 5-lead SC70 (210°C/W), and 8-lead SOT-23 (160°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current from the AD8038/AD8039 will likely cause a catastrophic failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: ±5 V, C_L = 5 pF, G = +2, R_G = R_F = 1 kΩ, R_L = 2 kΩ, V_O = 2 V p-p, Frequency = 1 MHz, T_A = 25°C.

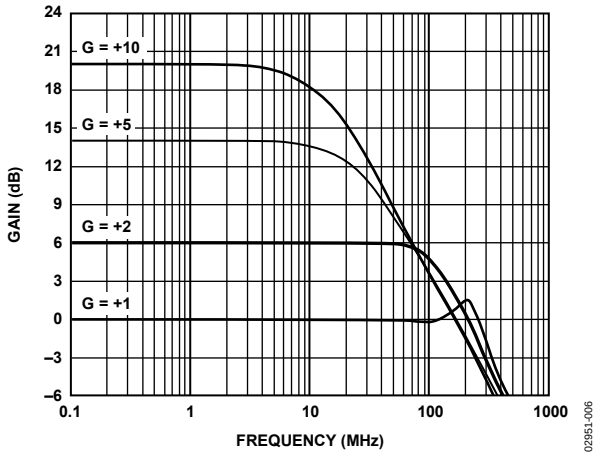


Figure 6. Small Signal Frequency Response for Various Gains, V_{OUT} = 500 mV p-p

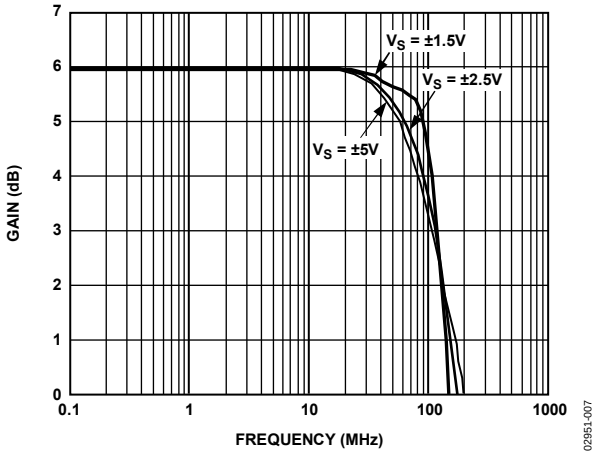


Figure 7. Small Signal Frequency Response for Various Supplies, V_{OUT} = 500 mV p-p

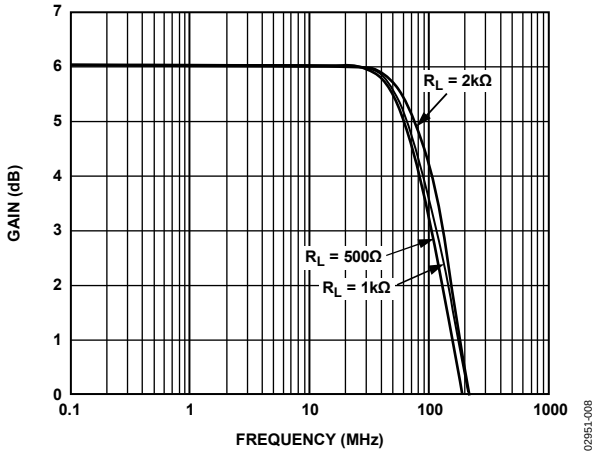


Figure 8. Small Signal Frequency Response for Various R_L, V_S = ±5 V, V_{OUT} = 500 mV p-p

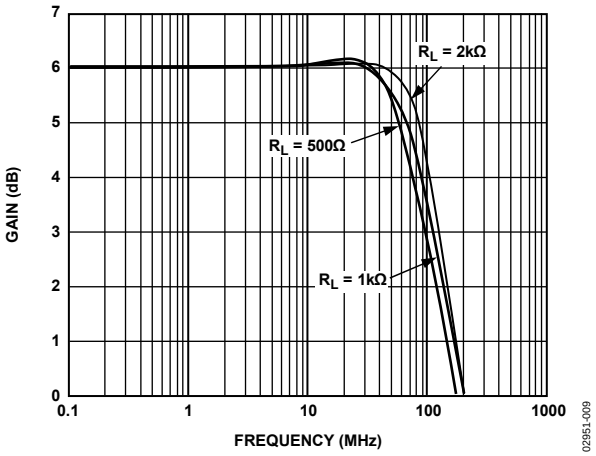


Figure 9. Small Signal Frequency Response for Various R_L, V_S = 5 V, V_{OUT} = 500 mV p-p

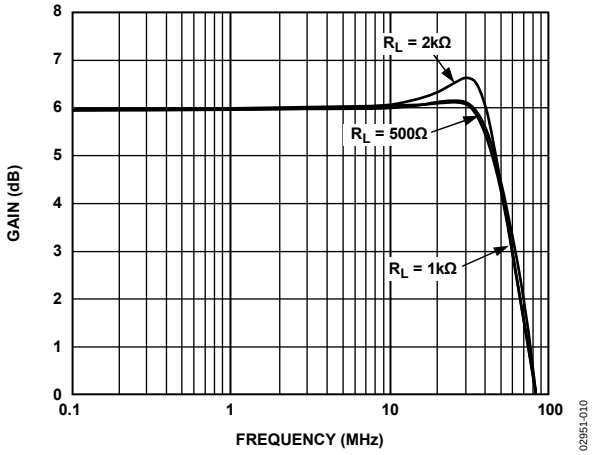


Figure 10. Large Signal Frequency Response for Various R_L, V_{OUT} = 3 V p-p, V_S = 5 V

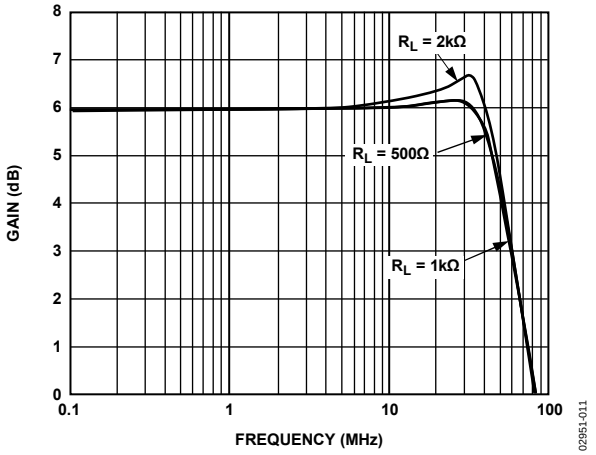


Figure 11. Large Signal Frequency Response for Various R_L, V_{OUT} = 4 V p-p, V_S = ±5 V

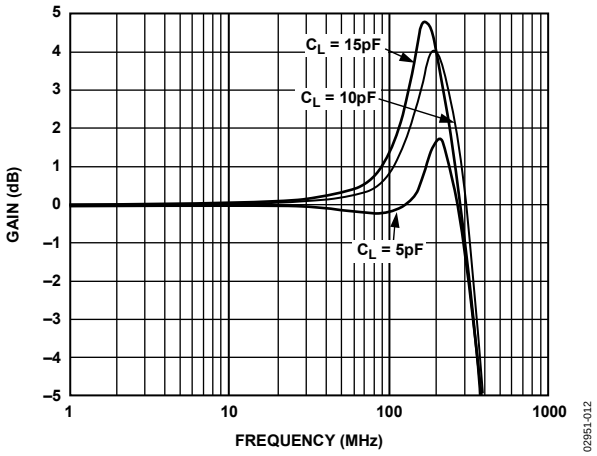


Figure 12. Small Signal Frequency Response for Various C_L, V_{OUT} = 500 mV p-p, V_S = ±5 V, G = +1

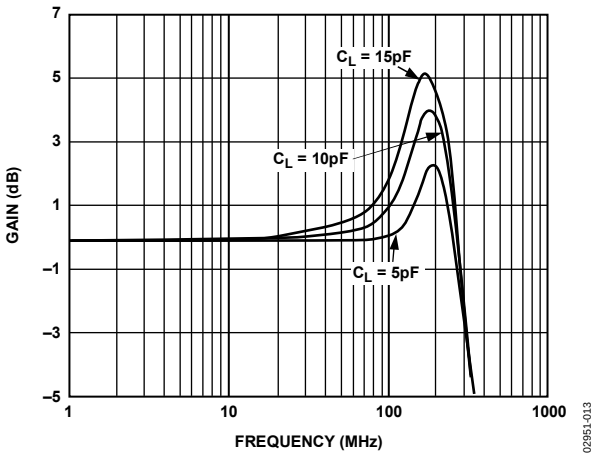


Figure 13. Small Signal Frequency Response for Various C_L, V_{OUT} = 500 mV p-p, V_S = 5 V, G = +1

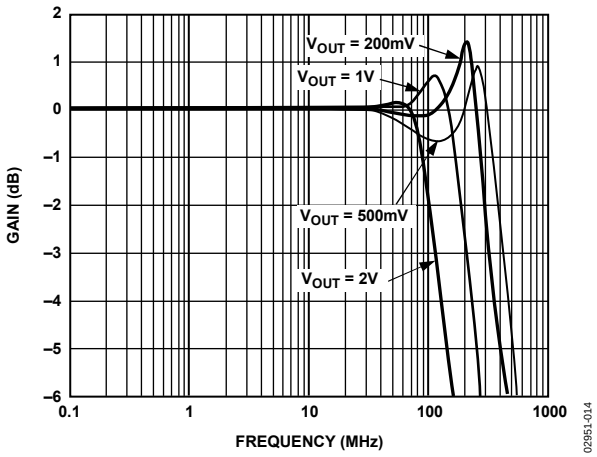


Figure 14. Frequency Response for Various Output Voltage Levels

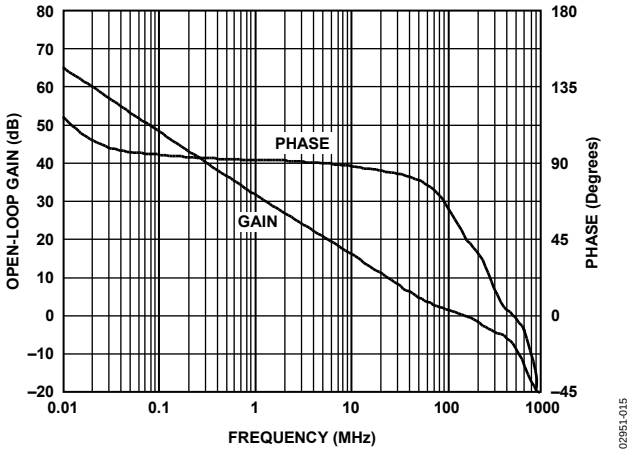


Figure 15. Open-Loop Gain and Phase, V_S = ±5 V

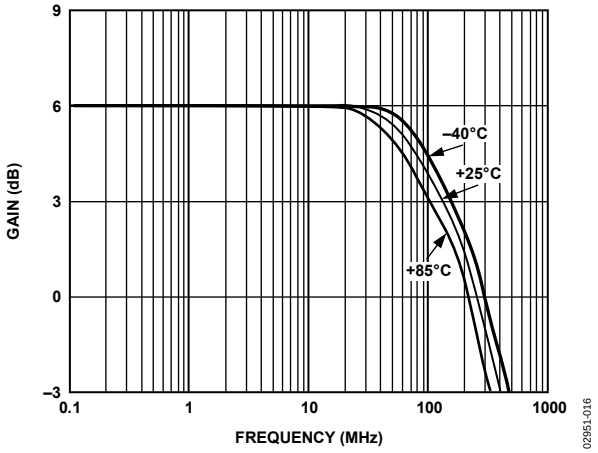


Figure 16. Frequency Response vs. Temperature, Gain = +2, V_S = ±5 V, V_{OUT} = 2 V p-p

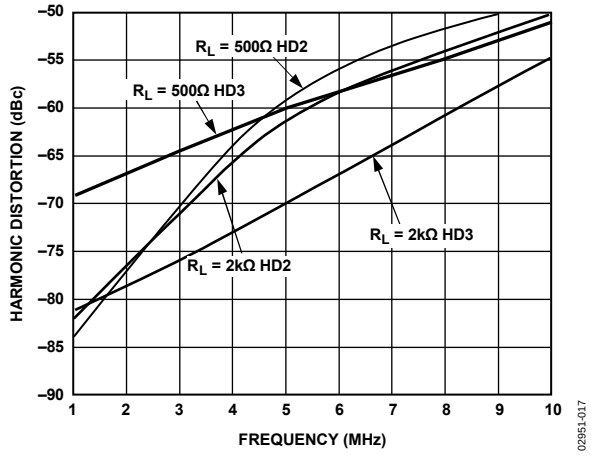


Figure 17. Harmonic Distortion vs. Frequency for Various Loads, V_S = ±5 V, V_{OUT} = 2 V p-p, G = +2

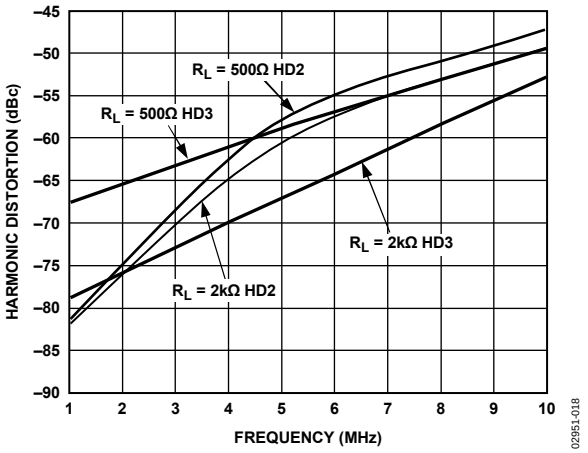


Figure 18. Harmonic Distortion vs. Frequency for Various Loads, V_S = 5 V, V_{OUT} = 2 V p-p, G = +2

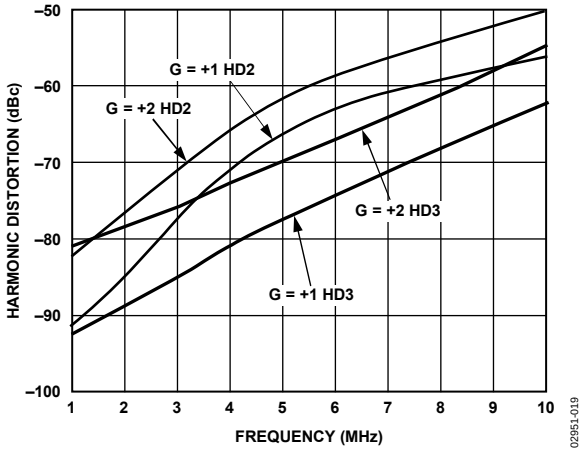


Figure 19. Harmonic Distortion vs. Frequency for Various Gains, V_S = ±5 V, V_{OUT} = 2 V p-p

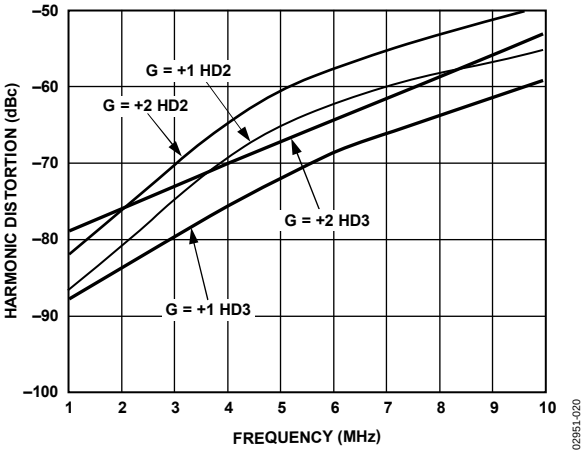


Figure 20. Harmonic Distortion vs. Frequency for Various Gains, V_S = 5 V, V_{OUT} = 2 V p-p

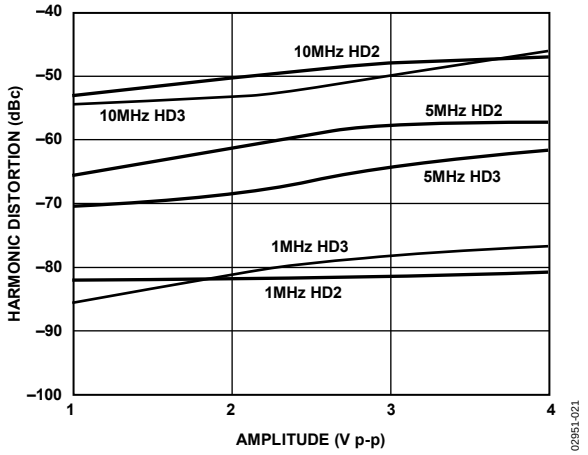


Figure 21. Harmonic Distortion vs. V_{OUT} Amplitude for Various Frequencies, V_S = ±5 V, G = +2

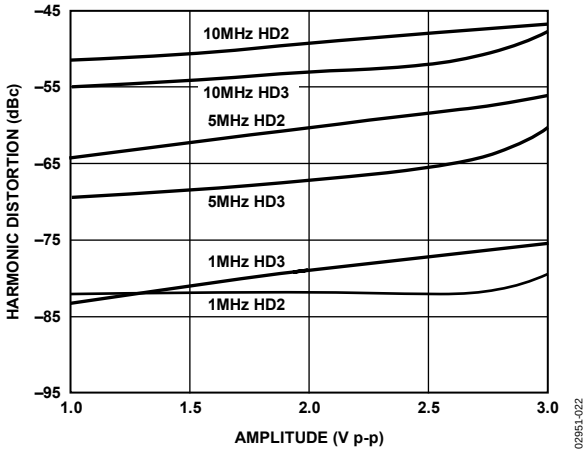


Figure 22. Harmonic Distortion vs. Amplitude for Various Frequencies, V_S = 5 V, G = +2

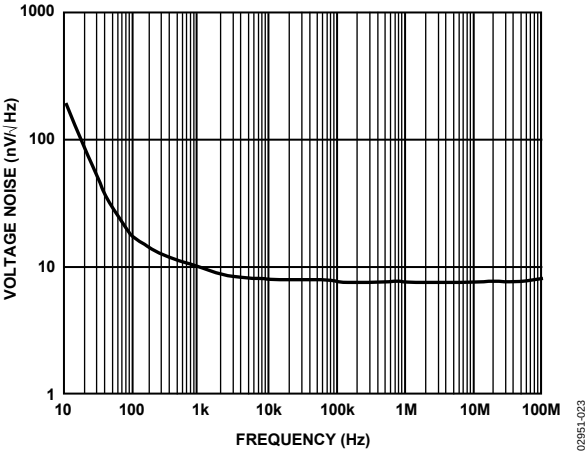


Figure 23. Input Voltage Noise vs. Frequency

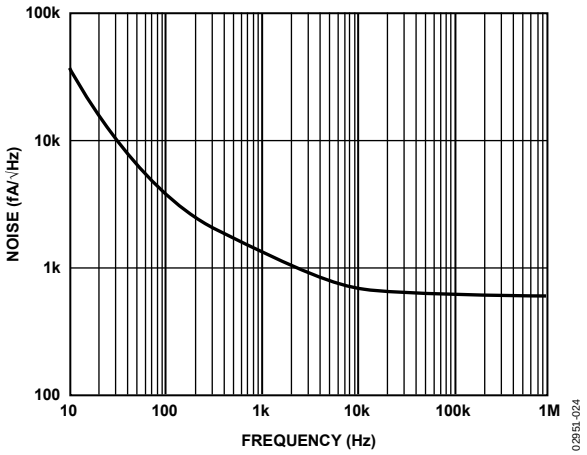


Figure 24. Input Current Noise vs. Frequency

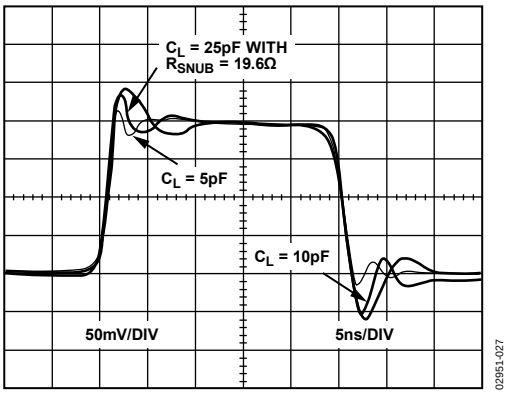


Figure 27. Small Signal Transient Response for Various C_L, V_S = 5 V

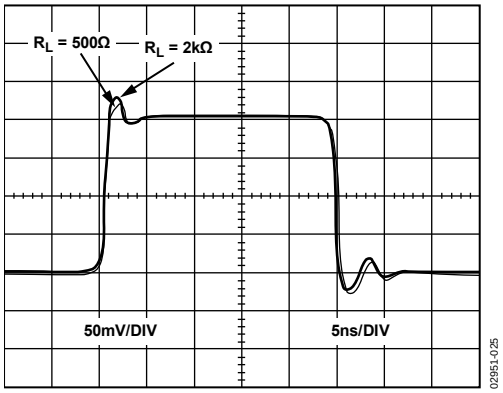


Figure 25. Small Signal Transient Response for Various R_L, V_S = 5 V

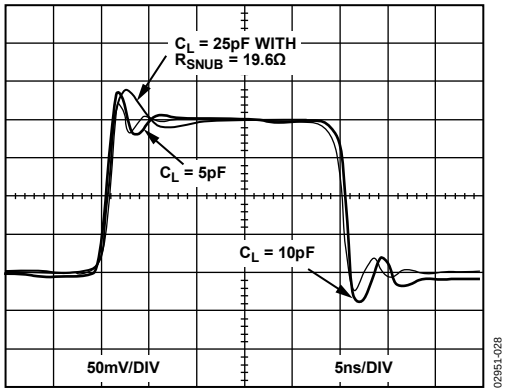


Figure 28. Small Signal Transient Response for Various C_L, V_S = ±5 V

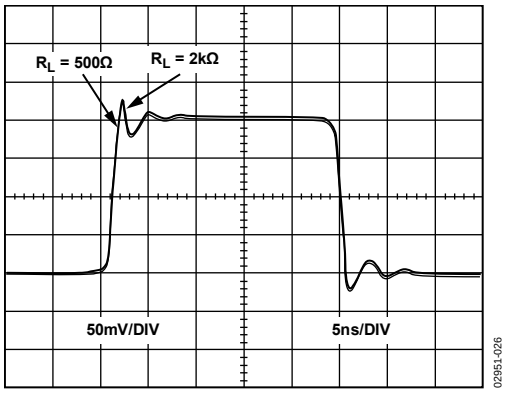


Figure 26. Small Signal Transient Response for Various R_L, V_S = ±5 V

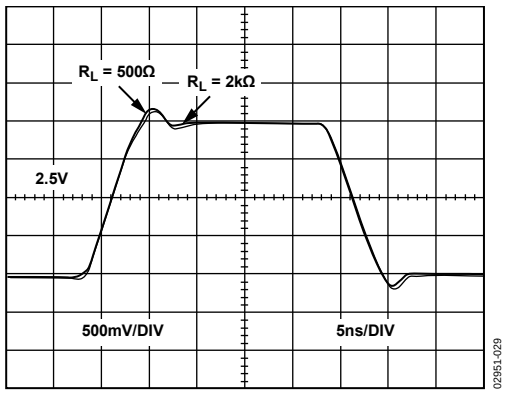


Figure 29. Large Signal Transient Response for Various R_L, V_S = 5 V

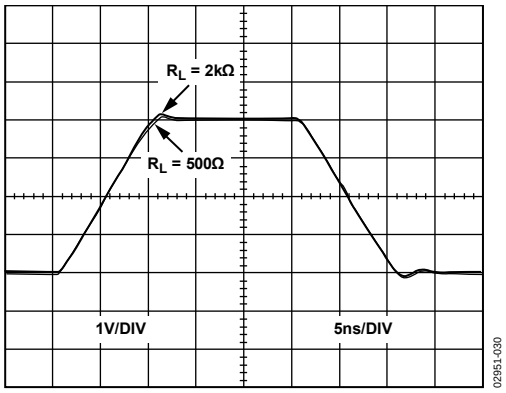


Figure 30. Large Signal Transient Response for Various R_L, V_S = ±5 V

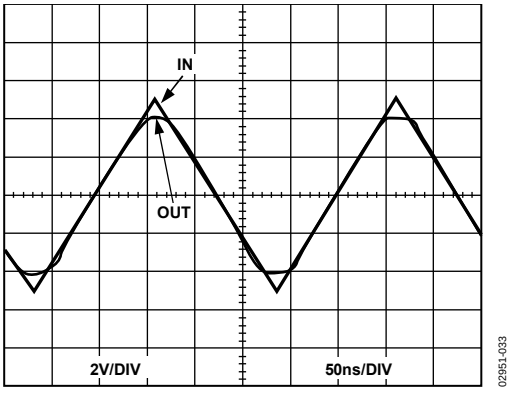


Figure 33. Input Overdrive Recovery, Gain = +1

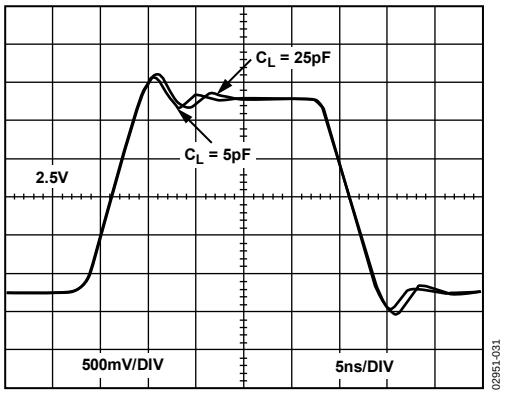


Figure 31. Large Signal Transient Response for Various C_L, V_S = 5 V

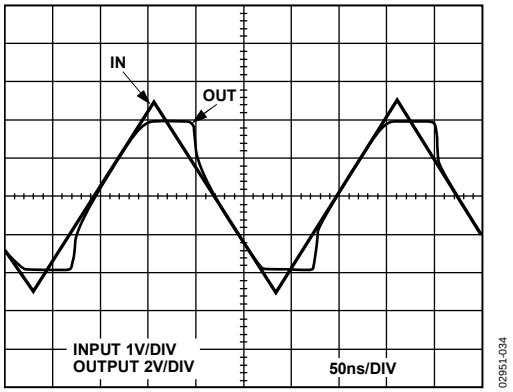


Figure 34. Output Overdrive Recovery, Gain = +2

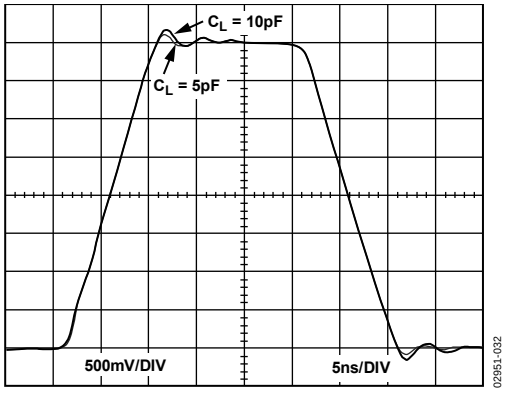


Figure 32. Large Signal Transient Response for Various C_L, V_S = ±5 V

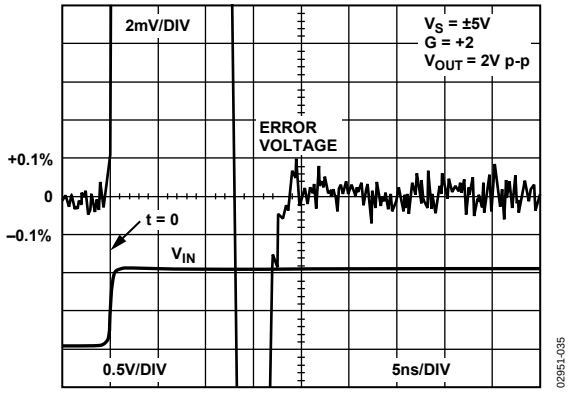


Figure 35. 0.1% Settling Time V_{OUT} = 2 V p-p

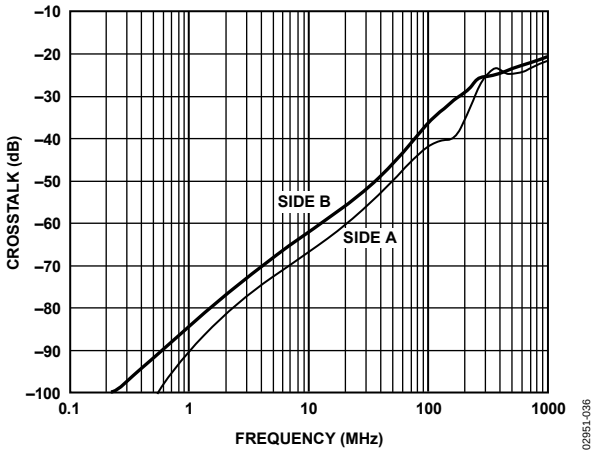


Figure 36. AD8039 Crosstalk, V_{IN} = 1 V p-p, Gain = +1

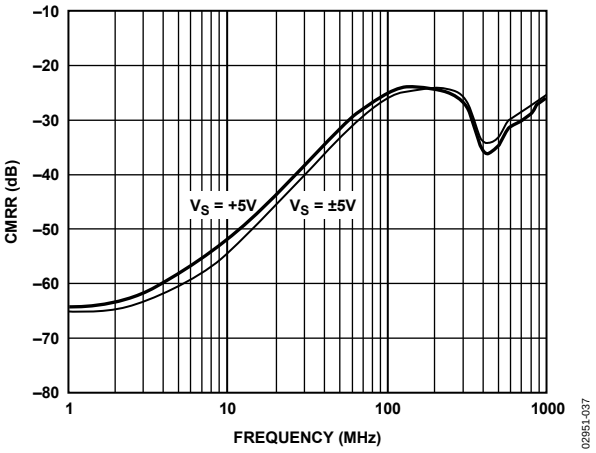


Figure 37. CMRR vs. Frequency, V_{IN} = 1 V p-p

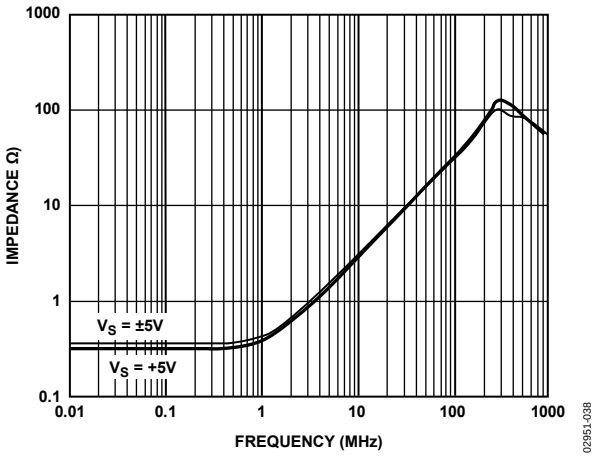


Figure 38. Output Impedance vs. Frequency

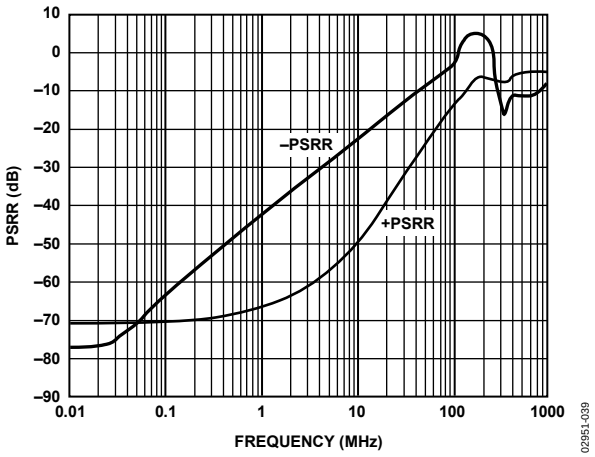


Figure 39. PSRR vs. Frequency

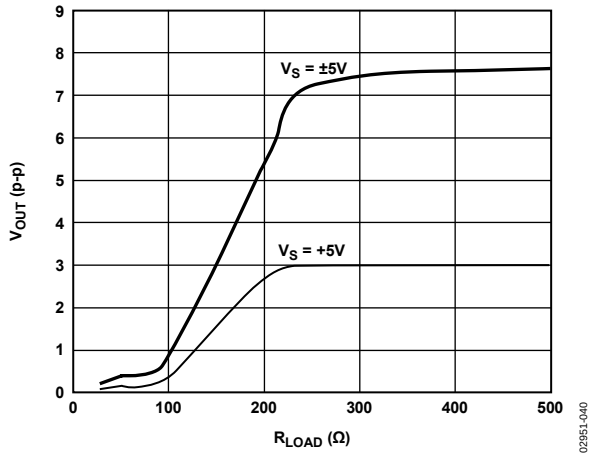


Figure 40. Output Swing vs. Load Resistance

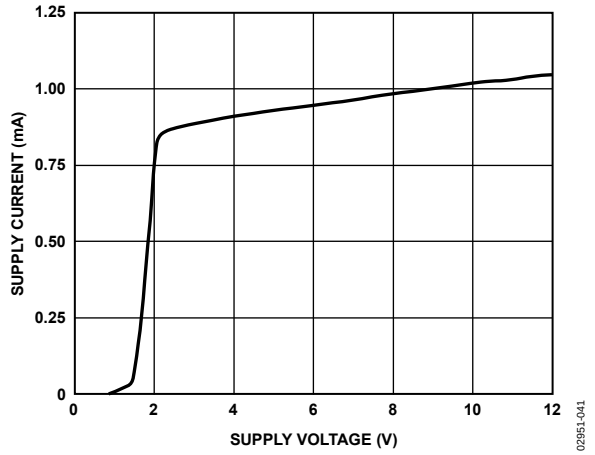


Figure 41. AD8038 Supply Current vs. Supply Voltage

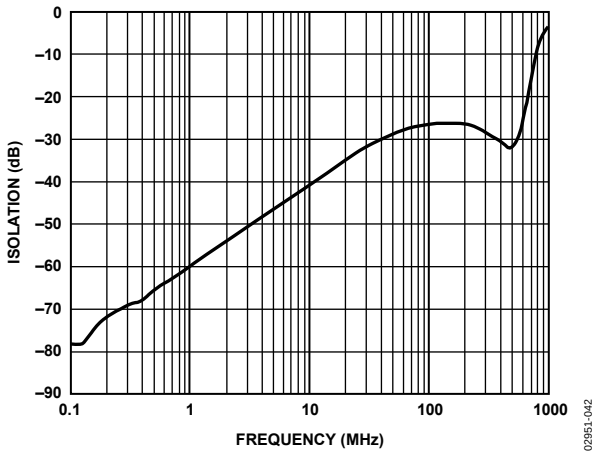


Figure 42. AD8038 Input-Output Isolation ($G = +2$, $R_L = 2\ k\Omega$, $V_S = \pm 5\ V$)

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

DISABLE

The AD8038 in the 8-lead SOIC package provides a disable feature. This feature disables the input from the output (see Figure 42 for input-output isolation) and reduces the quiescent current from typically 1 mA to 0.2 mA. When the $\overline{\text{DISABLE}}$ node is pulled below 4.5 V from the positive supply rail, the part becomes disabled. To enable the part, the $\overline{\text{DISABLE}}$ node needs to be pulled to greater than (V_S – 2.5).

POWER SUPPLY BYPASSING

Power supply pins are actually inputs, and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering a majority of the noise.

Decoupling schemes are designed to minimize the bypassing impedance at all frequencies with a parallel combination of capacitors. The 0.01 µF or 0.001 µF (X7R or NPO) chip capacitors are critical and should be placed as close as possible to the amplifier package. Larger chip capacitors, such as 0.1 µF capacitors, can be shared among a few closely spaced active components in the same signal path. A 10 µF tantalum capacitor is less critical for high frequency bypassing and, in most cases, only one per board is needed at the supply inputs.

GROUNDING

A ground plane layer is important in densely packed PC boards to spread the current minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise.

The length of the high frequency bypass capacitor leads is most critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few picofarads of capacitance reduces the input impedance at high frequencies, in turn increasing the gain of the amplifiers, causing peaking of the frequency response, or even oscillations if severe enough. It is recommended that the external passive components that are connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

OUTPUT CAPACITANCE

To a lesser extent, parasitic capacitances on the output can cause peaking of the frequency response. Two methods to minimize this effect include the following:

- Put a small value resistor in series with the output to isolate the load capacitor from the output stage of the amplifier, see Figure 12, Figure 13, Figure 27, and Figure 28.
- Increase the phase margin with higher noise gains or add a pole with a parallel resistor and capacitor from –IN to the output.

INPUT-TO-OUTPUT COUPLING

The input and output signal traces should not be parallel to minimize capacitive coupling between the inputs and outputs, avoiding any positive feedback.

APPLICATIONS INFORMATION

LOW POWER ADC DRIVER

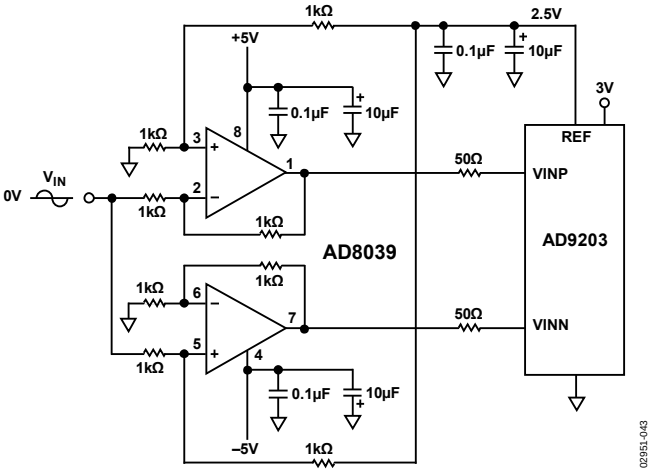


Figure 43. Schematic to Drive AD9203 with the AD8039

The AD9203 is a low power (125 mW on a 5 V supply), 40 MSPS 10-bit converter. As such, the low power, high performance AD8039 is an appropriate amplifier choice to drive it.

In low supply voltage applications, differential analog inputs are needed to increase the dynamic range of the ADC inputs. Differential driving can also reduce second and other even-order distortion products. The AD8039 can be used to make a dc-coupled, single-ended-to-differential driver for driving these ADCs. Figure 43 is a schematic of such a circuit for driving the AD9203, 10-bit, 40 MSPS ADC.

The AD9203 works best when the common-mode voltage at the input is at the midsupply or 2.5 V. The output stage design of the AD8039 makes it ideal for driving these types of ADCs.

In this circuit, one of the op amps is configured in the inverting mode, and the other is in the noninverting mode. However, to provide better bandwidth matching, each op amp is configured for a noise gain of +2. The inverting op amp is configured for a gain of −1, and the noninverting op amp is configured for a gain of +2. Each has a very similar ac response. The input signal to the noninverting op amp is divided by 2 to normalize its voltage level and make it equal to the inverting output.

The outputs of the op amps are centered at 2.5 V, which is the midsupply level of the ADC. This is accomplished by first taking the 2.5 V reference output of the ADC and dividing it by 2 with a pair of 1 kΩ resistors. The resulting 1.25 V is applied to the positive input of each op amp. This voltage is then multiplied by the gain of the op amps to provide a 2.5 V level at each output.

LOW POWER ACTIVE VIDEO FILTER

Some composite video signals derived from a digital source contain clock feedthrough that can limit picture quality. Active filters made from op amps can be used in this application, but they consume 25 mW to 30 mW for each channel. In power-sensitive applications, this can be too much, requiring the use of passive filters that can create impedance matching problems when driving any significant load.

The AD8038 can be used to make an effective low-pass active filter that consumes one-fifth of the power consumed by an active filter made from an op amp. Figure 44 shows a circuit that uses a AD8038 with ±2.5 V supplies to create a three-pole Sallen-Key filter. This circuit uses a single RC pole in front of a standard 2-pole active section.

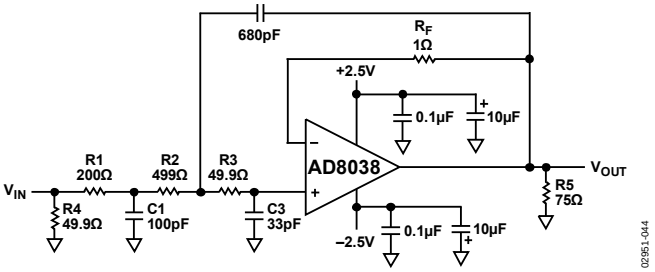


Figure 44. Low-Pass Filter for Video

Figure 45 shows the frequency response of this filter. The response is down 3 dB at 6 MHz; therefore, it passes the video band with little attenuation. The rejection at 27 MHz is 45 dB, which provides more than a factor of 100 in suppression of the clock components at this frequency.

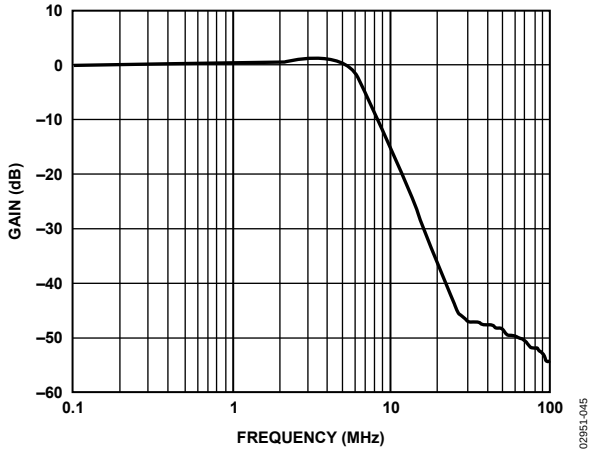


Figure 45. Video Filter Response

OUTLINE DIMENSIONS

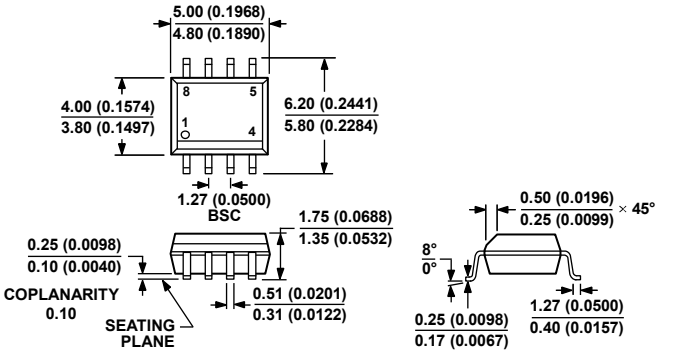


Figure 46. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

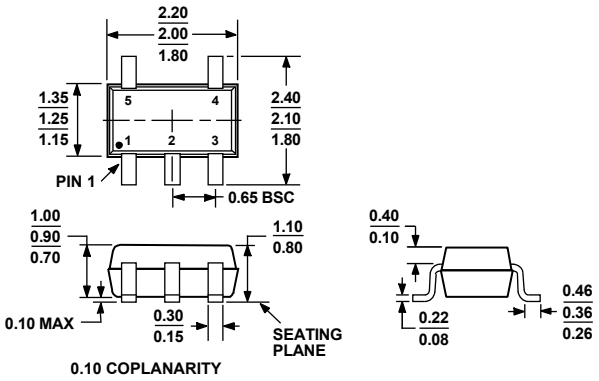
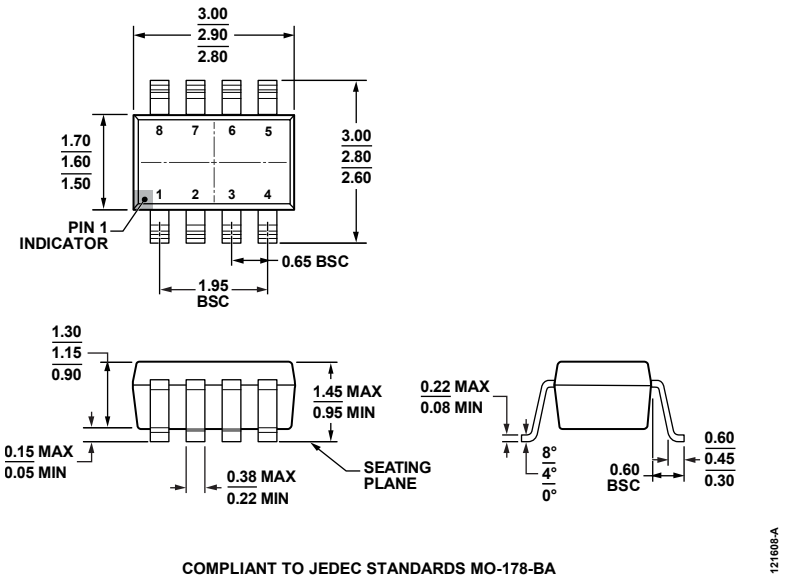


Figure 47. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 48. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8038AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038ARZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038AKSZ-R2[1]	−40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	H1C
AD8038AKSZ-REEL[1]	−40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	H1C
AD8038AKSZ-REEL7[1]	−40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	H1C
AD8039AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8039AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8039AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8039ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8039ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8039ARZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8039ART-R2	−40°C to +85°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	HYA
AD8039ART-REEL	−40°C to +85°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	HYA
AD8039ART-REEL7	−40°C to +85°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	HYA
AD8039ARTZ-R2[1]	−40°C to +85°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	HYA#
AD8039ARTZ-REEL[1]	−40°C to +85°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	HYA#
AD8039ARTZ-REEL7[1]	−40°C to +85°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	HYA#

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked..

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