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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V, load resistance (R_L) = 25 Ω connected to V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC PERFORMANCE					V_{DD} = 3.6 V to 4.5 V; device operates over 2.7 V to 5.5 V with reduced performance
Resolution		10		Bits	117 µA/LSB
Relative Accuracy[2]		±1.5	±4	LSB	
Differential Nonlinearity[2, 3]			±1	LSB	Guaranteed monotonic over all codes
Zero-Code Error[2, 4]	0	0.5	1	mA	All 0s loaded to DAC
Offset Error @ Code 16[2]		0.5		mA	
Gain Error[2]			±0.6	% of FSR	at 25°C
Offset Error Drift[4, 5]		10		µA/°C	
Gain Error Drift[2, 5]		±0.2	±0.5	LSB/°C	
OUTPUT CHARACTERISTICS					
Minimum Sink Current[4]		3		mA	
Maximum Sink Current		120		mA	
Output Current During XSHUTDOWN[5]		80		nA	XSHUTDOWN = 0
Output Compliance[5]	0.6		V_{DD}	V	Output voltage range over which maximum 120 mA sink current is available
Output Compliance[5]	0.48		V_{DD}	V	Output voltage range over which 90 mA sink current is available
Power-Up Time[5]		20		µs	To 10% of FS, coming out of power-down mode; V_{DD} = 5 V
LOGIC INPUTS (XSHUTDOWN)[5]					
Input Current			±1	µA	
Input Low Voltage, V_{INL}			0.54	V	V_{DD} = 2.7 V to 5.5 V
Input High Voltage, V_{INH}	1.26			V	V_{DD} = 2.7 V to 5.5 V
Pin Capacitance		3		pF	
LOGIC INPUTS (SCL, SDA)[5]					
Input Low Voltage, V_{INL}	−0.3		+0.54	V	V_{DD} = 2.7 V to 3.6 V
Input High Voltage, V_{INH}	1.26		V_{DD} + 0.3	V	V_{DD} = 2.7 V to 3.6 V
Input Low Voltage, V_{INL}	−0.3		+0.54	V	V_{DD} = 3.6 V to 5.5 V
Input High Voltage, V_{INH}	1.4		V_{DD} + 0.3	V	V_{DD} = 3.6 V to 5.5 V
Input Leakage Current, I_{IN}			±1	µA	V_{IN} = 0 V to V_{DD}
Input Hysteresis, V_{HYST}	0.05 V_{DD}			V	
Digital Input Capacitance, C_{IN}		6		pF	
Glitch Rejection[6]			50	ns	Pulse width of spike suppressed
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)		0.5	1	mA	I_{DD} specification is valid for all DAC codes; V_{INH} = 1.8 V, V_{INL} = GND, V_{DD} = 2.7 V to 3.6 V
I_{DD} (Power-Down Mode)[7]		0.5		µA	V_{INH} = 1.8 V, V_{INL} = GND, V_{DD} = 3 V

[1] Temperature range for the B version is −30°C to +85°C.
[2] See the Terminology section.
[3] Linearity is tested using a reduced code range: Code 32 to Code 1023.
[4] To achieve near zero output current, use the power-down feature.
[5] Guaranteed by design and characterization; not production tested. XSHUTDOWN is active low. SDA and SCL pull-up resistors are tied to 1.8 V.
[6] Input filtering on both the SCL and the SDA inputs suppress noise spikes that are less than 50 ns.
[7] XSHUTDOWN is active low.

AC SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V, R_L = 25 Ω connected to V_{DD}, unless otherwise noted.

Table 2.

Parameter	B Version[1, 2] Min	Typ	Max	Unit	Test Conditions/Comments
Output Current Settling Time		250		µs	V_{DD} = 3.6 V, R_L = 25 Ω, L_L = 680 µH, ¼ scale to ¾ scale change (0x100 to 0x300)
Slew Rate		0.3		mA/µs	
Major Code Change Glitch Impulse		0.15		nA-sec	1 LSB change around major carry
Digital Feedthrough[3]		0.06		nA-sec	

[1] Temperature range for the B version is −40°C to +85°C.
[2] Guaranteed by design and characterization; not production tested.
[3] See the Terminology section.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	B Version Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[2]	0.9	µs max	$t_{HD, DAT}$, data hold time
	0	µs min	
t_7	0.6	µs min	$t_{SU, STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}	300	ns max	t_R, rise time of both SCL and SDA when receiving
	0	ns min	Can be CMOS driven
t_{11}	250	ns max	t_F, fall time of SDA when receiving
	300	ns max	t_F, fall time of both SCL and SDA when transmitting
	20 + 0.1 C_B[3]	ns min	
C_B	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization; not production tested.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{INH\ MIN}$ of the SCL signal) to bridge the undefined region of the SCL falling edge.
[3] C_B is the total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 V_{DD} and 0.7 V_{DD}.

Timing Diagram

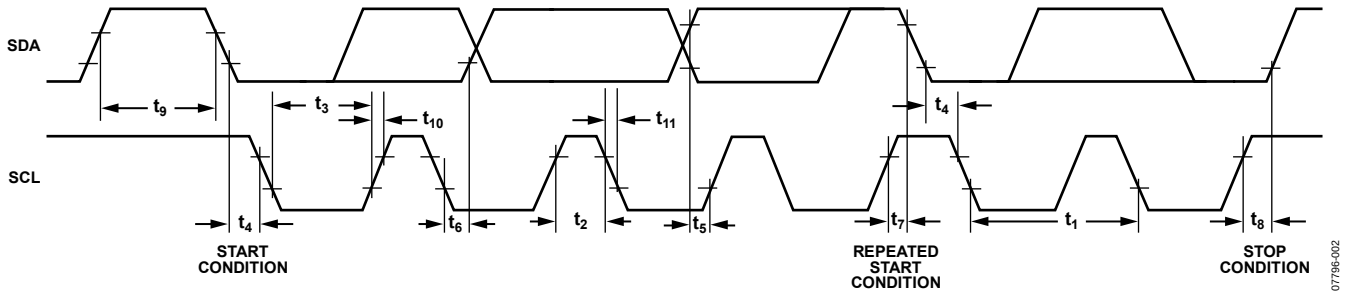

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +5.5 V
V_{DD} to DGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
SCL, SDA to DGND	−0.3 V to V_{DD} + 0.3 V
XSHUTDOWN to DGND	−0.3 V to V_{DD} + 0.3 V
I_{SINK} to AGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−30°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
WLCSP Power Dissipation	($T_{J\ MAX} - T_A$)/θ_{JA}
θ_{JA} Thermal Impedance[1]	
Mounted on 4-Layer Board	95°C/W
Lead Temperature, Soldering	
Maximum Peak Reflow Temperature[2]	260°C (±5°C)

[1] To achieve the optimum θ_{JA}, it is recommended that the AD5821A be soldered on a 4-layer board.
[2] As per JEDEC J-STD-020C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

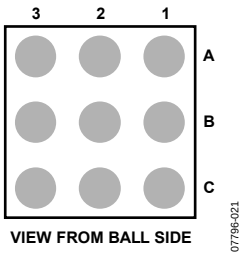

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Mnemonic	Description
A1	I_{SINK}	Output Current Sink.
A2	NC	No Connection.
A3	XSHUTDOWN	Power-Down. Asynchronous power-down signal, active low.
B1	AGND	Analog Ground Pin.
B2	DGND	Digital Ground Pin.
B3	SDA	I^2C Interface Signal.
C1	DGND	Digital Ground Pin.
C2	V_{DD}	Digital Supply Voltage.
C3	SCL	I^2C Interface Signal.

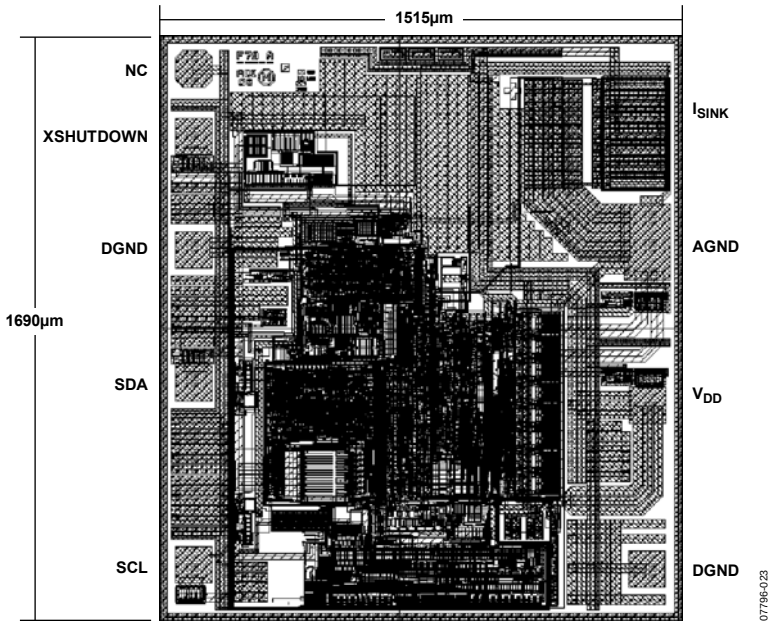

Figure 4. Metallization Photo
Dimensions shown in microns (µm)

TYPICAL PERFORMANCE CHARACTERISTICS

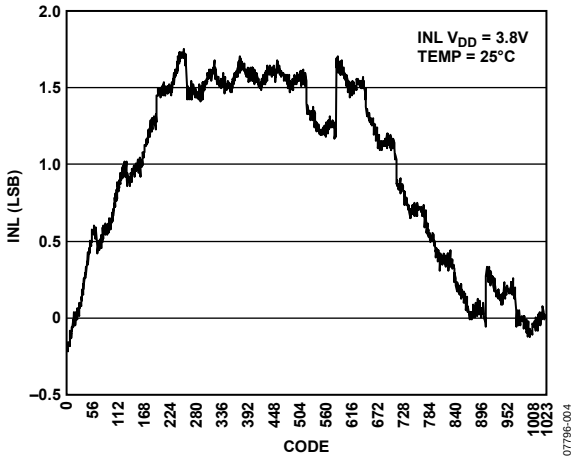

Figure 5. Typical INL vs. Code Plot

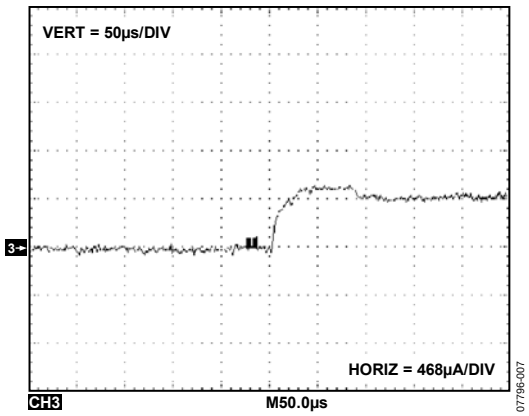

Figure 8. Settling Time for a 4-LSB Step (V_{DD} = 3.6 V)

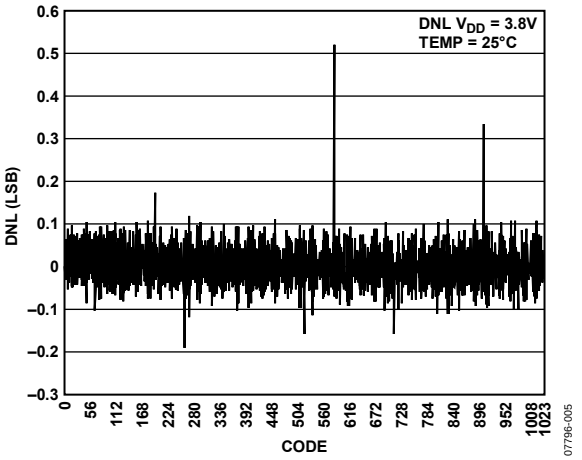

Figure 6. Typical DNL vs. Code Plot

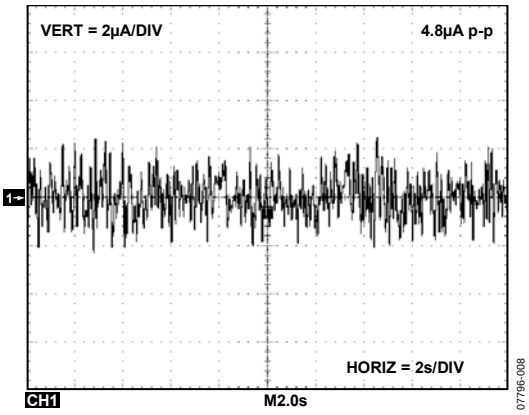

Figure 9. 0.1 Hz to 10 Hz Noise Plot (V_{DD} = 3.6 V)

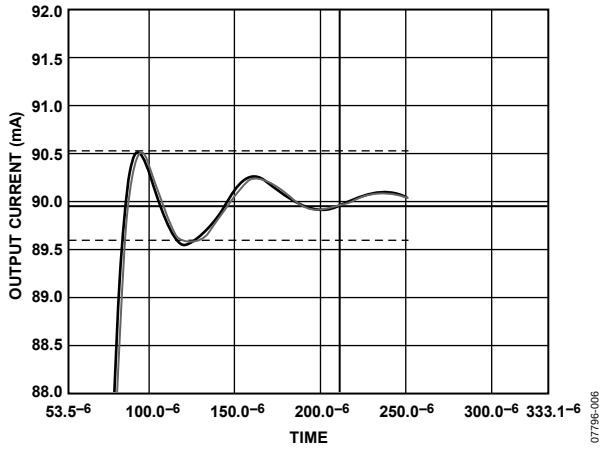

Figure 7. ¼ to ¾ Scale Settling Time (V_{DD} = 3.6 V)

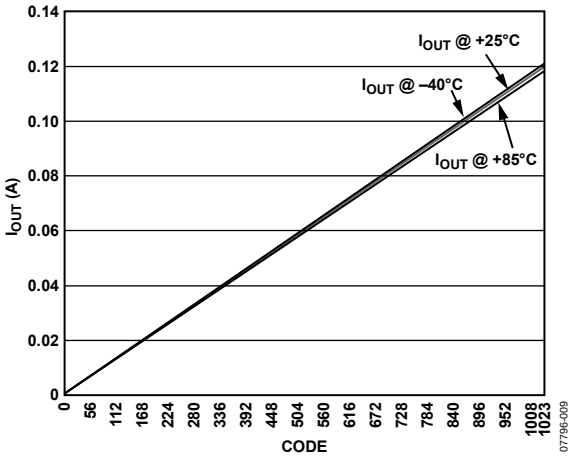

Figure 10. Sink Current vs. Code vs. Temperature (V_{DD} = 3.6 V)

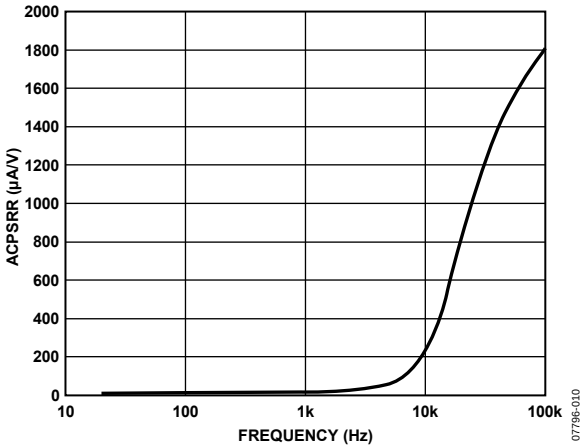

Figure 11. AC Power Supply Rejection Ratio (V_{DD} = 3.6 V)

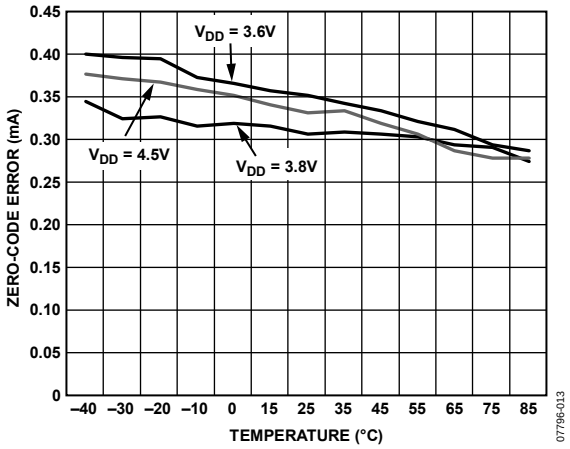

Figure 14. Zero-Code Error vs. Temperature vs. Supply Voltage

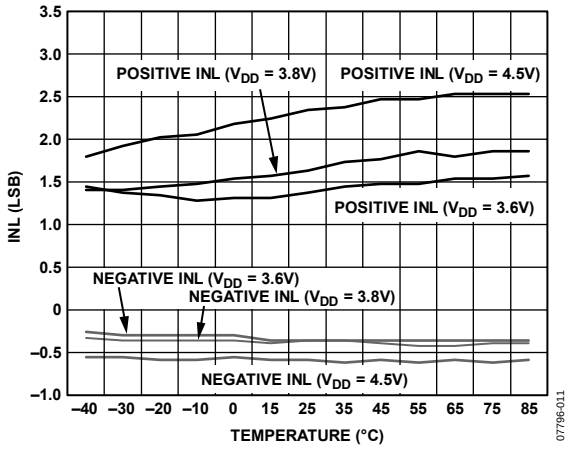

Figure 12. INL vs. Temperature vs. Supply Voltage

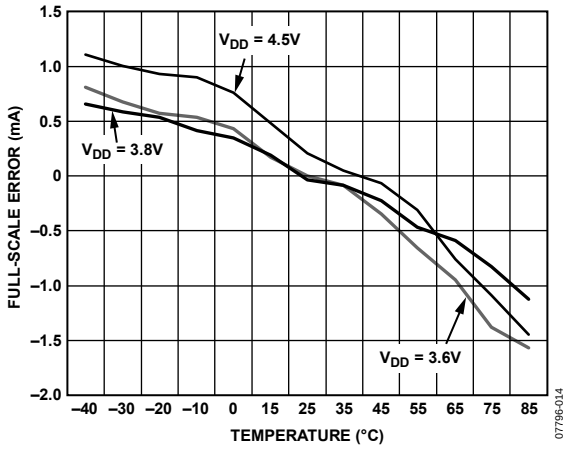

Figure 15. Full-Scale Error vs. Temperature vs. Supply Voltage

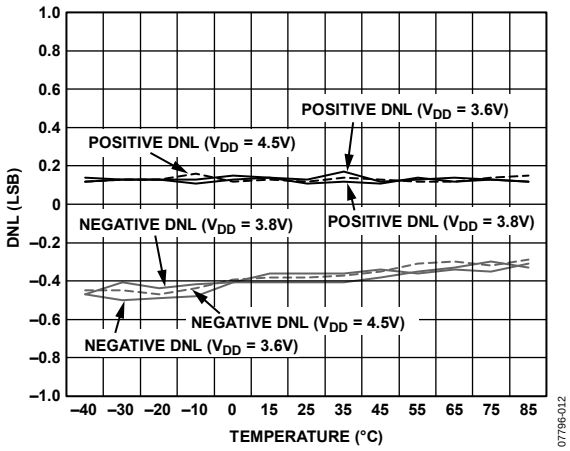

Figure 13. DNL vs. Temperature vs. Supply Voltage

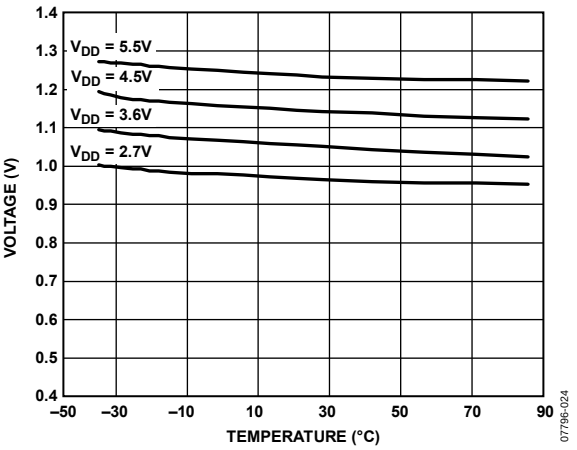

Figure 16. SCL and SDA Logic High Level (V_{INH}) vs. Temperature and Supply Voltage

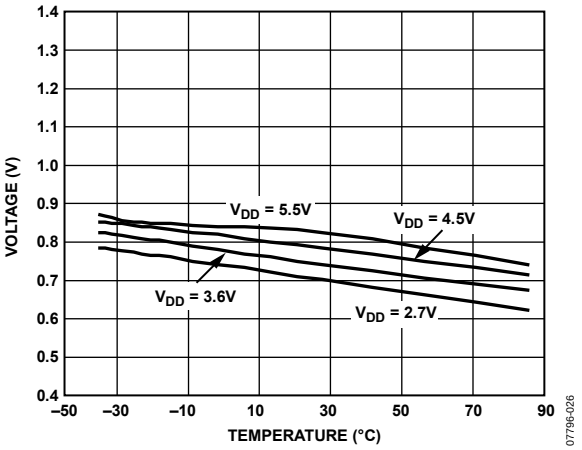

Figure 17. SCL and SDA Logic Low Level (V_{INL}) vs. Temperature and Supply Voltage

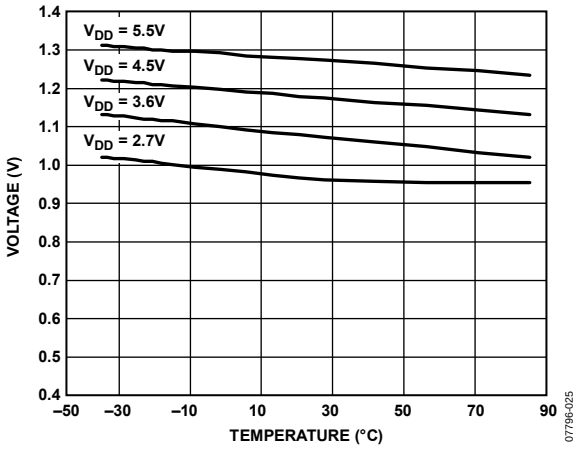

Figure 18. XSHUTDOWN Logic High Level (V_{INH}) vs. Temperature and Supply Voltage

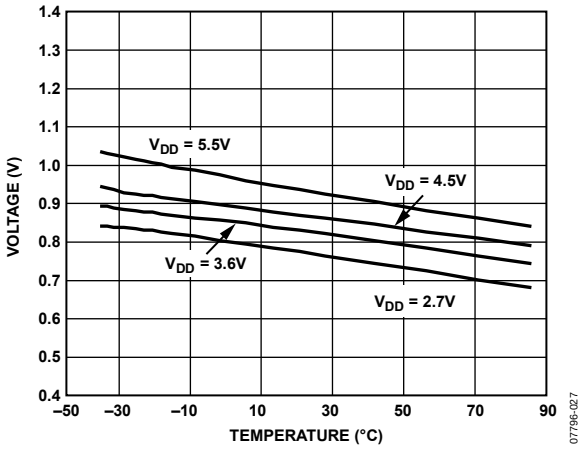

Figure 19. DNL vs. XSHUTDOWN Logic Low Level (V_{INL}) vs. Temperature and Supply Voltage

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measurement of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 5.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 6.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 mA. The zero-code error is always positive in the AD5821A because the output of the DAC cannot go below 0 mA. This is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in milliamperes (mA).

Gain Error
Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percent of the full-scale range.

Gain Error Drift
Gain error drift is a measurement of the change in gain error with changes in temperature. It is expressed in LSB/°C.

Digital-to-Analog Glitch Impulse
This is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanoampere seconds (nA-sec) and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. It is specified in nanoampere seconds (nA-sec) and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Offset Error
Offset error is a measurement of the difference between I_{SINK} (actual) and I_{OUT} (ideal) in the linear region of the transfer function, expressed in milliamperes (mA). Offset error is measured on the AD5821A with Code 16 loaded into the DAC register.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in microvolts per degree Celsius (μV/°C).

THEORY OF OPERATION

The AD5821A is a fully integrated, 10-bit DAC with 120 mA output current sink capability. It is intended for driving voice coil actuators in applications such as lens autofocus, image stabilization, and optical zoom. The circuit diagram is shown in Figure 20. A 10-bit current output DAC coupled with Resistor R generates the voltage that drives the noninverting input of the operational amplifier. This voltage also appears across the R_{SENSE} resistor and generates the sink current required to drive the voice coil.

Resistor R and Resistor R_{SENSE} are interleaved and matched. Therefore, the temperature coefficient and any nonlinearities over temperature are matched, and the output drift over temperature is minimized. Diode D1 is an output protection diode.

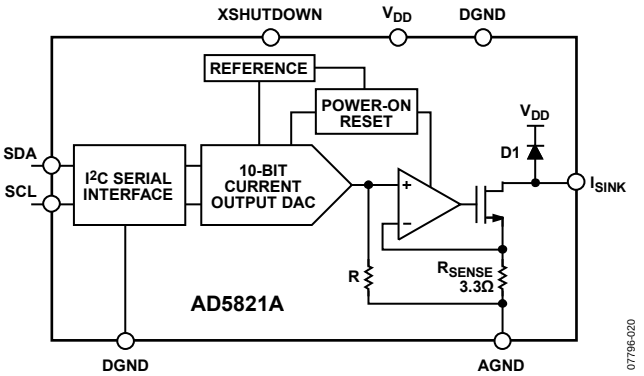

Figure 20. Block Diagram Showing Connection to Voice Coil

SERIAL INTERFACE

The AD5821A is controlled using the industry-standard I²C 2-wire serial protocol. Data can be written to or read from the DAC at data rates of up to 400 kHz. After a read operation, the contents of the input register are reset to all 0s.

I²C BUS OPERATION

An I²C bus operates with one or more master devices that generate the serial clock (SCL) and read and write data on the serial data line (SDA) to and from slave devices such as the AD5821A. On all devices on an I²C bus, the SDA pin is connected to the SDA line and the SCL pin connected to the SCL line of the master device. I²C devices can only pull the bus lines low; pulling high is achieved by pull-up resistors, R_P. The value of R_P depends on the data rate, bus capacitance, and the maximum load current that the I²C device can sink (3 mA for a standard device).

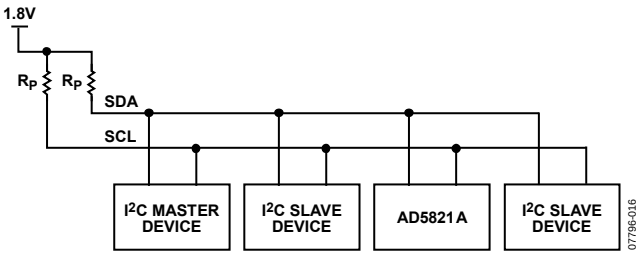

Figure 21. Typical I²C Bus

When the bus is idle, SCL and SDA are both high. The master device initiates a serial bus operation by generating a start condition, which is defined as a high-to-low transition on the SDA low while SCL is high. The slave device connected to the bus responds to the start condition and shifts in the next eight data bits under control of the serial clock.

These eight data bits consist of a 7-bit address, plus a read/write ($R/\overline{W}$) bit that is 0 if data is to be written to a device, and 1 if data is to be read from a device. Each slave device on an I²C bus must have a unique address. The address of the AD5821A is 0001100; however, 0001101, 0001110, and 0001111 address the part because the last two bits are unused/don't cares (see Figure 22 and Figure 23). Because the address plus the $R/\overline{W}$ bit always equals eight bits of data, the write address of the AD5821A is 00011000 (0x18) and the read address is 00011001 (0x19) (see Figure 22 and Figure 23).

At the end of the address data, after the $R/\overline{W}$ bit, the slave device that recognizes its own address responds by generating an acknowledge (ACK) condition. This is defined as the slave device pulling SDA low while SCL is low before the ninth clock pulse and keeping it low during the ninth clock pulse. Upon receiving the ACK, the master device can clock data into the AD5821A in a write operation, or it can clock it out in a read operation. Data must change either during the low period of the clock (because SDA transitions during the high period define a start condition), or during a stop condition, as described in the Data Format section.

I²C data is divided into blocks of eight bits, and the slave generates an ACK at the end of each block. Because the AD5821A requires 10 bits of data, two data-words must be written to it when a write operation occurs, or read from it when a read operation occurs. At the end of a read or write operation, the AD5821A acknowledges the second data byte. The master generates a stop condition, defined as a low-to-high transition on SDA while SCL is high, to end the transaction.

DATA FORMAT

Data is written to the AD5821A high byte first, MSB first, and is shifted into the 16-bit input register. After all data is shifted in, data from the input register is transferred to the DAC register.

Because the DAC requires only 10 bits of data, not all bits of the input register data are used. The MSB is reserved for an active-high, software-controlled, power-down function.

The data format is shown in Table 6. When referring to this table, note that Bit 14 is unused; Bit 13 to Bit 4 correspond to the DAC data bits, D9 to D0; and Bit 3 to Bit 0 are unused.

During a read operation, data is read in the same bit order.

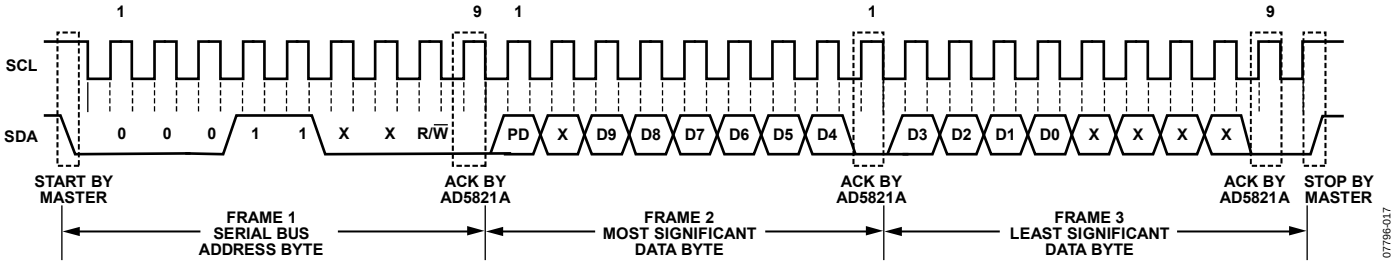

Figure 22. Write Operation

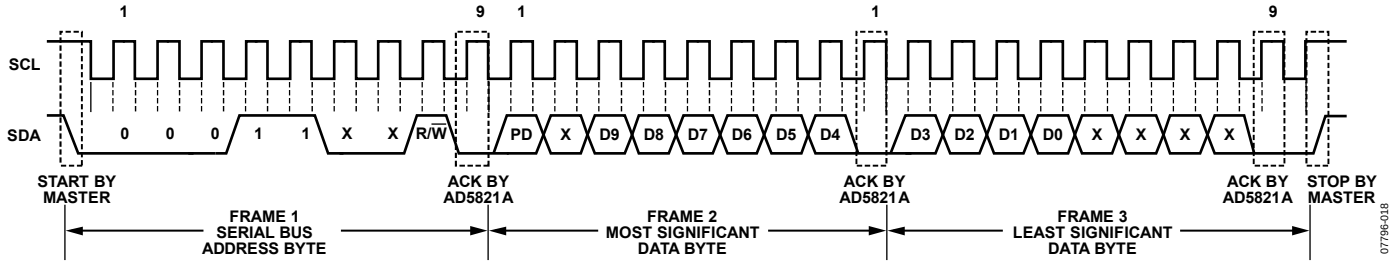

Figure 23. Read Operation

Table 6. Data Format

	High Byte								Low Byte							
Serial Data-Words	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Function	XSHUTDOWN[1]	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

[1] XSHUTDOWN = soft power-down; X = unused/don't care; and D9 to D0 = AC data.

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in an application, it is beneficial to consider power supply and ground return layout on the PCB. The PCB for the AD5821A should have separate analog and digital power supply sections. Where shared AGND and DGND is necessary, the connection of grounds should be made at only one point, as close as possible to the AD5821A.

Pay special attention to the layout of the AGND return path and, and trace it between the voice coil motor and I_{SINK} to minimize any series resistance. Figure 24 shows the output current sink of the AD5821A and illustrates the importance of reducing the effective series impedance of AGND and the trace resistance between the motor and I_{SINK}. The voice coil is modeled using Inductor L_C and Resistor R_C. The current through the voice coil is effectively a dc current that results in a voltage drop, V_{COIL}, when the AD5821A is sinking current. The effect of any series inductance is minimal.

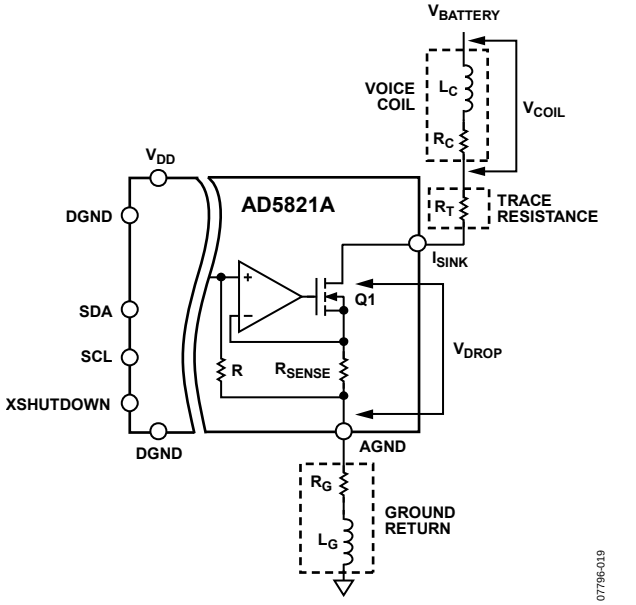

Figure 24. Effect of PCB Trace Resistance and Inductance

When sinking the maximum current of 120 mA, the maximum voltage drop allowed across R_{SENSE} is 400 mV, and the minimum drain to source voltage of Q1 is 200 mV. This means that the AD5821A output has a compliance voltage of 600 mV. If V_{DROP} falls below 600 mV, the output transistor, Q1, can no longer operate properly and I_{SINK} may not be maintained as a constant.

When sinking 90 mA, the maximum voltage drop allowed across R_{SENSE} is 300 mV, and the minimum drain to source voltage of Q1 is 180 mV. This means that the AD5821A output has a compliance voltage of 480 mV. If V_{DROP} falls below 480 mV, the output transistor, Q1, can no longer operate properly and I_{SINK} may not be maintained as a constant. As I_{SINK} decreases, the voltage required across the transistor, Q1, also decreases and, therefore, lower supplies can be used with the voice coil motor.

As the current increases to 120 mA through the voice coil, V_{COIL} increases. V_{DROP} decreases and eventually approaches the minimum specified compliance voltage of 600 mV (or 480 mV, if I_{SINK} = 90 mA). The ground return path is modeled by the components R_G and L_G. The trace resistance between the voice coil and the AD5821A is modeled as R_T. The inductive effects of L_G influence R_{SENSE} and R_C equally, and because the current is maintained as a constant, it is not as critical as the purely resistive component of the ground return path. When the maximum sink current is flowing through the motor, the resistive elements, R_T and R_G, may have an impact on the voltage headroom of Q1 and could, in turn, limit the maximum value of R_C because of voltage compliance.

For example, if

V_{BAT} = 3.6 V

R_G = 0.5 Ω

R_T = 0.5 Ω

I_{SINK} = 120 mA

V_{DROP} = 600 mV (compliance voltage)

Then the largest value of resistance of the voice coil, R_C, is

$$R_C = \frac{V_{BAT} - [V_{DROP} + (I_{SINK} \times R_T) + (I_{SINK} \times R_G)]}{I_{SINK}} =$$

$$\frac{3.6\text{ V} - [600\text{ mV} + 2 \times (120\text{ mA} \times 0.5\ \Omega)]}{120\text{ mA}} = 24\ \Omega$$

Using another example, if

V_{BAT} = 3.6 V

R_G = 0.5 Ω

R_T = 0.5 Ω

I_{SINK} = 90 mA

V_{DROP} = 480 mV (compliance voltage specification at 90 mA)

Then the largest value of resistance of the voice coil, R_C, is

$$R_C = \frac{V_{BAT} - [V_{DROP} + (I_{SINK} \times R_T) + (I_{SINK} \times R_G)]}{I_{SINK}} =$$

$$\frac{3.6\text{ V} - [480\text{ mV} + 2 \times (90\text{ mA} \times 0.5\ \Omega)]}{90\text{ mA}} = 33.66\ \Omega$$

For this reason, it is important to minimize any series impedance on both the ground return path and interconnect between the AD5821A and the motor. It is also important to note that for lower values of I_{SINK} the compliance voltage of the output stage also decreases. This decrease allows the user to either use voice coil motors with high resistance values or decrease the power supply voltage on the voice coil motor. The compliance voltage decreases as the I_{SINK} current decreases.

The power supply of the AD5821A, or the regulator used to supply the AD5821A, should be decoupled. Best practice power supply decoupling recommends that the power supply be decoupled with a 10 µF capacitor. Ideally, this 10 µF capacitor should be of a tantalum bead type. However, if the power supply or regulator supply is well regulated and clean, such decoupling may not be required. The AD5821A should be decoupled locally with a 0.1 µF ceramic capacitor, and this 0.1 µF capacitor should be located as close as possible to the V_{DD} pin. The 0.1 µF capacitor should be ceramic with a low effective series resistance and effective series inductance. The 0.1 µF capacitor provides a low impedance path to ground for high transient currents.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, they should run at right angles to each other to reduce feedthrough effects through the board. The best technique is to use a multilayer board with ground and power planes, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

APPLICATIONS INFORMATION

The AD5821A is designed to drive both spring-preloaded and nonspring linear motors used in applications such as lens autofocus, image stabilization, or optical zoom. The operation principle of the spring-preloaded motor is that the lens position is controlled by the balancing of a voice coil and spring. Figure 25 shows the transfer curve of a typical spring-preloaded linear motor for autofocus. The key points of this transfer function are displacement or stroke, which is the actual distance the lens moves in millimeters (mm) and the current through the motor, measured in milliamps (mA).

A start current is associated with spring-preloaded linear motors, which is a threshold current that must be exceeded for any displacement in the lens to occur. The start current is usually 20 mA or greater; the rated stroke or displacement is usually 0.25 mm to 0.4 mm; and the slope of the transfer curve is approximately 10 µm/mA or less.

The AD5821A is designed to sink up to 120 mA, which is more than adequate for available commercial linear motors or voice coils. Another factor that makes the AD5821A the ideal solution for these applications is the monotonicity of the device, ensuring that lens positioning is repeatable for the application of a given digital word.

Figure 26 shows a typical application circuit for the AD5821A.

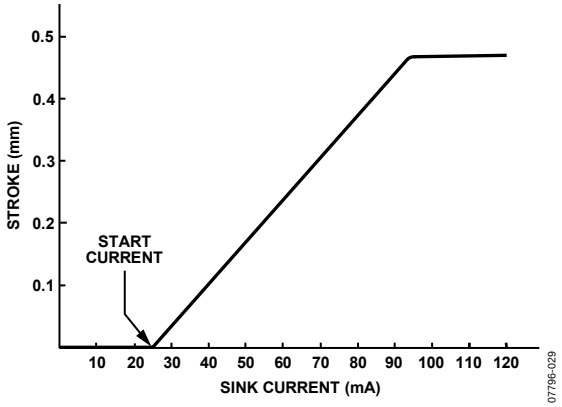

Figure 25. Spring-Preloaded Voice Coil Stroke vs. Sink Current

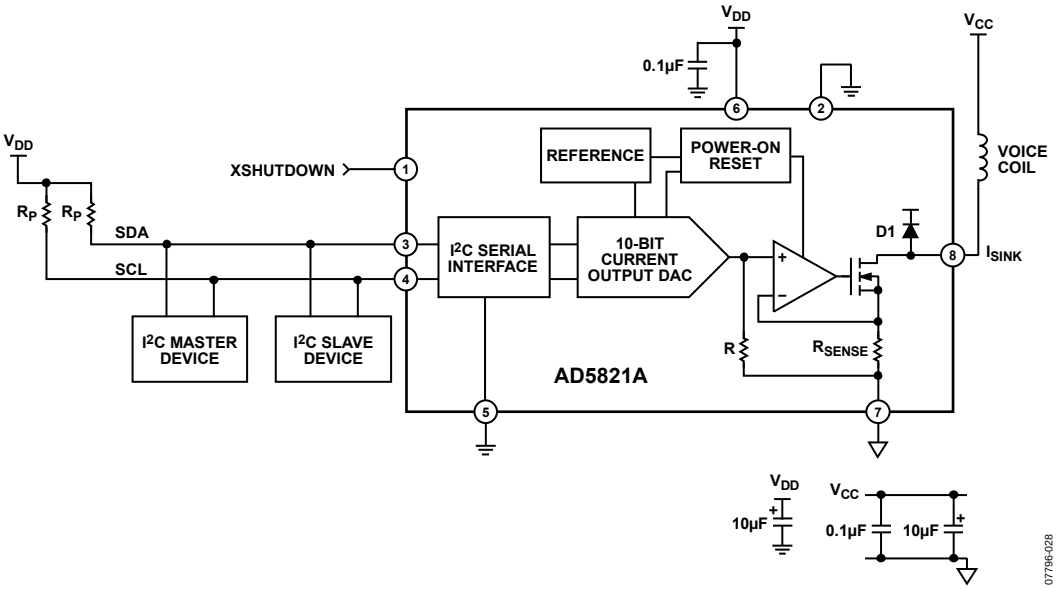

Figure 26. Typical Application Circuit

OUTLINE DIMENSIONS

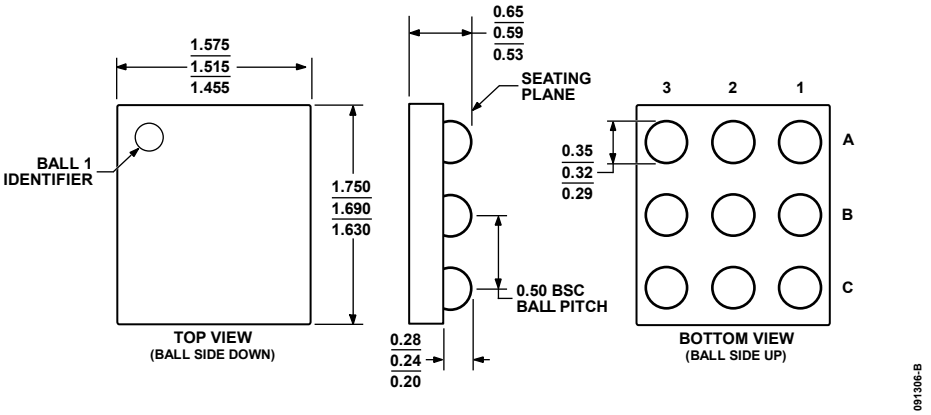

Figure 27. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD5821ABCBZ-REEL7[1]	−30°C to +85°C	9-Ball Wafer Level Chip Scale Package (WLCSP)	CB-9-1	1X
AD5821ABCBZ-REEL[1]	−30°C to +85°C	9-Ball Wafer Level Chip Scale Package (WLCSP)	CB-9-1	1X
AD5821A-WAFER	−40°C to +85°C	Bare Die Wafer		
AD5821AD-WAFER	−40°C to +85°C	Bare Die Wafer on Film		
EVAL-AD5821AEBZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES