AD5116* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- AD5116 Evaluation Board

Documentation

Application Notes

- AN-1291: Digital Potentiometers: Frequently Asked Questions

Data Sheet

- AD5116: Single-Channel, 64-Position, Push Button, ±8% Resistor Tolerance, Nonvolatile Digital Potentiometer Data Sheet

User Guides

- UG-324: Evaluation Board for the AD5116 Digital Potentiometer

Tools and Simulations

- AD5116 IBIS Model

Design Resources

- AD5116 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD5116 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

TABLE OF CONTENTS

REVISION HISTORY

11/12—Rev. A to Rev. B

Changed Low Power Consumption from 2.5 mA to 2.5 µA ... 1
Changed I_{DD} Unit from mA to µA, Table 2 ... 4

4/12—Rev. 0 to Rev. A

Changes to Features Section ... 1
Changes to Positive Supply Current, Table 2 ... 4
Changes to Ordering Guide ... 16

10/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

5 kΩ, 10 kΩ, and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		6			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 5 kΩ, V_{DD} = 2.3 V to 2.7 V	−2.5	±0.5	+2.5	LSB
		R_{AB} = 5 kΩ, V_{DD} = 2.7 V to 5.5 V	−1	±0.25	+1	LSB
		R_{AB} = 10 kΩ	−1	±0.25	+1	LSB
		R_{AB} = 80 kΩ	−0.25	±0.1	+0.25	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1	±0.25	+1	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.5	±0.15	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.15	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 5 kΩ	−2.5			LSB
		R_{AB} =10 kΩ	−1.5			LSB
		R_{AB} = 80 kΩ	−1			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 5 kΩ			+1.5	LSB
		R_{AB} =10 kΩ			+1	LSB
		R_{AB} = 80 kΩ			+0.25	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 5 kΩ, 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3, 6]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale, $V_W = V_A$ = 2.5 V or $V_W = V_B$ = 2.5 V		20		pF
Capacitance W[3, 6]	C_W	f = 1 MHz, measured to GND, code = half scale, $V_A = V_B$ = 2.5 V		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$		50		nA
DIGITAL INPUTS (PU AND PD)						
Input Logic[3]						
High	V_{INH}		2			V
Low	V_{INL}				0.8	V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUT ($\overline{ASE}$)						
Output High Voltage[3]	V_{OH}	I_{SINK} = 2 mA, V_{DD} = 5 V	4.8			V
Output Current[3]	I_O	V_{DD} = 5 V			16	mA
Three-State Leakage Current[3]	I_{OZ}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Positive Supply Current	I_{DD}	V_{DD} = 5 V		0.75	3.5	µA
		V_{DD} = 2.7 V			2.5	µA
		V_{DD} = 2.3 V			2.4	µA
EEMEM Store Current[3, 7]	$I_{DD\_NVM\_STORE}$			2		mA
EEMEM Read Current[3, 8]	$I_{DD\_NVM\_READ}$			320		µA
Power Dissipation[9]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		5		µW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 5 kΩ		−43		dB
		R_{AB} =10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB
DYNAMIC CHARACTERISTICS[3, 10]						
Bandwidth	BW	Code = half scale − 3 dB				
		R_{AB} = 5 kΩ		4		MHz
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2$ + 1 V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 5 kΩ		−75		dB
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				
		R_{AB} = 5 kΩ		2.5		µs
		R_{AB} = 10 kΩ		3		µs
		R_{AB} = 80 kΩ		10		µs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 5 kΩ		7		nV/√Hz
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		nV/√Hz
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[11]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to 0.8 × V_{DD}/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] C_A is measured with $V_W = V_A$ = 2.5 V, C_B is measured with $V_W = V_B$ = 2.5 V, and C_W is measured with $V_A = V_B$ = 2.5 V.
[7] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[8] Different from operating current; supply current for NVM read lasts approximately 20 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$).
[10] All dynamic characteristics use V_{DD} = 5.5 V, and V_{LOGIC} = 5 V.
[11] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[12] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

INTERFACE TIMING SPECIFICATIONS

V_{DD} = 2.3 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_1		8			ms	Debounce time
t_2		1			sec	Manual to auto scan time
t_3		140			ms	Auto scan step
t_4	$\overline{ASE}$ = 0 V, PD = GND, PU = GND	1			sec	Auto save execute time
t_5	$\overline{ASE}$ = V_{DD}	8			ms	Low pulse time to manual storage
$t_{EEPROM\_PROGRAM}$ [1]			15	50	ms	Memory program time
t_{POWER_UP} [2]				50	µs	Power-on EEPROM restore time

[1] EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at a lower temperature and higher write cycles.
[2] Maximum time after V_{DD} is equal to 2.3 V.

TIMING DIAGRAMS

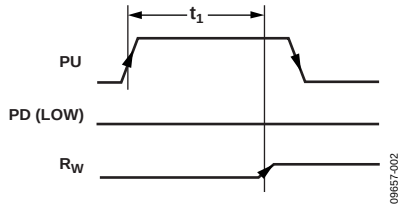

Figure 2. Manual Increment Mode Timing

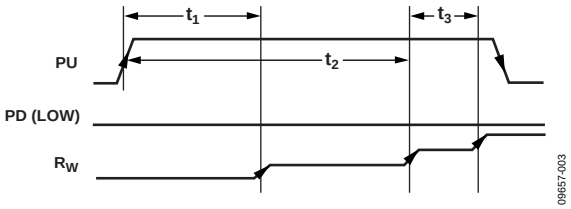

Figure 3. Auto Increment Mode Timing

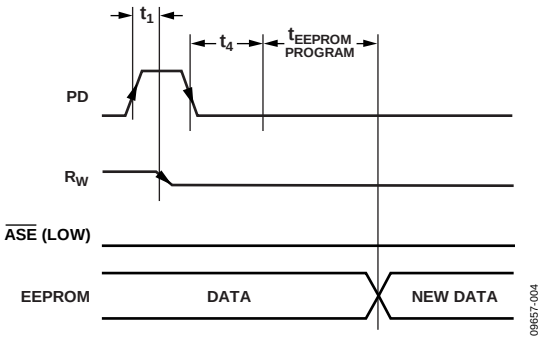

Figure 4. Auto Save Mode Timing

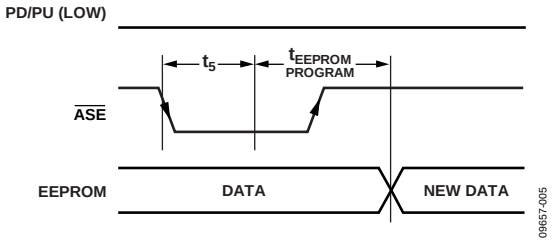

Figure 5. Manual Save Mode Timing

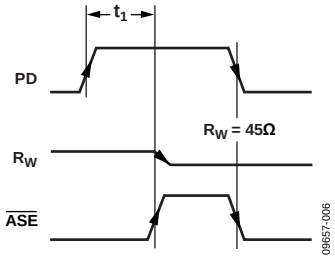

Figure 6. End Scale Indication Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_A, V_W, V_B to GND	GND − 0.3 V to V_{DD} + 0.3 V
I_A, I_W, I_B	
Pulsed[1]	
Frequency > 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/d[2]
R_{AW} = 80 kΩ	±1.5 mA/d[2]
Frequency ≤ 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/√d[2]
R_{AW} = 80 kΩ	±1.5 mA/√d[2]
Continuous	
R_{AW} = 5 kΩ and 10 kΩ	±6mA
R_{AW} = 80 kΩ	±1.5mA
Push Button Inputs	−0.3 V to +7 V or V_{DD} + 0.3 V (whichever is less)
Operating Temperature Range[3]	−40°C to +125°C
Maximum Junction Temperature (T_J Max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time At Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Pulse duty factor.
[3] Includes programming of EEPROM memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51, and the value is dependent on the test board and test environment.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	90[1]	25	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec air flow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

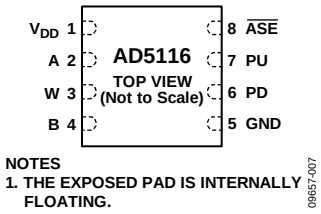

Figure 7. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. GND ≤ V_A ≤ V_{DD}.
3	W	Wiper terminal of RDAC. GND ≤ V_W ≤ V_{DD}.
4	B	Terminal B of RDAC. GND ≤ V_B ≤ V_{DD}.
5	GND	Ground Pin.
6	PD	Push-Down Pin. Connect to the external push button. Active high. An internal 100 kΩ pull-down resistor is connected to GND.
7	PU	Push-Up Pin. Connect to the external push button. Active high. An internal 100 kΩ pull-down resistor is connected to GND.
8	$\overline{ASE}$	Automatic Save Enable. Automatic save enable is configured at power-up. Active low. This pin requires a pull resistor connected between V_{DD} or GND. If $\overline{ASE}$ is enabled, this pin also indicates when the end scale (maximum or minimum resistance) has been reached.
	EPAD	Exposed Pad. The exposed pad is internally floating.

TYPICAL PERFORMANCE CHARACTERISTICS

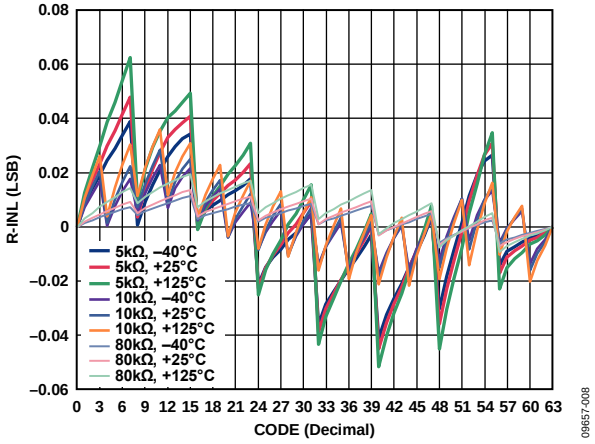

Figure 8. R-INL vs. Code

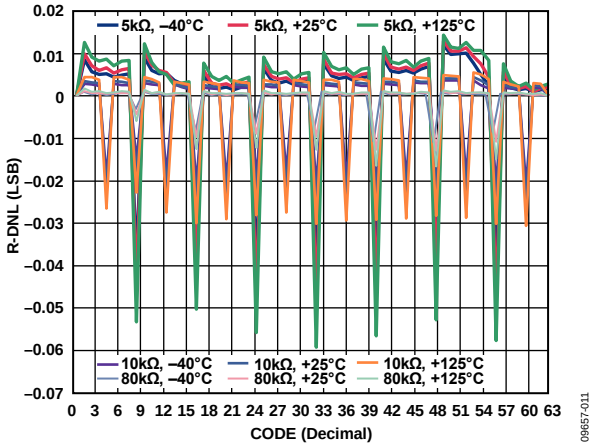

Figure 11. R-DNL vs. Code

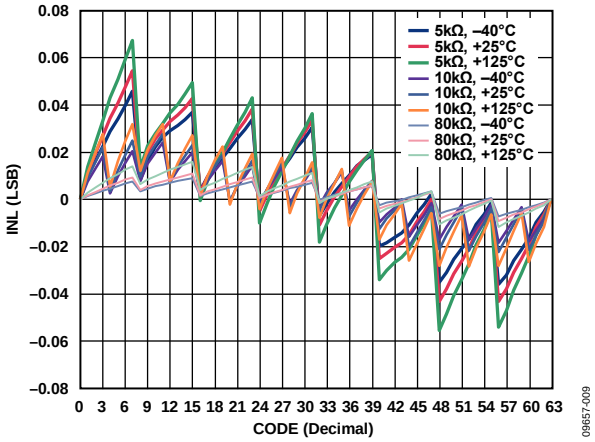

Figure 9. INL vs. Code

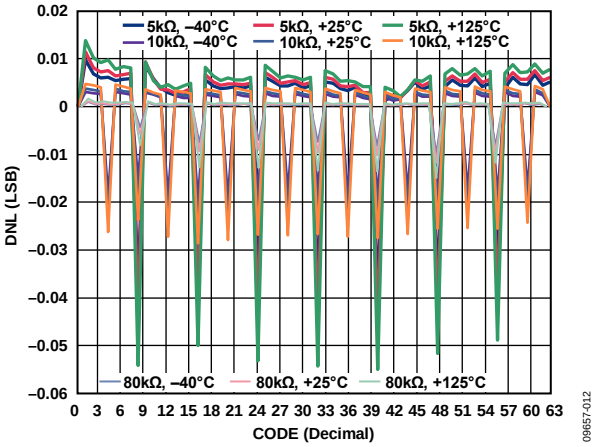

Figure 12. DNL vs. Code

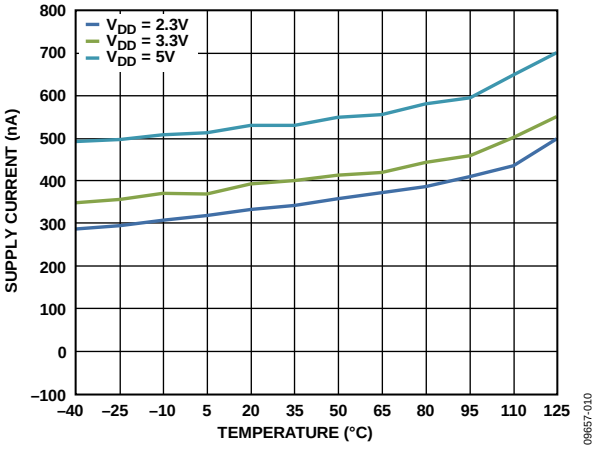

Figure 10. Supply Current vs. Temperature

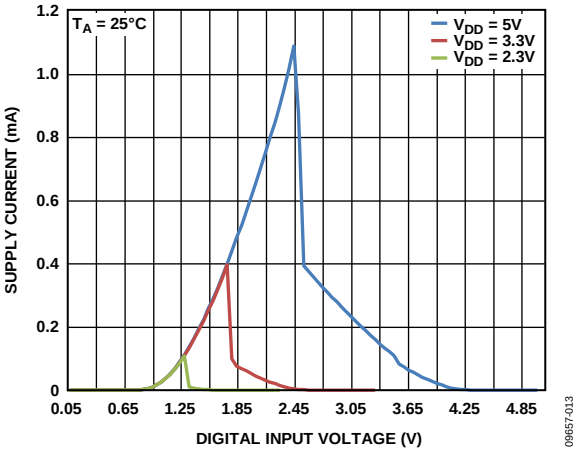

Figure 13. Supply Current (I_{DD}) vs. Digital Input Voltage

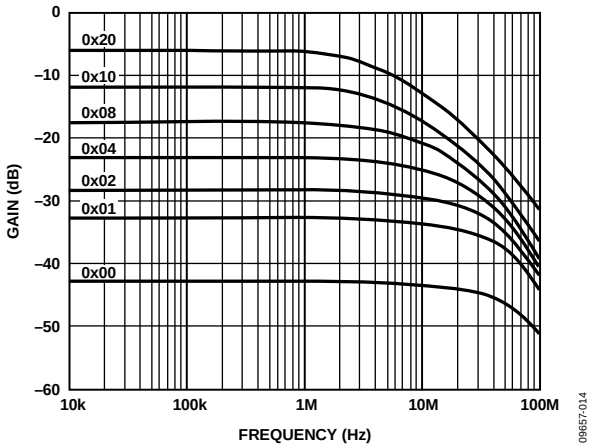

Figure 14. 5 kΩ Gain vs. Frequency vs. Code

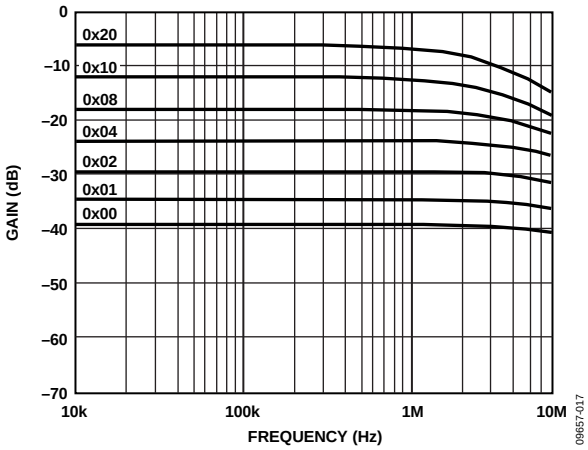

Figure 17. 10 kΩ Gain vs. Frequency vs. Code

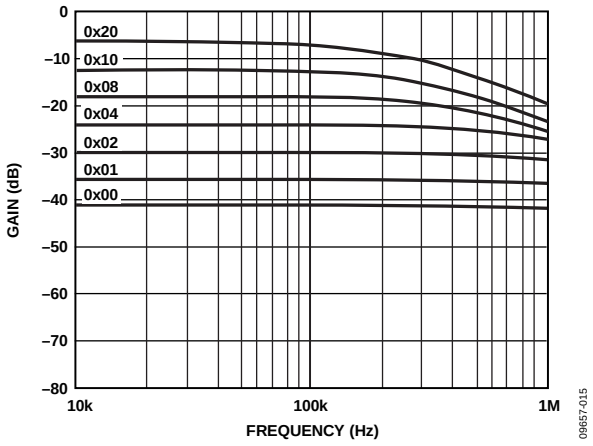

Figure 15. 80 kΩ Gain vs. Frequency vs. Code

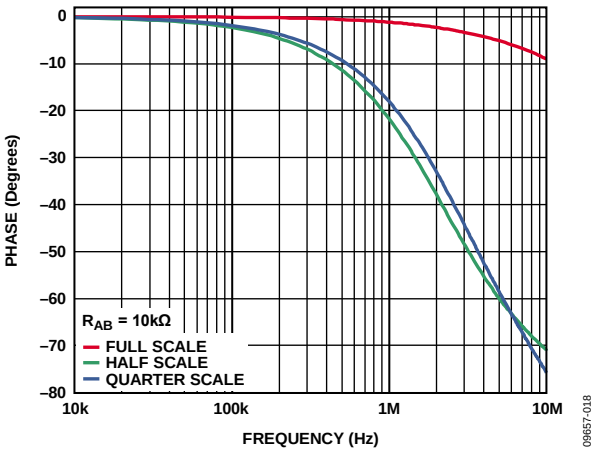

Figure 18. Normalized Phase Flatness vs. Frequency

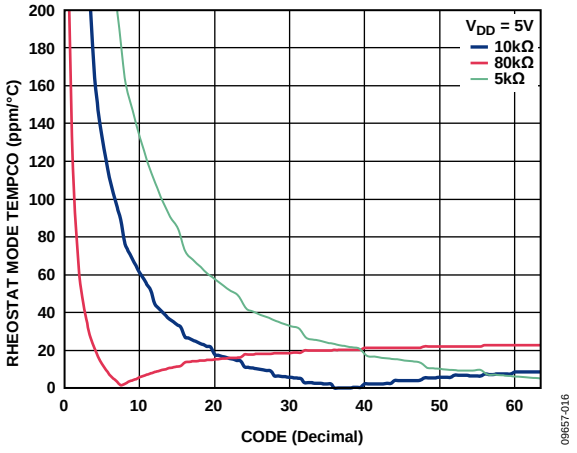

Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

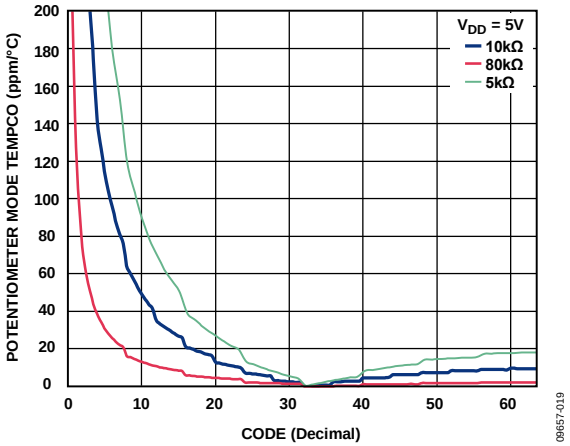

Figure 19. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

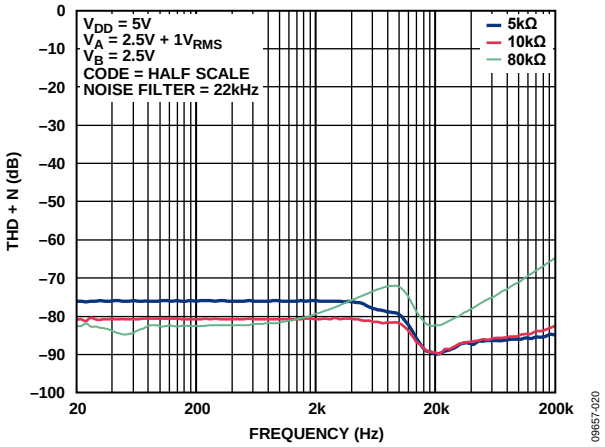

Figure 20. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

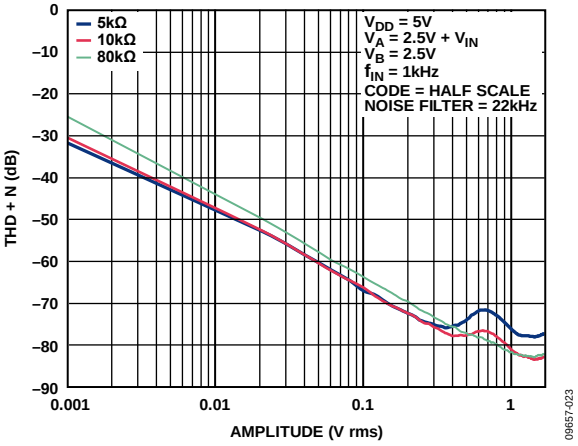

Figure 23. Total Harmonic Distortion + Noise (THD + N) vs. Amplitude

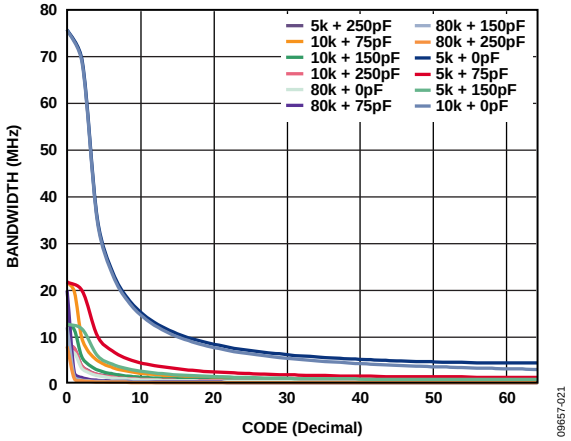

Figure 21. Maximum Bandwidth vs. Code vs. Net Capacitance

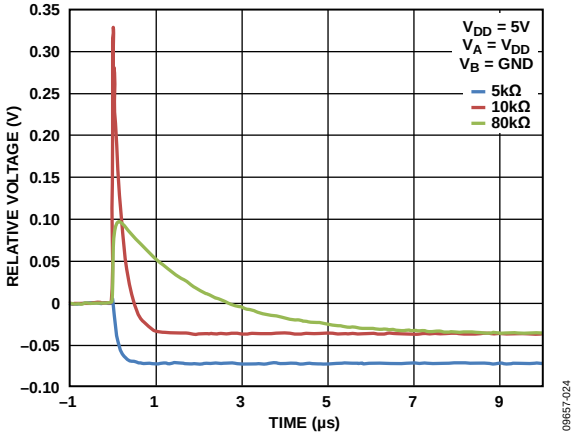

Figure 24. Maximum Transition Glitch

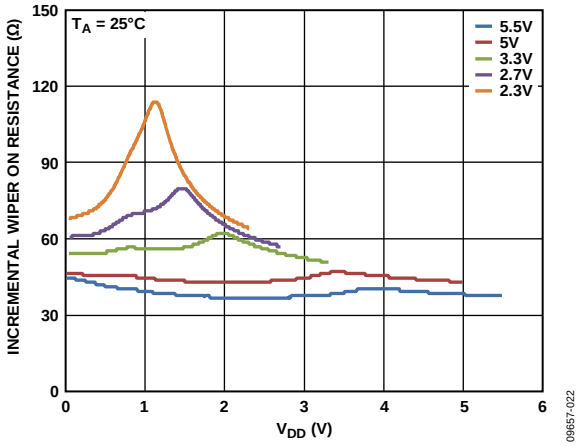

Figure 22. Incremental Wiper on Resistance vs. V_{DD}

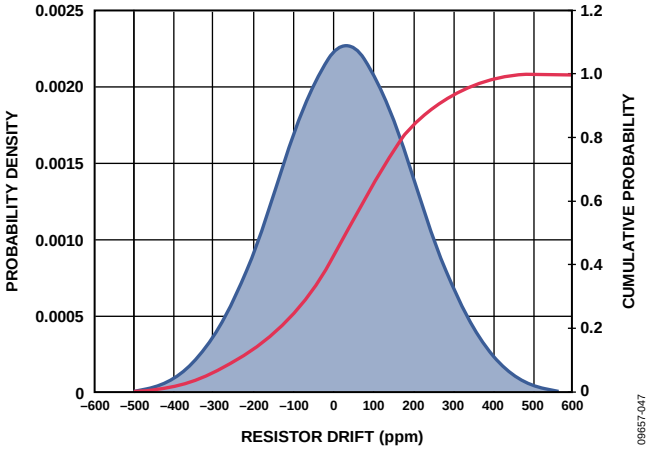

Figure 25. Resistor Lifetime Drift

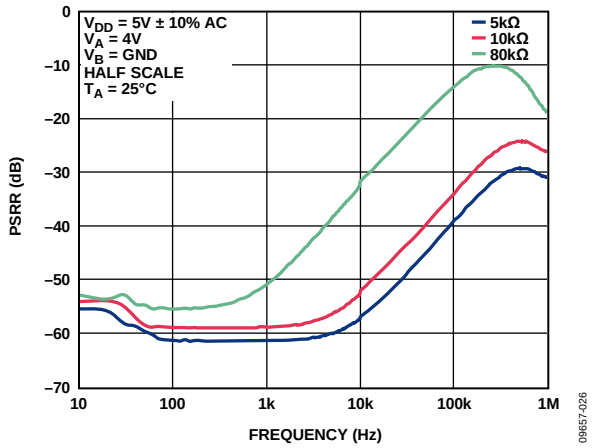

Figure 26. Power Supply Rejection Ratio (PSRR) vs. Frequency

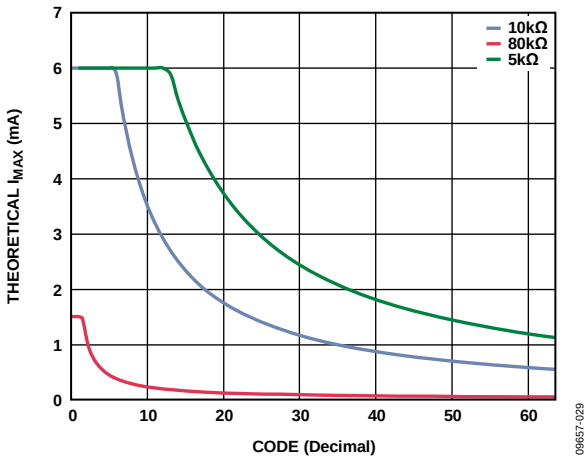

Figure 29. Theoretical Maximum Current vs. Code

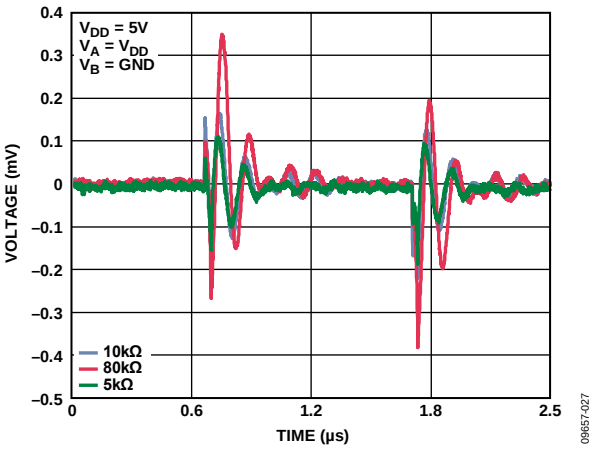

Figure 27. Digital Feedthrough

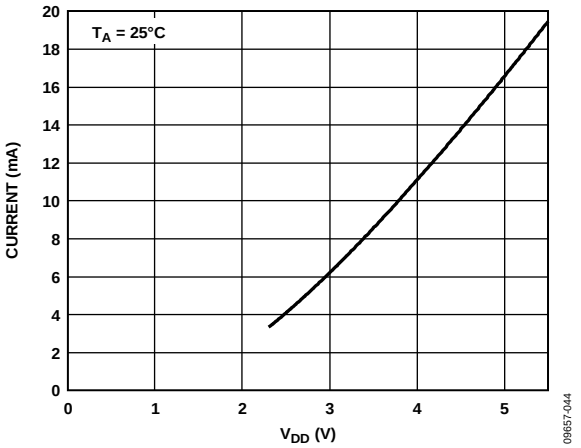

Figure 30. Maximum $\overline{ASE}$ Output Current vs. Voltage

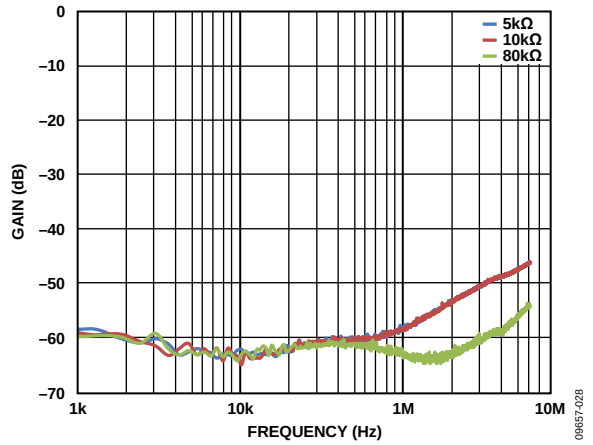

Figure 28. Shutdown Isolation vs. Frequency

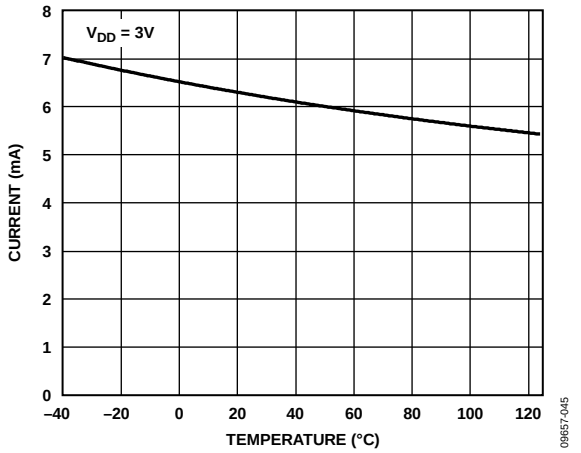

Figure 31. Maximum $\overline{ASE}$ Output Current vs. Temperature

TEST CIRCUITS

Figure 32 to Figure 37 define the test conditions used in the Specifications section.

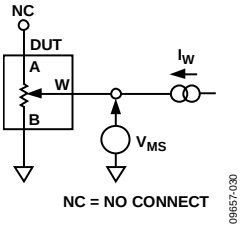

Figure 32. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

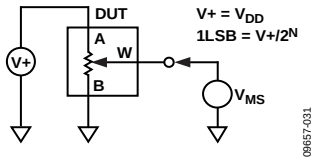

Figure 33. Potentiometer Divider Nonlinearity Error (INL, DNL)

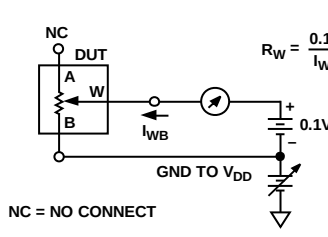

Figure 34. Wiper Resistance

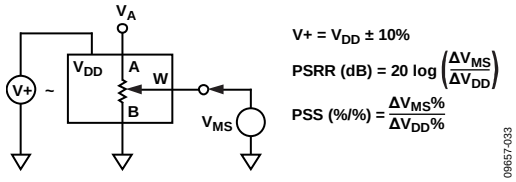

Figure 35. Power Supply Sensitivity (PSS, PSRR)

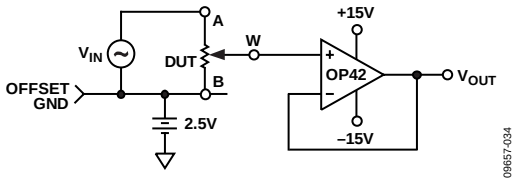

Figure 36. Gain and Phase vs. Frequency

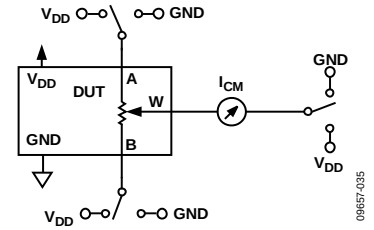

Figure 37. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5116 digital programmable resistor is designed to operate as a true variable resistor for analog signals within the terminal voltage range of GND < V_{TERM} < V_{DD}. The resistor wiper position is determined by the RDAC register contents. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

The RDAC register can be programmed with any position setting using the push button interface. Once a desirable wiper position is found, this value can be stored in the EEPROM memory. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of EEPROM data takes approximately 20 ms; during this time, the device is locked and does not accept any new operation, thus preventing any changes from taking place.

The AD5116 is designed to support external push buttons (tactile switches) directly, as shown in Figure 1.

RDAC REGISTER

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is 0x20, the wiper is connected to midscale of the variable resistor. The RDAC register is controlled using the PD and PU push buttons. The step-up and step-down operations require the activation of the PU (push-up) and PD (push-down) pins. These pins have 100 kΩ internal pull-up resistors that PU and PD activate at logic high. The following paragraphs explain how to increment the RDAC register, but all the descriptions are valid to decrement the RDAC register, swapping PU by PD.

Manual Increment

The AD5116 features an adaptive debouncer that monitors the duration of the logic high level of PU signal between bounces. If the PU logic high level signal duration is shorter than 8 ms, the debouncer ignores it as an invalid incrementing command. Whenever the logic high level of PU signal lasts longer than 8 ms, the debouncer assumes that the last bounce is met and, therefore, increments the RDAC register by one step. The wiper is incremented by one tap position, as shown in Figure 2.

Auto Scan Increment

If the PU button is held for longer than 1 second, continuously holding it activates auto scan mode, and the AD5116 increments the RDAC register by one step every 140 ms until PU is released. Typical timing is shown in Figure 3.

Low Wiper Resistance Feature

The AD5116 includes extra steps to achieve a minimum wiper resistance. Between Terminal W and Terminal B, this extra step is called bottom scale and the wiper resistance decreases from 70 Ω to 45 Ω. Between Terminal A and Terminal W, this extra step is called top scale and connects the A and W terminals, reducing the 1 LSB resistor typical at full-scale code. These new extra steps are loaded automatically in the RDAC register after zero-scale or full-scale position has been reached. The extra steps are not equal to 1 LSB, and are not included in the INL, DNL, R-INL, and R-DNL specifications.

Whenever the minimum R_{WB} (= R_{BS}) is reached, the resistance stops decrementing. Any continuous holding of the PD to logic high simply elevates the supply current. When R_{AW} reaches the minimum resistance (= R_{TS}), continuous holding of PU only elevates the supply current.

EEPROM

The AD5116 contains an EEPROM memory that allows wiper position storage. Once a desirable wiper position is found, this value can be saved into the EEPROM. Thereafter, the wiper position will always be set at that position for any future on-off-on power supply sequence.

AUTOMATIC SAVE ENABLE

At power-up, the AD5116 checks the level in the $\overline{ASE}$ pin. If the pin is pulled low, as shown in Figure 38, the automatic store is enabled. If the pin is pulled high, as shown in Figure 39, automatic store is disabled and the RDAC register should be stored manually. During the storage cycle, the device is locked and does not accept any new operation preventing any changes from taking place.

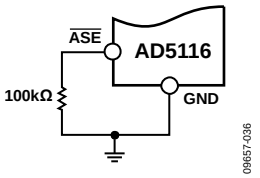

Figure 38. Automatic Store Enables

Auto Save

If there is no activity on inputs during 1 second, the AD5116 stores the RDAC register data into EEPROM, as shown in Figure 4.

Manual Store

The storage is controlled by the $\overline{ASE}$ pin, which is connected to an adaptive debouncer. If the $\overline{ASE}$ pin is pulled low longer than 8 ms, the AD5116 saves the RDAC register data into EEPROM, as shown in Figure 5.

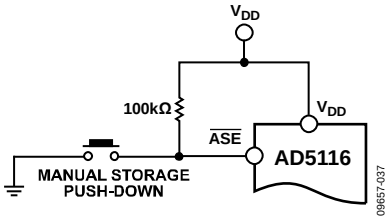

Figure 39. Automatic Store Disables with Manual Storage Push Button

END SCALE RESISTANCE INDICATOR

When the auto save mode is enabled, the $\overline{ASE}$ pin also indicates when the RDAC register reaches the maximum or minimum scale. The AD5116 pulls the $\overline{ASE}$ pin high and holds it as long as PD or PU is active, and the part is placed in the end scale resistance (R_{TS} or R_{BS}), as shown in Figure 6. The typical pin configuration is shown in Figure 40.

When the part is placed at the end of the resistance scale (R_{TS} or R_{BS}), the $\overline{ASE}$ pin is pulled high during the debounce time, until the RDAC register is incremented (R_{BS}) or decremented (R_{TS}) by activating PU or PD.

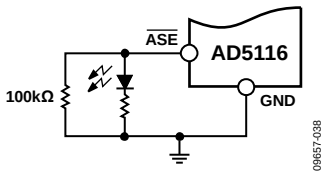

Figure 40. Typical End Scale Indicator Circuit

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5116 employs a two-stage segmentation approach as shown in Figure 41. The AD5116 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from V_{DD}.

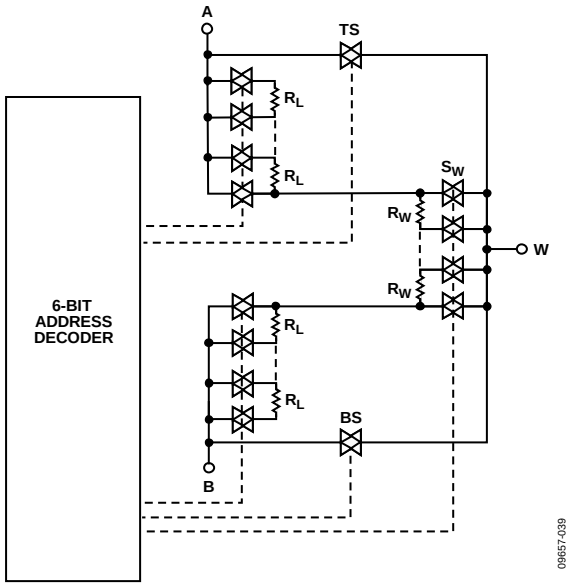

Figure 41. Simplified RDAC Circuit

Top Scale/Bottom Scale Architecture

In addition, the AD5116 includes a new feature to reduce the resistance between terminals. These extra steps are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 70 Ω to 45 Ω. At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB and the total resistance is reduced to 70 Ω. The extra steps are not equal to 1 LSB and are not included in the INL, DNL, R-INL, and R-DNL specifications.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—±8% Resistor Tolerance

The AD5116 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating or tied to the W terminal as shown in Figure 42.

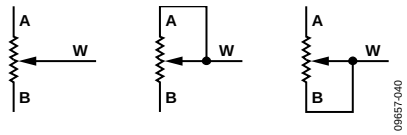

Figure 42. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is available in 5 kΩ, 10 kΩ, and 80 kΩ and has 64 tap points accessed by the wiper terminal. The 6-bit data in the RDAC latch is decoded to select one of the 64 possible wiper settings. The general equation for determining the digitally programmed output resistance between the W terminal and B terminal is:

$$R_{WB} = R_{BS} \quad \text{Bottom scale} \quad (1)$$

$$R_{WB}(D) = \frac{D}{64} \times R_{AB} + R_W \quad \text{From 0 to 64} \quad (2)$$

where:
D is the decimal equivalent of the binary code in the 6-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_{BS} is the wiper resistance at bottom scale.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equation for this operation is:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale} \quad (3)$$

$$R_{AW}(D) = \frac{64 - D}{64} \times R_{AB} + R_W \quad \text{From 0 to 63} \quad (4)$$

$$R_{AW} = R_{TS} \quad \text{Top scale} \quad (5)$$

where:
D is the decimal equivalent of the binary code in the 6-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.
R_{TS} is the wiper resistance at top scale.

Regardless of which setting the part is operating in, take care to limit the current between the A terminal to B terminal, W terminal to A terminal, and W terminal to B terminal, to the maximum continuous current or pulsed current specified in Table 4. Otherwise, degradation or possible destruction of the internal switch contact can occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B, as shown in Figure 43. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-to-B, W-to-A, and W-to-B can be at either polarity.

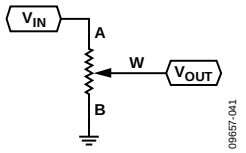

Figure 43. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for simplicity, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 5 V. The general equation defining the output voltage at V_W, with respect to ground for any valid input voltage applied to Terminal A and Terminal B, is:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B \quad (6)$$

where:
$R_{WB}(D)$ can be obtained from Equation 1 or Equation 2.
$R_{AW}(D)$ can be obtained from Equation 3 to Equation 5 .

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

TERMINAL VOLTAGE OPERATING RANGE

The AD5116 is designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on Terminal A, Terminal B, or Terminal W that exceed V_{DD} are clamped by the forward-biased diode. There is no polarity constraint between V_A, V_W, and V_B, but they cannot be higher than V_{DD} or lower than GND.

POWER-UP SEQUENCE

Because of the ESD protection diodes that limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 44), it is important to power on V_{DD} before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diodes are forward-biased such that V_{DD} is powered on unintentionally and can affect other parts of the circuit. Similarly, V_{DD} should be powered down last. The ideal power-on sequence is in the following order: GND, V_{DD}, and $V_A/V_B/V_W$. The order of powering V_A, V_B, and V_W is not important as long as they are powered on after V_{DD}. The states of the PU and PD pins can be logic low or floating, but they should not be logic high during power-on.

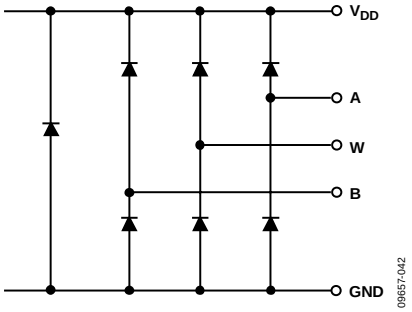

Figure 44. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 45 illustrates the basic supply bypassing configuration for the AD5116.

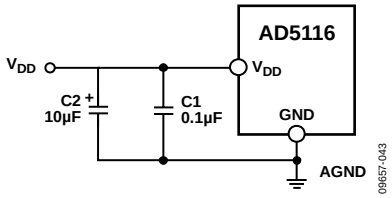

Figure 45. Power Supply Bypassing

OUTLINE DIMENSIONS

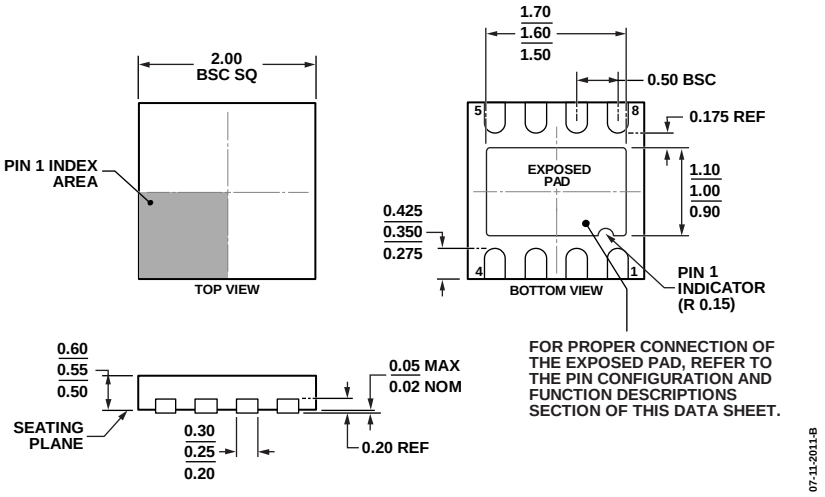

Figure 46. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option	Branding Code
AD5116BCPZ5-RL7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7G
AD5116BCPZ5-500R7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7G
AD5116BCPZ10-RL7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7F
AD5116BCPZ10-500R7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7F
AD5116BCPZ80-RL7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7H
AD5116BCPZ80-500R7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	CP-8-10	7H
EVAL-AD5116EBZ				Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5116EBZ has an R_{AB} of 10 kΩ.

D09657-0-11/12(B)