April 1988
Revised October 2000

74F675A
16-Bit Serial-In, Serial/Parallel-Out Shift Register

General Description

The 74F675A contains a 16-bit serial in/serial out shift register and a 16-bit parallel out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

Features

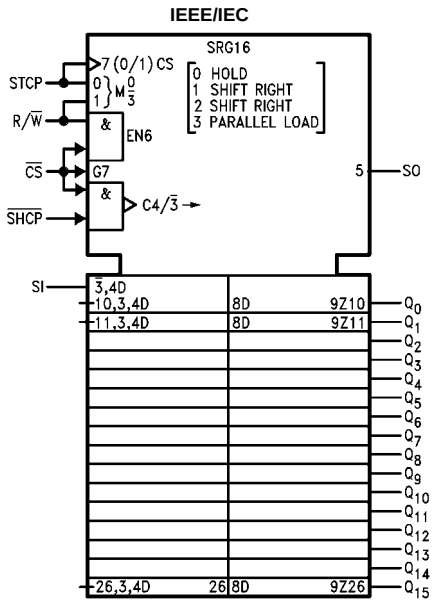
- Serial-to-parallel converter
- 16-Bit serial I/O shift register
- 16-Bit parallel out storage register
- Recirculating parallel transfer
- Expandable for longer words
- Slim 24 lead package
- 74F675A version prevents false clocking through $\overline{CS}$ or R/$\overline{W}$ inputs

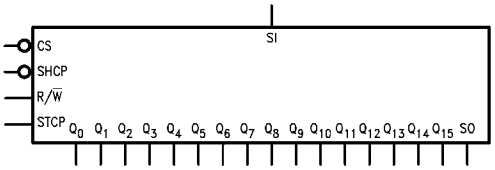
Ordering Code:

Order Number	Package Number	Package Description
74F675ASC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F675APC	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600 Wide
74F675ASPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

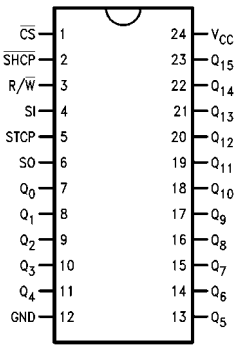
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols





Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
SI	Serial Data Input	1.0/1.0	20 µA/–0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20 µA/–0.6 mA
STCP	Store Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
R/$\overline{W}$	Read/Write Input	1.0/1.0	20 µA/–0.6 mA
SO	Serial Data Output	50/33.3	–1 mA/20 mA
Q_0–Q_{15}	Parallel Data Outputs	50/33.3	–1 mA/20 mA

Functional Description

The 16-Bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift Right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

Shift Register Operations Table

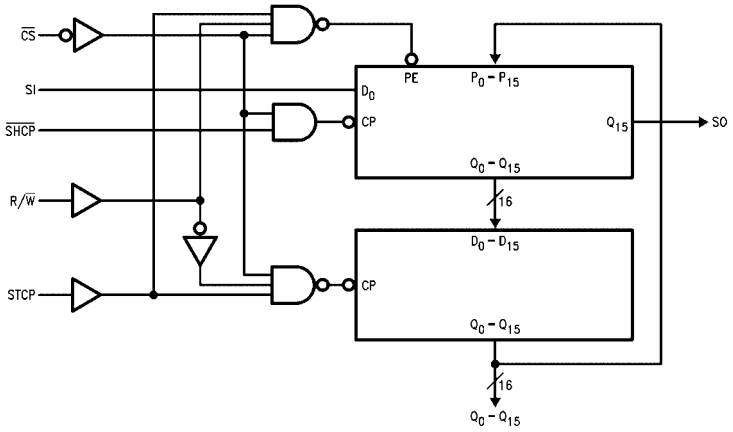
Control Inputs				Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↘	X	Shift Right
L	H	↘	L	Shift Right
L	H	↘	H	Parallel Load, No Shifting

Storage Register Operations Table

Inputs			Operating Mode
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↗	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↘ = HIGH-to-LOW Transition
↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			106	160	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			106	160	mA	Max	V_O = LOW

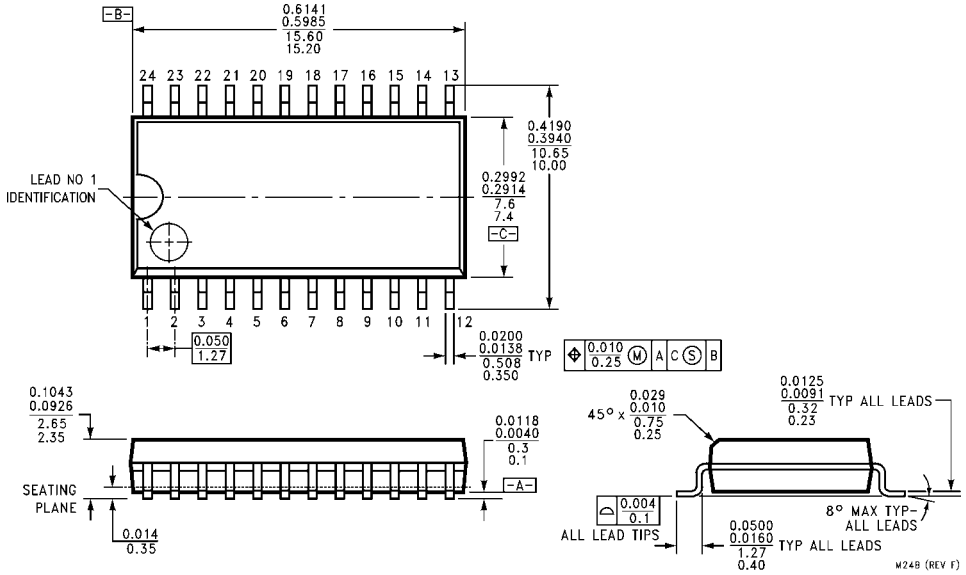
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100	130		85		MHz
t_{PLH}	Propagation Delay	3.0	8.0	10.5	2.5	12.0	ns
t_{PHL}	STCP to Q_n	3.0	10.5	13.5	2.5	15.0	
t_{PLH}	Propagation Delay	4.0	7.0	9.5	3.5	10.5	ns
t_{PHL}	$\overline{SHCP}$ to SO	4.5	8.0	10.5	4.0	12.0	

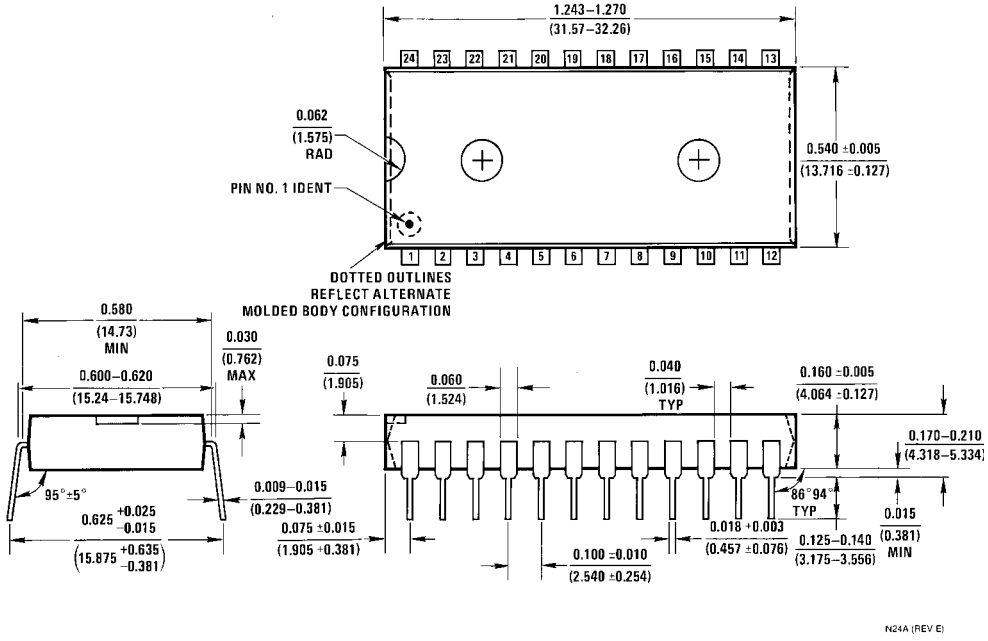
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	3.5		4.0		ns
$t_S(L)$	$\overline{CS}$ or R/$\overline{W}$ to STCP	5.5		6.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	$\overline{CS}$ or R/$\overline{W}$ to STCP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.5		ns
$t_S(L)$	SI to $\overline{SHCP}$	3.0		3.5		
$t_H(H)$	Hold Time, HIGH or LOW	3.0		3.5		
$t_H(L)$	SI to $\overline{SHCP}$	3.0		3.5		
$t_S(H)$	Setup Time, HIGH or LOW	6.5		7.5		ns
$t_S(L)$	R/$\overline{W}$ to $\overline{SHCP}$	9.0		10.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	R/$\overline{W}$ to $\overline{SHCP}$	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	7.0		8.0		ns
$t_S(L)$	STCP to $\overline{SHCP}$	7.0		8.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	STCP to $\overline{SHCP}$	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.5		ns
$t_S(L)$	$\overline{CS}$ to $\overline{SHCP}$	3.0		3.5		
$t_H(H)$	Hold Time, HIGH or LOW	3.0		3.5		
$t_H(L)$	$\overline{CS}$ to $\overline{SHCP}$	3.0		3.5		
$t_W(H)$	$\overline{SHCP}$ Pulse Width	5.0		6.0		ns
$t_W(L)$	HIGH or LOW	5.0		6.0		
$t_W(H)$	STCP Pulse Width	6.0		7.0		
$t_W(L)$	HIGH or LOW	5.0		6.0		
$t_S(L)$	$\overline{SHCP}$ to STCP	8.0		9.0		ns
$t_H(H)$	$\overline{SHCP}$ to STCP	0.0		0.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted

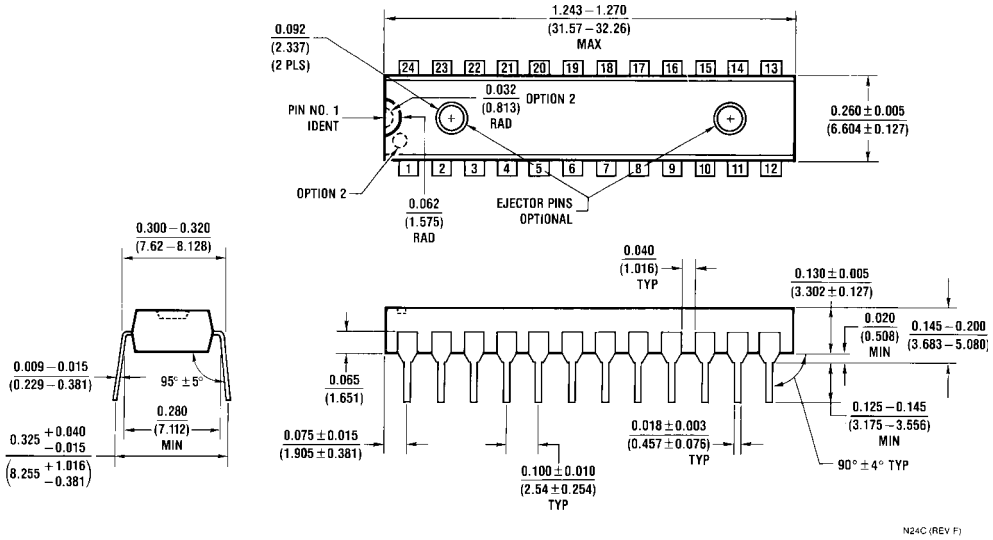


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600 Wide
Package Number N24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N24C

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