1 Characteristics

Table 2. Electrical Characteristics (Tj = 25° C, unless otherwise specified)

Symbol	Test Conditions	Quadrant		Z04				Unit
				02	05	09	10	
I_{GT} (1)	V_D = 12 V R_L = 30 Ω	I - II - III - IV	MAX.	3	5	10	25	mA
V_{GT}		ALL	MAX.	1.3				V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ T_j = 125° C	ALL	MIN.	0.2				V
I_H (2)	I_T = 50 mA		MAX.	3	5	10	25	mA
I_L	$I_G = 1.2\ I_{GT}$	I - III - IV	MAX.	6	10	15	25	mA
		II		12	15	25	50	
dV/dt (2)	V_D = 6 % V_{DRM} gate open T_j = 110° C		MIN.	10	20	100	200	V/µs
(dV/dt)c (2)	(dI/dt)c = 1.8 A/ms T_j = 110° C		MIN.	0.5	1	2	5	V/µs

1. minimum IGT is guaranted at 5% of IGT max.
2. for both polarities of A2 referenced to A1.

Table 3. Static Characteristics

Symbol	Test Conditions			Value	Unit
V_{TM} (1)	I_{TM} = 5.5 A t_p = 380 µs	T_j = 25° C	MAX.	2.0	V
V_{to} (1)	Threshold voltage	T_j = 125° C	MAX.	0.95	V
R_d (1)	Dynamic resistance	T_j = 125° C	MAX.	180	mΩ
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$	T_j = 25° C	MAX.	5	µA
		T_j = 125° C		0.5	mA

1. for both polarities of A2 referenced to A1.

Table 4. Thermal resistances

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction to lead (AC)	15	° C/W
$R_{th(j-a)}$	Junction to ambient	100	° C/W

Figure 1. Maximum power dissipation versus RMS on-state current (full cycle)

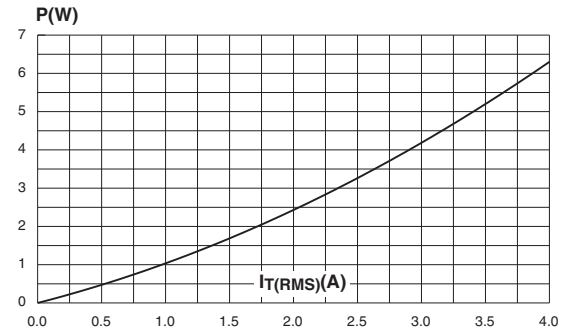


Figure 2. RMS on-state current versus ambient temperature (full cycle)

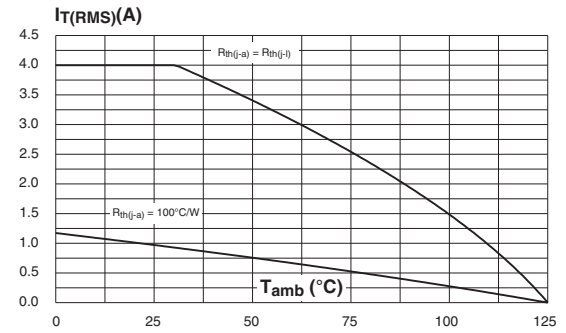


Figure 3. Relative variation of thermal impedance versus pulse duration

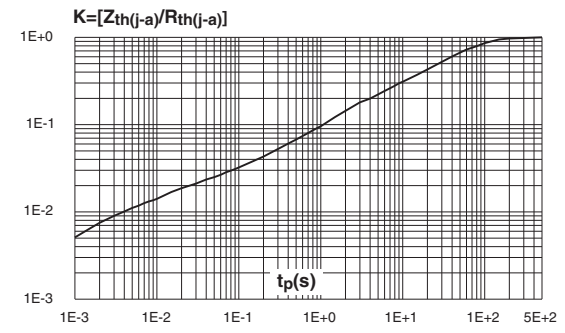


Figure 4. Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

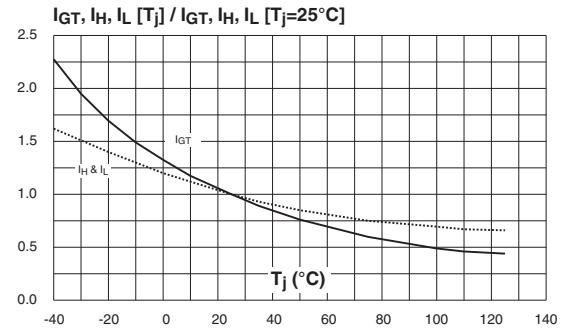


Figure 5. Surge peak on-state current versus number of cycles

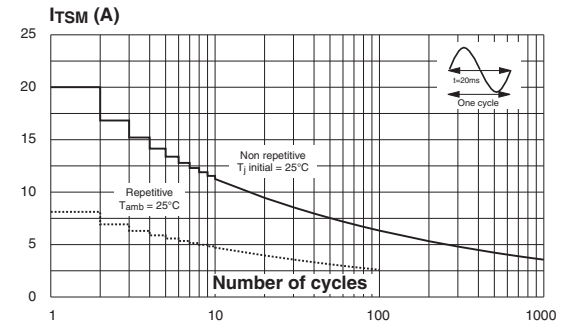


Figure 6. Non-repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms and corresponding value of I^2t

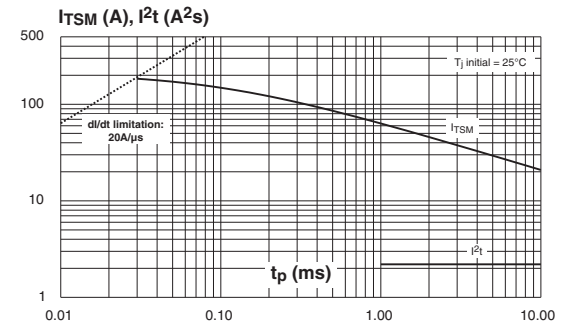


Figure 7. On-state characteristics (maximum values)

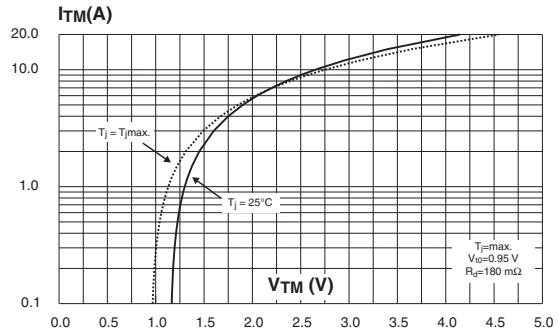


Figure 8. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

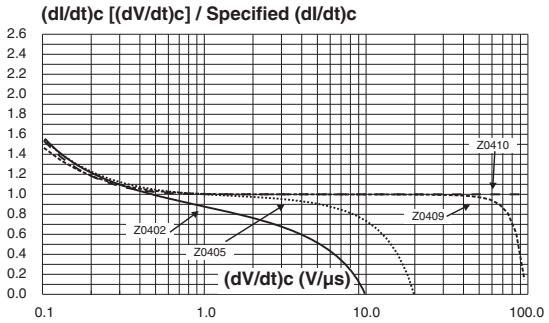
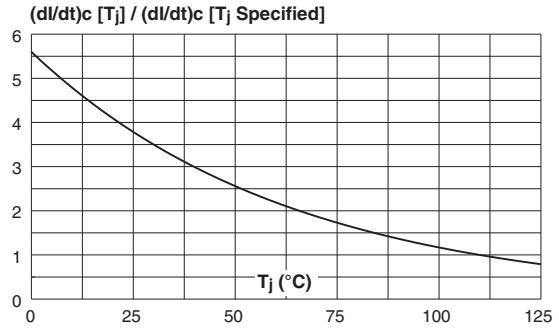


Figure 9. Relative variation of critical rate of decrease of main current versus junction temperature



2 Ordering information scheme

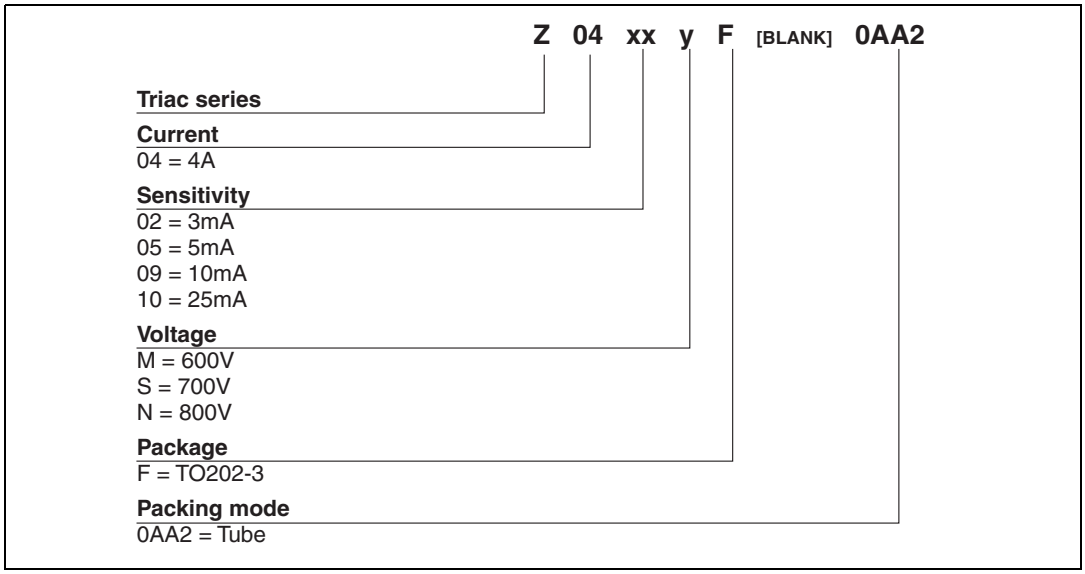
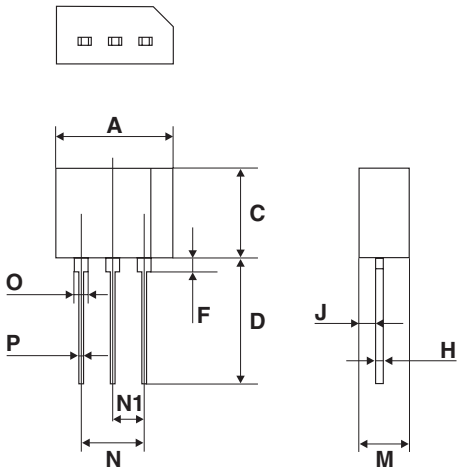


Table 5. Product selector

Part Number	Voltage			Sensitivity	Type	Package
	600 V	700 V	800 V			
Z0402MF	X			3 mA	Standard	TO202-3
Z0402SF		X		3 mA		
Z0402NF			X	3 mA		
Z0405MF	X			5 mA		
Z0405SF		X		5 mA		
Z0405NF			X	5 mA		
Z0409MF	X			10 mA		
Z0409SF		X		10 mA		
Z0409NF			X	10 mA		
Z0410MF	X			25 mA		
Z0410SF		X		25 mA		
Z0410NF			X	25 mA		

3 Package information



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			10.1			0.398
C		7.3			0.287	
D		10.5			0.413	
F			1.5			0.059
H		0.51			0.020	
J		1.5			0.059	
M		4.5			0.177	
N			5.3			0.209
N1		2.54			0.100	
O			1.4			0.055
P			0.7			0.028

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Ordering type	Marking	Weight	Base qty	Delivery mode
Z04xxyF 0AA2(1)	Z04xxyF(1)	0.8 g	50	Tube

1. xx = sensitivity, y = voltage

5 Revision history

Date	Revision	Description of Changes
Oct-2001	4	Last update.
13-Feb-2006	5	TO202-3 delivery mode changed from bulk to tube. ECOPACK statement added.
31-Mar-2006	6	Reformatted to current standard. Lead marking changed on page 1
12-05-2006	7	Typographical error for (dV/dt)c corrected in Table 2.

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