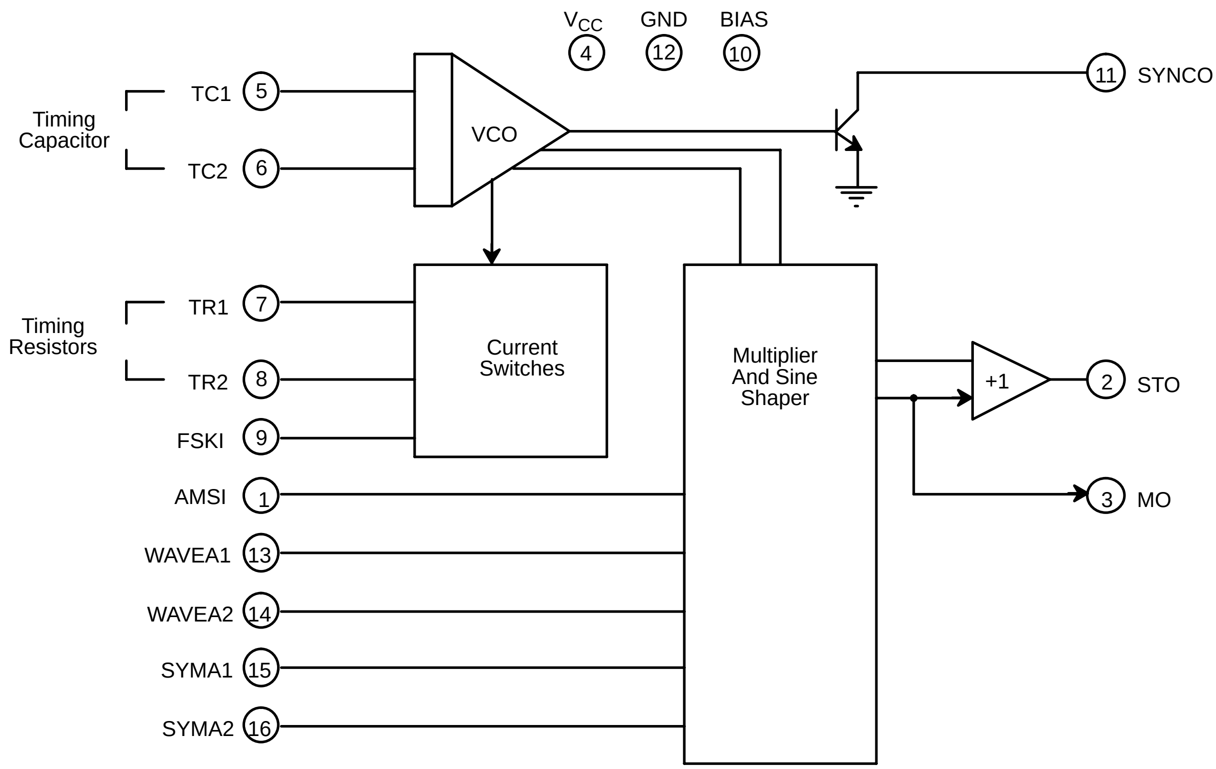
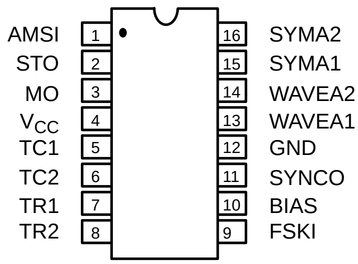
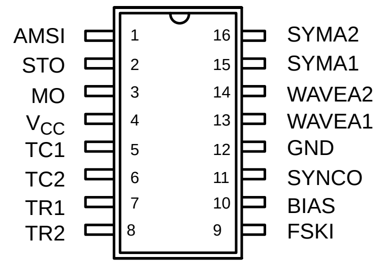


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 2* **Vcc = 12V, T_A = 25°C, C = 0.01μF, R_1 = 100kΩ, R_2 = 10kΩ, R_3 = 25kΩ** Unless Otherwise Specified. S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics								
Single Supply Voltage	**10**		**26**	10		26	V	
Split-Supply Voltage	**±5**		**±13**	±5		±13	V	
Supply Current		12	**17**		14	20	mA	$R_1 \geq 10k\Omega$
Oscillator Section								
Max. Operating Frequency	**0.5**	1		0.5	1		MHz	C = 1000pF, R_1 = 1kΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50μF, R_1 = 2MΩ
Frequency Accuracy		±1	**±4**		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability Frequency		±10	**±50**		±20		ppm/°C	$0°C \leq T_A \leq 70°C$ $R_1 = R_2$ = 20kΩ
Sine Wave Amplitude Stability[2]		4800			4800		ppm/°C	
Supply Sensitivity		0.01	**0.1**		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2$ = 20kΩ
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1kΩ f_L @ R_1 = 2MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1kHz, f_H = 10kHz
1000:1 Sweep		8			8		%	f_L = 100Hz, f_H = 100kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	**0.001**		100	0.001		100	μF	*Figure 5*
Timing Resistors: R_1 & R_2	**1**		2000	1		2000	kΩ	
Triangle Sine Wave Output[1]								*Figure 3*
Triangle Amplitude		160			160		mV/kΩ	*Figure 2,* S_1 Open
Sine Wave Amplitude	**40**	60	80		60		mV/kΩ	*Figure 2*, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	R_1 = 30kΩ
With Adjustment		0.4	**1.0**		0.5	1.5	%	See *Figure 7* and *Figure 8*

Notes

[1] *Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.*

[2] *For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.*

***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Amplitude Modulation								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	C_L = 10pF
Fall Time		50			50		ns	C_L = 10pF
Saturation Voltage		0.2	**0.4**		0.2	0.6	V	I_L = 2mA
Leakage Current		0.1	**20**		0.1	100	μA	V_{CC} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	**2.4**	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	**3.3**	2.5	3	3.5	V	Measured at Pin 10.

Notes
[1] *Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.*
[2] *For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.*
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
Power Dissipation 750mW
Derate Above 25°C . . . . 5mW/°C
Total Timing Current 6mA
Storage Temperature . . . . -65°C to +150°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

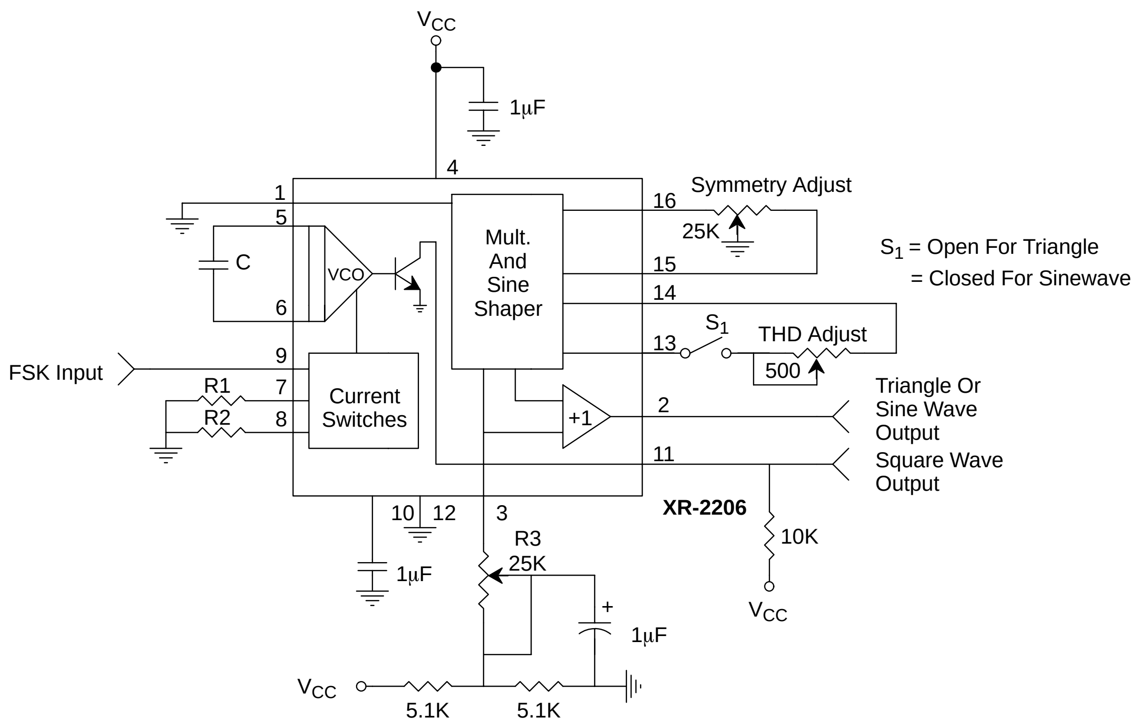


Figure 2. Basic Test Circuit

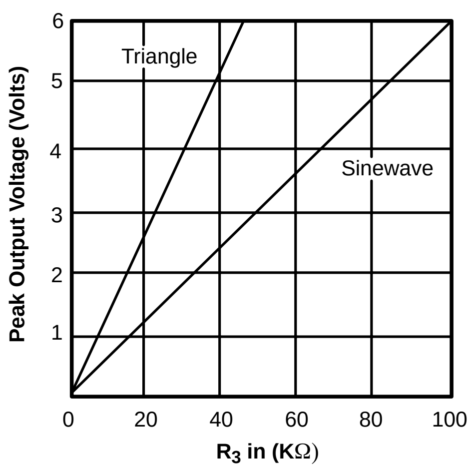


Figure 3. Output Amplitude as a Function of the Resistor, R3, at Pin 3

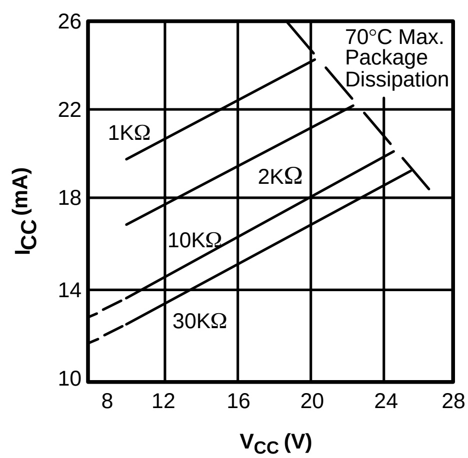


Figure 4. Supply Current vs Supply Voltage, Timing, R

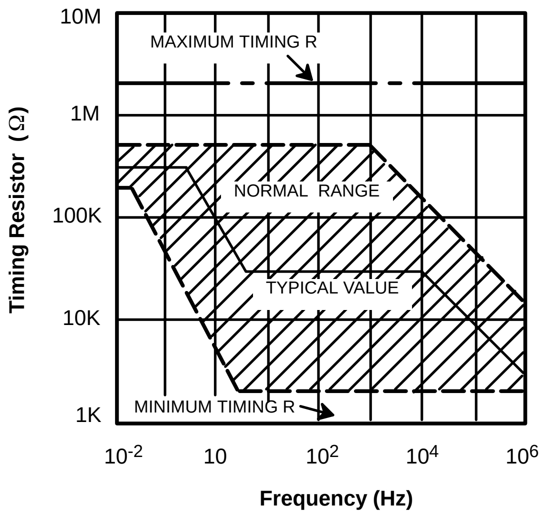


Figure 5. R versus Oscillation Frequency.

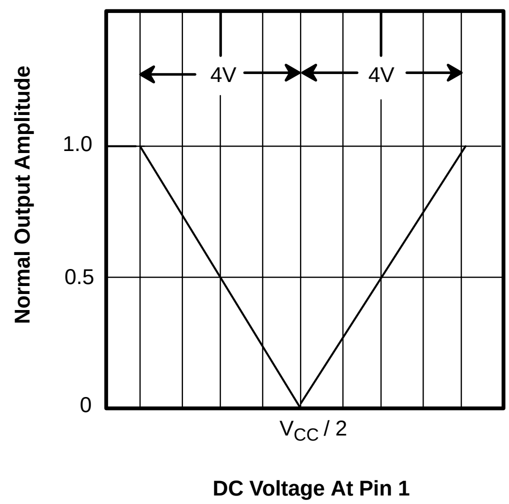


Figure 6. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1)

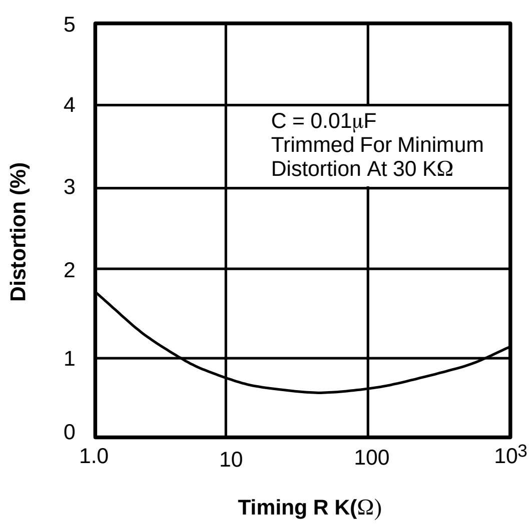


Figure 7. Trimmed Distortion versus Timing Resistor.

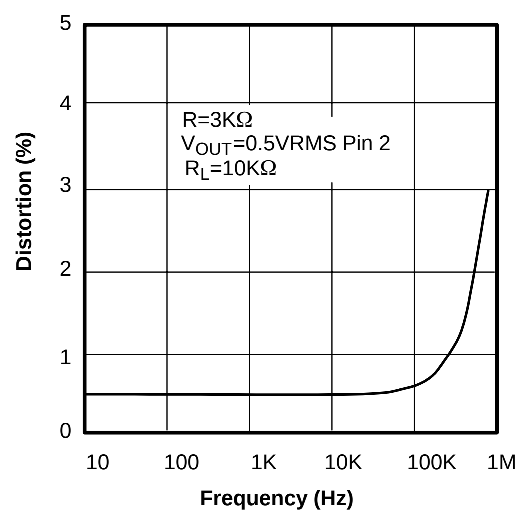


Figure 8. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

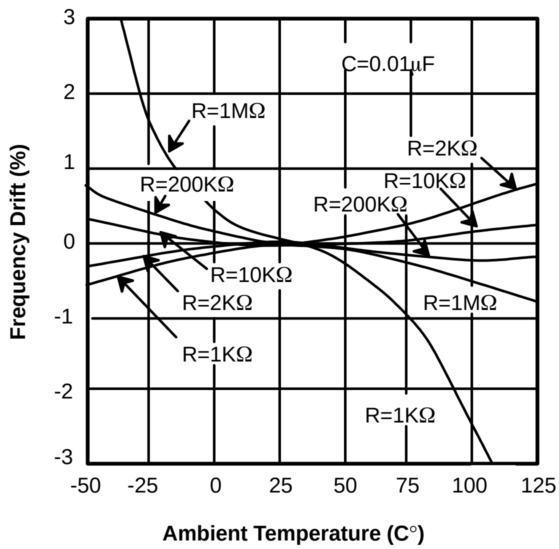


Figure 9. Frequency Drift versus Temperature.

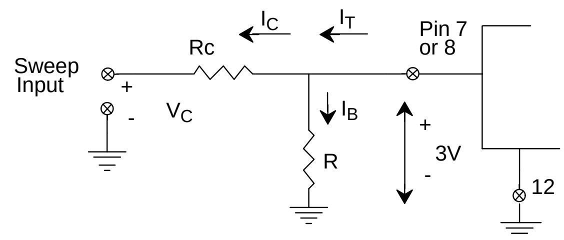


Figure 10. Circuit Connection for Frequency Sweep.

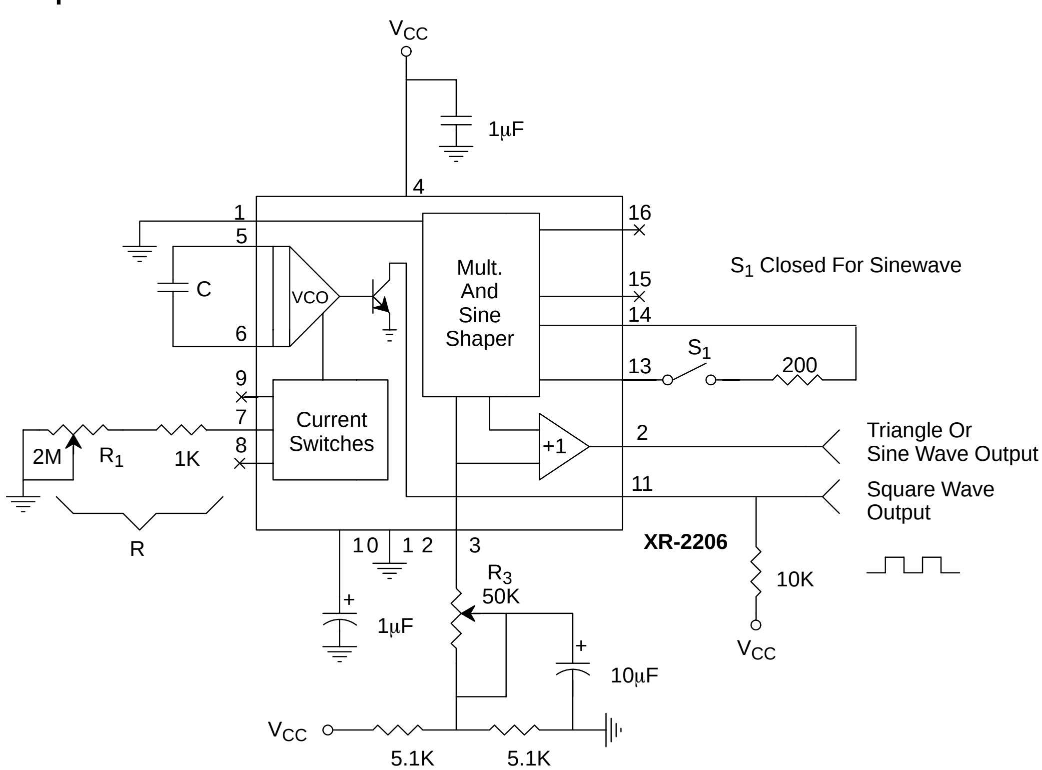


Figure 11. Circuit tor Sine Wave Generation without External Adjustment.
(See *Figure 3* for Choice of R_3)

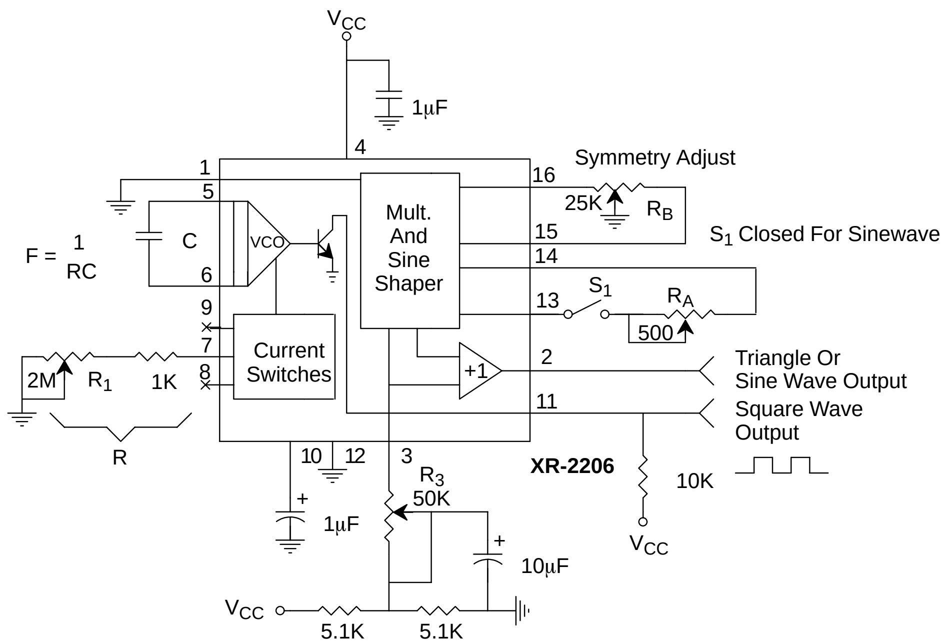


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing - See *Figure 3*)

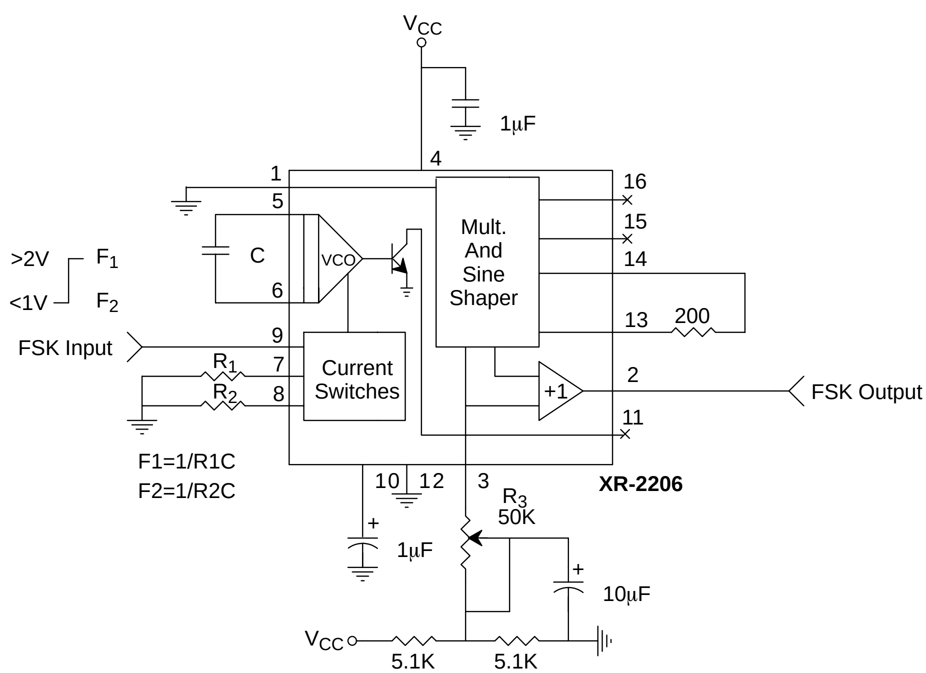


Figure 13. Sinusoidal FSK Generator

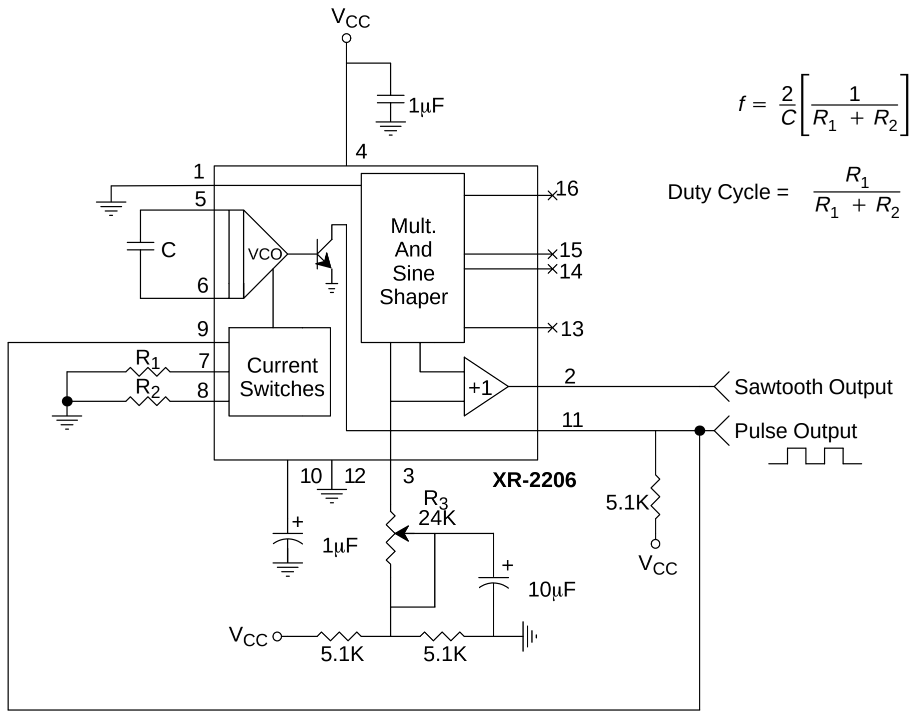


Figure 14. Circuit for Pulse and Ramp Generation.

Frequency-Shift Keying

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in *Figure 13.* Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage $\geq$ 2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is $\leq$1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels. f_1 and f_2, as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-.

Output DC Level Control

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In *Figure 11*, *Figure 12* and *Figure 13*, Pin 3 is biased midway between V+ and ground, to give an output dc level of $\approx$ $V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is < 2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of *Figure 11* can be converted to split-supply operation, simply by replacing all ground connections with V^-. For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to -0.5% by additional adjustments as shown in *Figure 12.* The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of *Figure 11* and *Figure 12* can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 13 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-.

Pulse and Ramp Generation

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1kΩ to 2MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_0 = \frac{1}{RC}\ Hz$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in *Figure 5.* Temperature stability is optimum for 4kΩ < R < 200kΩ. Recommended values of C are from 1000pF to 100µF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320 I_T(mA)}{C(\mu F)}\ Hz$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with IT, over a wide range of current values, from 1µA to 3mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in *Figure 10.* The frequency of oscillation is related to VC as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right) Hz$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_C C}\ \ Hz/V$$

CAUTION: *For safety operation of the circuit, I_T should be limited to $\leq$ 3mA.*

Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see *Figure 3*). For sine wave output, amplitude is approximately 60mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160mV peak per kΩ of R_3. Thus, for example, R_3 = 50kΩ would produce approximately 13V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within 14 volts of $V_{CC}/2$ as shown in *Figure 6.* As this bias level approaches $V_{CC}/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55dB.

CAUTION: *AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of* V_{CC}.

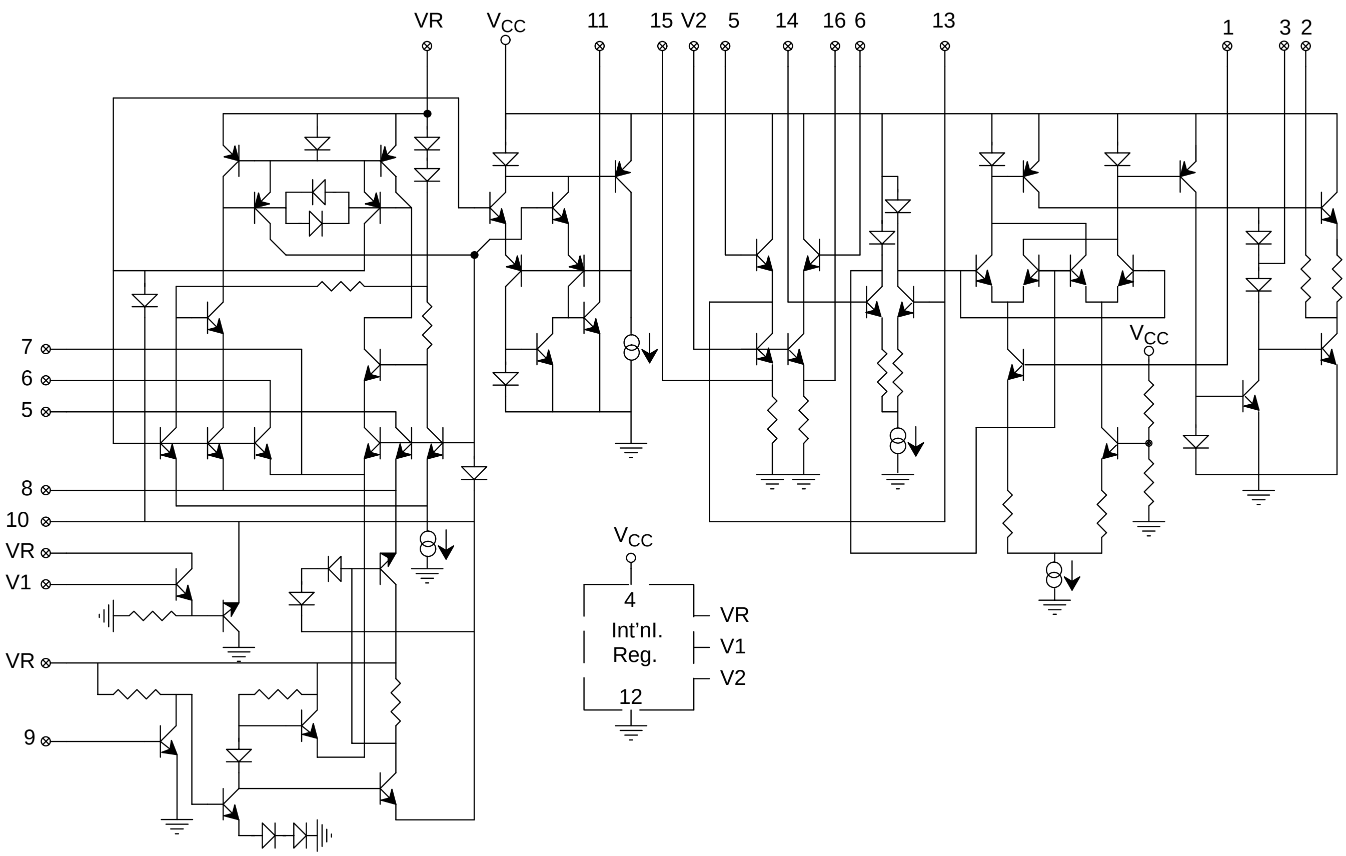
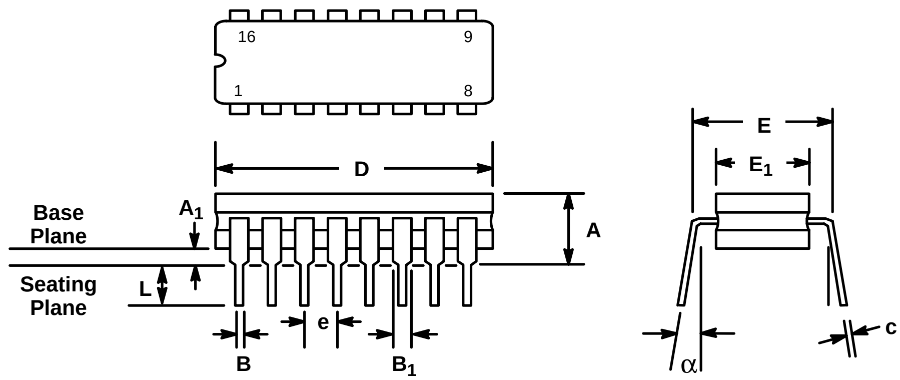


Figure 15. Equivalent Schematic Diagram

16 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

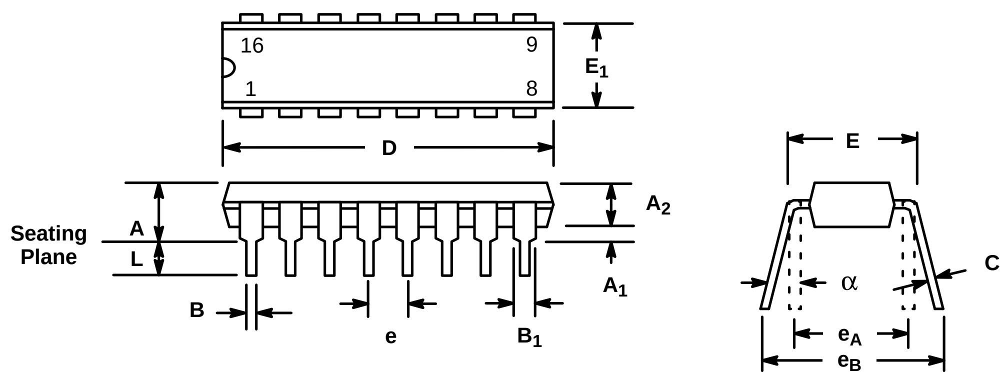


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.740	0.840	18.80	21.34
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)

Rev. 1.00

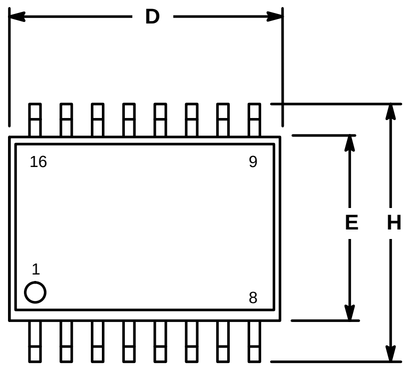


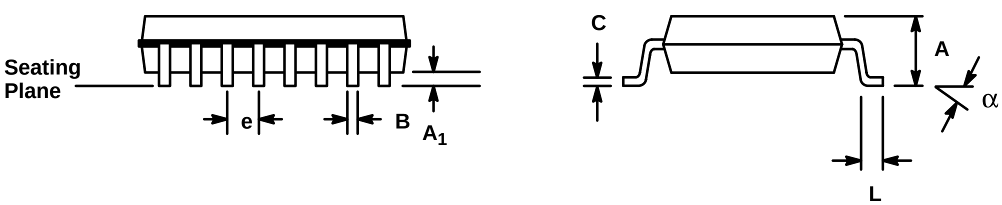
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00





SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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